

Errata

Title & Document Type: 3562A Dynamic Signal Analyzer Service Manual

Manual Part Number: 03562-90010

Revision Date: October 1985

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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SERVICE MANUAL

MODEL 3562A

DYNAMIC SIGNAL ANALYZER

Serial Number: 2435A00101

IMPORTANT NOTICE

This manual applies to instruments with the above serial number and greater. As changes are made in the instrument to improve performance and reliability, the appropriate pages will be revised to include this information.

WARNING

To prevent potential fire or shock hazard, do not expose instrument to rain or moisture.

Manual Part No. 03562-90010
Microfiche No. 03562-90210

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Printed: September 1985



SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.

GROUND THE INSTRUMENT

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SAFETY SYMBOLS

General Definitions of Safety Symbols Used On Equipment or In Manuals.



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.



Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).



OR



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



OR



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

SECTION I

GENERAL INFORMATION

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SECTION I

GENERAL INFORMATION

1-1 HOW THIS MANUAL IS ORGANIZED

This service manual provides all the information required by service personnel to test, adjust, and service the HP 3562A Dynamic Signal Analyzer. Figure 1-1 shows the front and rear views of the HP 3562A and figure 1-2 shows the accessories supplied with the HP 3562A.

The service manual is divided into nine sections, each covering a particular topic for servicing the HP 3562A. A brief description of these sections and when each section should be used is given in table 1-1.

This service manual is designed for troubleshooting the HP 3562A in a two step process. In step one, the information given in Section VII is used to isolate the failure to a circuit board. The information in Section VIII is used to isolate the failure to the component level. To start the troubleshooting process go to section VII.

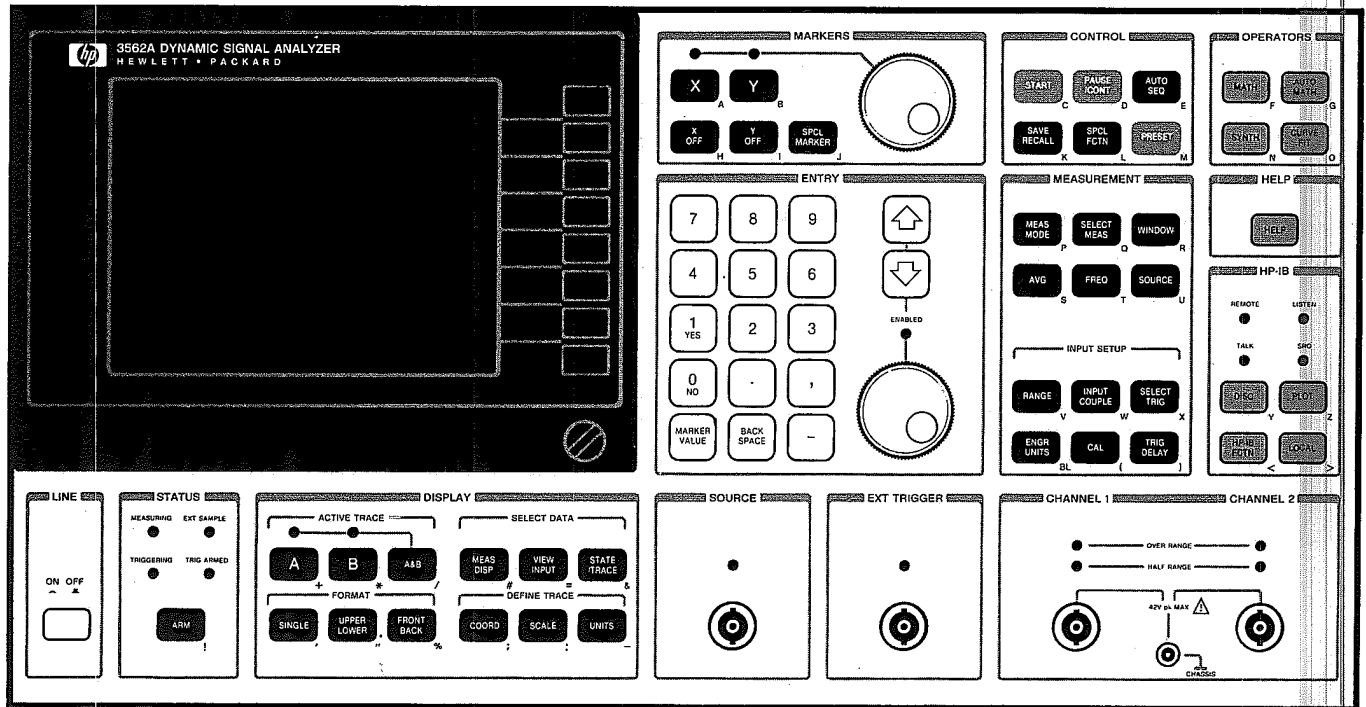
1-2 MANUAL AND INSTRUMENT IDENTIFICATION

The instrument identification serial number is located on the rear panel of the instrument. Hewlett-Packard uses a two section serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter designating the country in which the instrument was manufactured (A = U.S.A., G = West Germany, J = Japan, and U = United Kingdom). The prefix is the same for all identical instruments and changes only when a major instrument change is made. The suffix is unique to each instrument. The contents of this manual apply directly to instruments having the same serial number prefix as listed on the title page of this manual.

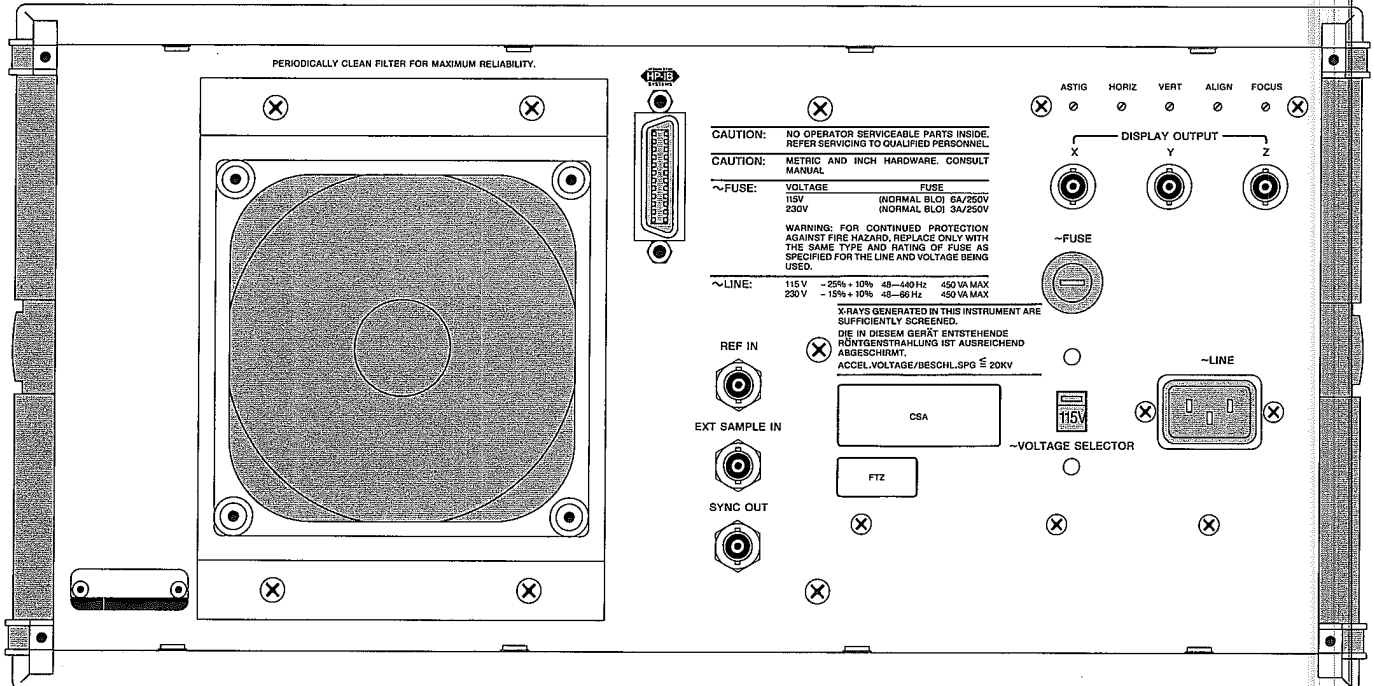
Instruments manufactured after the printing of this manual may have a serial number prefix which is not listed on the title page. This unlisted prefix indicates that the instrument is different from those documented in this manual. The manual for this instrument may be supplied with a yellow "Manual Changes" supplement which contains information documenting the differences.

In addition to instrument change information, the supplement may contain information for correcting the manual. To keep this manual as accurate as possible, Hewlett-Packard recommends that you periodically request the latest "Manual Changes" supplement.

Listed on the title page of this manual is a manual part number and a microfiche part number. The manual part number can be used to order extra copies of this service manual. The microfiche part number can be used to order 4 by 6 inch microfilm transparencies of this service manual.



HP 3562A Front View

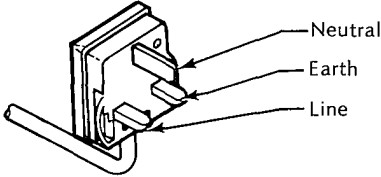
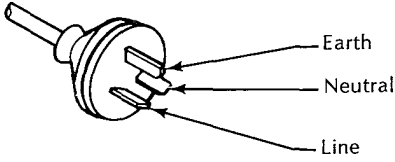
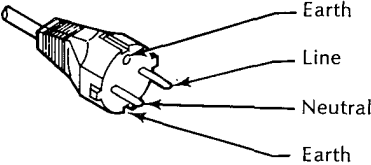
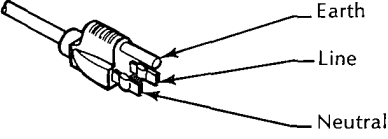
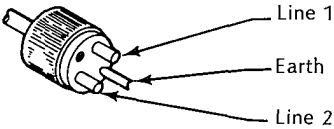
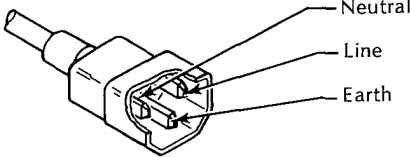
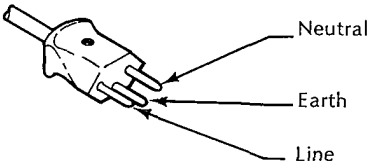
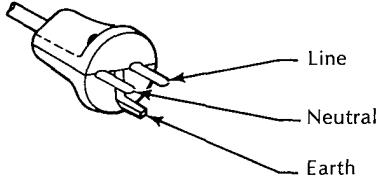


HP 3562A Rear View

Figure 1-1 HP 3562A Front and Rear Views

WARNING

The power cable plug must be inserted into a socket outlet provided with a protective earth terminal. Defeating the protection of the grounded instrument cabinet can subject the operator to lethal voltages.

| | |
|---|---|
|  <p>PLUG*: BS 1363A CABLE*: HP 8120-1703</p> <p>240 V OPERATION</p> |  <p>PLUG*: NZSS 198/AS C112 CABLE*: HP 8120-0696</p> <p>240 V OPERATION</p> |
|  <p>PLUG*: CEE7-V11 CABLE*: HP 8120-1692</p> <p>240 V OPERATION</p> |  <p>PLUG*: NEMA 5-15P CABLE*: HP 8120-1521</p> <p>120 V-6A**</p> |
|  <p>PLUG*: NEMA 5-15P CABLE*: HP 8120-0698</p> <p>240 V - 6A**</p> |  <p>PLUG*: CEE7-V11 CABLE*: HP 8120-1692</p> <p>240 V OPERATION</p> |
|  <p>PLUG*: SEV 1011.1959-24507 TYPE 12 CABLE*: HP 8120-2104</p> <p>240 V OPERATION</p> |  <p>PLUG*: DHCR 107 CABLE*: HP 8120-2956</p> <p>240 V OPERATION</p> |

*The number shown for the plug is the industry identifier for the plug only.
The number shown for the cable is an HP part number for a complete cable including the plug.
**UL listed for use in the United States of America.

Figure 1-2 Accessories Supplied with the HP 3562A

Table 1-1 Manual Section Descriptions

| SECTION | TITLE | DESCRIPTION |
|---------|----------------------|---|
| I | GENERAL INFORMATION | This section contains information on how to use this manual. Also included are Safety Considerations, Recommended Test Equipment and the HP 3562A Performance Specifications. |
| II | PERFORMANCE TESTS | This section contains the Operational Verification and the Performance Tests. Use the operational verification for incoming and after-repair inspections. Use the performance tests to verify that the HP 3562A conforms to its published specifications. |
| III | ADJUSTMENTS | This section describes the adjustment procedures which will return the instrument to peak operating condition. Use this section when adjustment is recommended in Sections II and VIII. |
| IV | REPLACEABLE PARTS | This section lists the replaceable parts in order of their reference designators. Ordering information is also included. |
| V | BACKDATING | This section lists the information required to adapt this service manual to instruments manufactured prior to the printing of this manual. |
| VI | CIRCUIT DESCRIPTIONS | This section contains the HP 3562A theory of operation, the signal name descriptions, and circuit board block diagrams. Use this section to understand how the HP 3562A's circuits function. |
| VII | FAULT ISOLATION | This section contains the information required to isolate failures to the circuit board level. Diagnostic pass and fail messages are found in this section. Use this section to start troubleshooting the HP 3562A. |
| VIII | SERVICE | This section contains all the information required to isolate failures to the component level. The information is listed in order of the circuit board assembly number, A1 through A35. Use this section after the faulty assembly has been identified. |
| IX | SCHEMATICS | This section contains circuit board schematics, component locators, and the instrument block diagram. Use this section with Sections VII and VIII. |

1-3 ACCESSORIES

The following accessories are supplied with the HP 3562A:

| | |
|------------------------------|----------------|
| Line Power Cord | See figure 1-2 |
| Operating Manual | HP 03562-90000 |
| Programming Manual | HP 03562-90030 |
| Service Manual | HP 03562-90010 |
| Display Service Manual | HP 01345-90916 |

The following accessories are available:

| | |
|--------------------|--------------|
| Transit Case | HP 9211-2663 |
|--------------------|--------------|

1-4 INSTRUMENT DESCRIPTION

The HP 3562A is a dual-channel, FFT-based network, spectrum and waveform analyzer which provides analysis capabilities in both the time and frequency domains. The 0-to-100 kHz frequency range, 150 dB measurement range and 80 dB dynamic range of the HP 3562A make it a powerful tool for testing and analysis in electronic, mechanical and servo control system applications.

This analyzer has a pair of differential input channels and a built-in signal source. Besides linear and logarithmic resolution measurement modes, the HP 3562A also provides swept sine measurements.

The digital section of this instrument provides the flexibility to manipulate the gathered data into almost any format required through waveform math, frequency response synthesis, and curve fitting routines. The HP 3562A also directly drives HP-GL plotters without a controller. External disc drives can be directly driven for data and instrument state storage.

1-5 OPTIONS

There are five options available for the HP 3562A. They are available either when the instrument is ordered, or they may be installed later. These options are listed in table 1-2.

Table 1-2 HP 3562A Options

| Option | Description |
|--------|---------------------------------|
| 907 | Front Handle Kit |
| 908 | Rack Mount Kit |
| 909 | Rack Mount and Front Handle Kit |
| 910 | Extra Operating Manuals (1 set) |
| 914 | Delete Service Manual |

1-6 SAFETY CONSIDERATIONS

The HP 3562A is a Safety Class 1 instrument (provided with a protective earth terminal). Although this instrument has been designed in accordance with international safety standards, this manual contains information, cautions and warnings which must be followed to ensure safe operation and retain the HP 3562A in safe operating condition. Service and adjustments should be performed only by qualified personnel who are aware of the hazards involved.

1-7 GROUNDING

On the HP-IB connector pin 12 and pins 18 through 24 are tied to protective earth ground and the HP-IB cable shield. The instrument frame, chassis, covers and all exposed metal surfaces are connected to protective earth ground. The input terminal outer BNC conductor is NOT connected to protective earth ground, and can be raised to a maximum of 42 Vpk with respect to instrument chassis.

WARNING

DO NOT interrupt the protective earth ground or "float" the HP 3562A. This action could expose the operator to potentially hazardous voltages.

1-8 OPERATOR MAINTENANCE

Operator maintenance is limited to replacing the line fuse (MP205) and cleaning the fan filter. There are no operator controls or user serviceable parts inside the HP 3562A. Only trained service personnel should perform instrument repairs.

WARNING

To avoid serious injury, disconnect the ac line power cord before removing or installing the ac line fuse.

Voltage settings

There are two voltage settings on the rear panel of the HP 3562A. Before connecting the line power cord or turning on the instrument, verify the voltage selector switch is in the correct position for the input line voltage.

WARNING

Only a fuse (MP205) with the required rated current and specified type should be used for replacement. The use of repaired fuses and short circuiting of fuse holders is not permitted. Whenever it is likely that the protection offered by the fuse has been impaired, the HP 3562A must be made inoperative and secured against unintended operation.

WARNING

Under no circumstances should an operator remove any covers, screws, or in any other way enter the HP 3562A. There are no operator controls inside the HP 3562A.

How to clean air filter

The cooling fan's air filter is located on the rear panel. To service the filter, remove the power cable and remove the four knurled nuts that hold the filter to the rear panel. Clean the filter using a solution of warm water and a mild soap or replace the filter. The air filter should be cleaned every 30 days.

Cleaning Solvents

Unplug the instrument power cord before cleaning any portion of the instrument. Use only non-abrasive, non-corrosive cleansers. A solution of warm water and mild soap is recommended.

1-9 SPECIFICATIONS

The 3562A specifications are listed in table 1-3. These specifications describe the instrument's warranted performance. Supplemental characteristics are intended to provide information useful in applying the instrument by giving typical, but non-warranted, performance specifications. Supplemental characteristics are denoted as "typical," "nominal", or "approximately".

Table 1-3 Specifications

FREQUENCY

Measurement Range: 64 μ Hz to 100 kHz, both channels single or dual channel operation.

Accuracy: \pm 0.004% of frequency reading

Resolution: Span/800, both channels, single or dual channel operation.

| Spans: | Baseband | Zoom |
|-------------------|-----------|-----------|
| # of spans | 66 | 65 |
| Minimum span | 10.24 mHz | 20.48 mHz |
| Maximum span | 100 kHz | 100 kHz |
| Time record (Sec) | 800/Span | 800/Span |

Window Functions: Hanning, flat top, uniform, force, exponential, and user-defined.

| Window Parameters: | Flat Top | Hanning | Uniform |
|-------------------------------------|----------|---------|---------|
| Noise Equiv BW (% of span) | 0.478 | 0.188 | 0.125 |
| 3 dB BW (% of span) | 0.45 | 0.185 | 0.125 |
| Shape Factor (60 dB BW/ 3 dB BW) | 2.6 | 9.1 | 716 |

Typical Real Time Bandwidth:

| | |
|--------------------------------|---------|
| Single channel, single display | 2.5 kHz |
| Single channel, fast averaging | 10 kHz |
| Dual channel, single display | 2 kHz |
| Dual channel, fast averaging | 5 kHz |
| Throughput to CS/80 disc | |
| Single channel | 10 kHz |
| Dual channel | 5 kHz |

Table 1-3 Specifications cont.

AMPLITUDE

Accuracy: Defined as full-scale accuracy at any of the 801 calculated frequency points. Overall accuracy is the sum of absolute accuracy, window flatness and noise level.

Absolute Accuracy:

Single channel (Channel 1 or Channel 2)

± 0.15 dB $\pm 0.015\%$ of input range (+27 dBV to -40 dBV, input connections as specified in Cases 1 and 2 in figure 1-3)

± 0.25 dB $\pm 0.025\%$ of input range (-41 dBV to -51 dBV, input connections as specified in Cases 1 and 2 in figure 1-3)

DC Response: Auto-Cal on

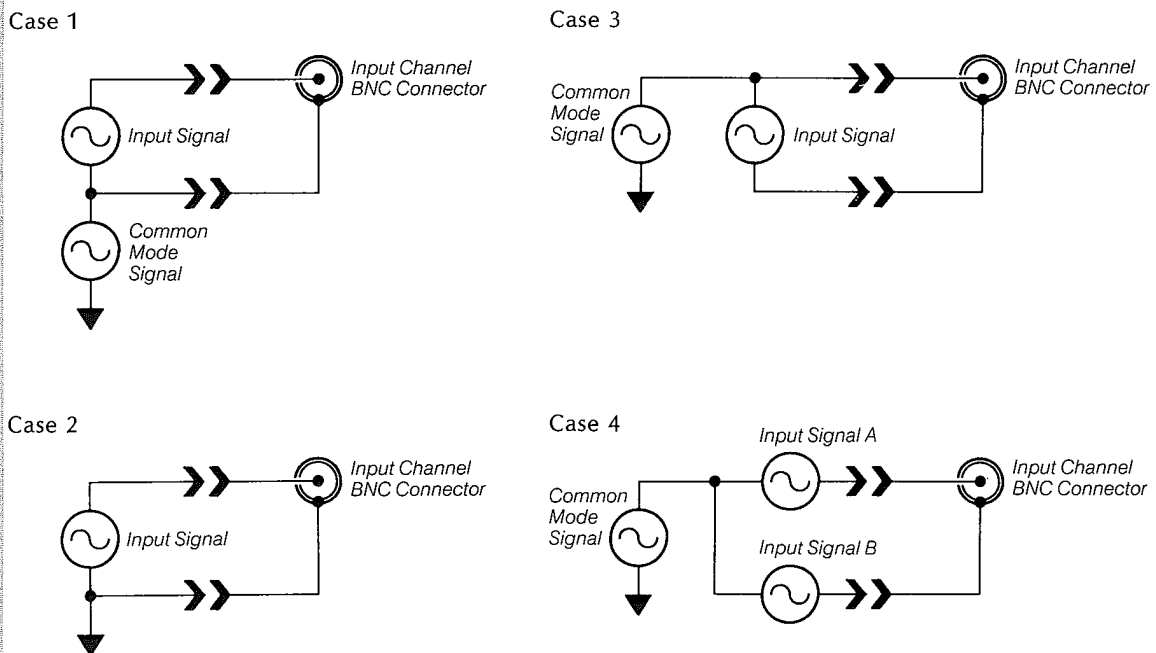
| | |
|----------------------|-------------------------|
| Input Range (dBVrms) | DC Level |
| +27 to -35 | >30 dB below full scale |
| -36 to -51 | >20 dB below full scale |

Frequency Response Channel Match:

± 0.1 dB, $\pm 0.5^\circ$ (input connections as specified in Cases 1 and 2 in figure 1-3)

Input Connections:

Cases 1 and 2 are the recommended input connections.



Cases 3 and 4 are input connections which degrade amplitude accuracy. For these cases, the amplitude accuracy previously specified must be modified with the accuracy adders. (See next paragraph)

Figure 1-3 Input Connections

Table 1-3

Specifications cont.

Accuracy Adder: Single channel, inputs connected as shown in Cases 3 and 4 in figure 1-3. Add ± 0.35 dB and $\pm 4.0^\circ$ to the absolute accuracy.

Accuracy Adder: Dual channel measurements Add ± 0.35 dB and $\pm 4.0^\circ$ once for each input connected as shown in Cases 3 and 4 in figure 1-3.

Window Flatness:

| | |
|-----------|--------------|
| Flat Top: | +0, -0.01 dB |
| Hanning: | +0, -1.5 dB |
| Uniform: | +0, -4.0 dB |

Noise Floor: Flat top window, 50Ω source impedance. -51 dBV range

20 Hz to 1 kHz (1 kHz span) < -126 dBV (< -134 dBV/ $\sqrt{\text{Hz}}$)

1 kHz to 100 kHz (100 kHz span) < -116 dBV (< -144 dBV/ $\sqrt{\text{Hz}}$)

Dynamic Range: All distortion (intermodulation and harmonic), spurious and alias products ≥ 80 dB below full scale input range (16 averages < 10 k Ω termination).

PHASE

Accuracy: Single Channel, input connections as specified in Cases 1 and 2 in figure 1-3.

| | |
|-------------------|------------|
| < 10 kHz | \pm |
| | 2. |
| | 5° |
| 10 kHz to 100 kHz | \pm |
| | 12 |
| | $.0^\circ$ |

INPUTS

Input impedance: $1\text{ M}\Omega \pm 5\%$ shunted by < 100 pF.

Input Coupling: The inputs may be ac or dc coupled; ac rolloff is < 3 dB at 1 Hz.

Crosstalk: < -140 dB (50Ω source, 50Ω input termination, input connectors shielded)

Common Mode Rejection:

| | |
|-----------------|----------|
| 0 Hz to 66 Hz | 80 dB |
| 66 Hz to 500 Hz | 65 dB |

Common Mode Voltage: dc to 500 Hz

| Input Range (dBV rms) | Maximum (ac + dc) |
|-----------------------|-------------------|
| +27 to -12 | ± 42.0 Vpk |
| -13 to -51 | ± 18.0 Vpk* |

*For the -43 to -51 dBV input ranges, common mode signal levels cannot exceed ± 18 Vpk or (Input Range) + (Common Mode Rejection), whichever is the lesser level.

Common Mode Voltage: 500 Hz to 100 kHz. The ac part of the signal is limited to 42 Vpk or (Input Range) + (10 dB), whichever is the lesser level.

Table 1-3

Specifications cont.

Common Mode Distortion: For the levels specified, distortion of common mode signals will be less than the level of the rejected common mode signal.

External Trigger Input Impedance: typically 50 kΩ ± 5%

External Sampling Input: TTL compatible input for signals ≤ 256 kHz (maximum sample rate).

External Reference Input:

Input Frequencies: 1,2,5 or 10 MHz ± 0.01%

Amplitude Range: 0 dBm to + 20 dBm (50Ω)

TRIGGER

Trigger Modes: Free run, input channel 1, input channel 2, and external trigger. Free run applies to all measurement modes. Input channel 1, input channel 2 and external trigger apply to the linear resolution mode, time capture mode, and time throughput measurements.

Trigger Conditions:

Free Run: A new measurement is initiated by the completion the previous measurement.

Input: A new measurement is initiated when the input signal to either Channel 1 or Channel 2 meets the specified trigger conditions, trigger level range is ± 100% of full scale input range; trigger level is user selectable in steps of (Input Range in volts)/128.

Source: Measurements are synchronized with the periodic signal types (burst random, sine chirp, and burst chirp).

External: A new measurement is initiated by a signal applied to the front panel Ext Trigger input. Trigger level range is ± 10 Vpk; trigger level is user selectable in 80 mV steps.

Trigger Delay:

Pre-Trigger: The measurement can be based on data from 1 to 4095 samples in baseband and from 1 to 4094 samples in zoom prior to trigger conditions being met. Resolution is 1 sample (1/2048 of a time record).

Post-Trigger: The measurement is initiated from 1 to 65,536 samples (1/2048 to 32 time records) after the trigger conditions are met. Resolution is 1 sample (1/2048 of a time record).

SOURCE

Band limited, band translated random noise, burst random, sine chirp, burst chirp, as well as fixed sine and swept sine signals are available from the front panel source output. DC Offset is also user-selectable.

Output Impedance: 50Ω Nominal

Output Level: Between -10Vpk and +10 Vpk (ac + dc) into a load ≥ 10 kΩ, < 1000 pF. Maximum current = 20 mA.

AC Level: ± 5 Vpk (≥ 10 kΩ, < 1000 pF load)

DC Offset: ± 10 Vpk in 100 mV steps. Residual offset at 0V offset ≤ 10 mV.

% In-Band Energy: (1 kHz span, 5 kHz center frequency)

Random Noise: 70%

Sine Chirp: 85%

Accuracy and Purity: Fixed or Swept Sine

Flatness: ± 1 dB from 0 to 65 kHz

+ 1 dB, - 1.5 dB from 65 kHz to 100 kHz

Distortion: (including subharmonics)

dc to 10 kHz - 60 dB

10 kHz to 100 kHz - 40 dB

Table 1-3 Specifications cont.

| GENERAL | |
|--|---|
| Specifications apply when AUTO CAL is enabled, or within 5° C and 2 hours of last internal calibration. | |
| Ambient Temperature: 0 to 55 °C. Relative Humidity: ≤95% at 40 °C. Altitude: ≤4,572m (15,000 ft). | |
| Storage: Temperature: -40 to +75 °C. Altitude: ≤15,240m (50,000 ft). | Weight: 26 kg (56 lbs) net 35 kg (77 lbs) shipping |
| Power: 115 Vac +10%, -25%, 48 to 440 Hz 230 Vac +10%, -15%, 48 to 66 Hz 450 VA maximum | Dimensions: 222 mm (8.75 in) high 426 mm (16.25 in) wide 578 mm (22.75 in) deep |
| HP-IB: Implementation of IEEE Std 488-1978 SH1 AH1 T5 TE0 L4 LE0 SR1 RL1 PP0 DC1 DT1 C0 Supports the 91XX and 794X families of HP disc drives as well as Hewlett-Packard Graphics Language (HP-GL) digital plotters. | |

1-10 RECOMMENDED TEST EQUIPMENT

The equipment required to maintain the HP 3562A is listed in table 1-4. Other equipment may be substituted for the recommended model if it meets or exceeds the listed critical specifications. When substitutions are made, the user may have to modify the performance and adjustment procedures to accommodate the different operating characteristics.

| Resistance | Tolerance | Power | -hp- Part Number |
|------------|-----------|--------|------------------|
| 1 k Ω | 1% | 0.25 W | 0757-0280 |
| 100 k Ω | 1% | 0.25 W | 0757-0465 |

Assembly

1. Cut resistor leads to 12mm on each end.
2. Solder one resistor lead to the center conductor of the BNC FEMALE connector.
3. Solder the CONDUCTOR CENTER PIN to the other lead of the resistor.
4. Screw the SLEEVE and the BNC MALE connector into place. Tighten securely.

Figure 1-4 Constructing a Feedthrough

Table 1-4 Recommended Test Equipment

| Instrument | Critical Specifications | Recommended Model | Use* |
|----------------------------------|--|--|-------|
| AC Calibrator | 10 Hz to 100 kHz; 1 mV to 10V Amplitude Accuracy: $\pm 0.1\%$ | Fluke 5200A Alternative HP 745A Datron 4200 | P,O |
| Frequency Synthesizer (2) | Frequency Range: 1 Hz to 100 kHz Frequency Accuracy: 10 ppm Amplitude Range: 40 Vp-p Amplitude Accuracy: 0.2 dB from 1 Hz to 100 kHz 1 dB from 100 kHz to 1 MHz | HP 3325A Opt 001 Opt 002 Alternative (1) HP 3326A Opt 002 | P,O |
| Digital Voltmeter | 5½ digit AC Voltage: 30 Hz to 100 kHz; 0.1 to 500V; $\pm 0.1\%$; 1 M Ω input impedance dc Voltage: 1V to 1000V; $\pm 0.1\%$ | HP 3456A | P,T,F |
| Low Distortion Oscillator | Frequency Range: 1 Hz to 100 kHz Amplitude Range: 0.1 V to 1 Vrms Distortion: ≤ -80 dB (0.01%) | HP 339A Alternative HP 3326A | P |
| Oscilloscope | Bandwidth: >50 MHz Two Channel; External Trigger | HP 1980B Alternative HP 1740 | A,T,F |
| Signature Analyzer | Maximum Clock: >25 MHz Clock Set up Time: <20 ns | HP 5006A Alternative HP 5005A HP 5005B | T |
| Variable AC Power Supply | Voltage Range: 80 to 120 Vac Frequency Range: 60 Hz Voltage Accuracy: $\pm 2\%$ | ** | T |
| Triple Output DC Power Supply | Voltage Range: +15 to -15 Vdc, 0 to +6 Vdc Power: 13 watts | HP 6235A Alternative: HP 6236A | T |
| Counter | Frequency Range: 0 Hz to 100 MHz External Frequency Standard Input: 10 MHz 10 MHz | HP 5335A Alternative: HP 5238B Opt 010 | A |

* P = Performance Tests, A = Adjustments, O = Operational Verification, F = Fault Isolation, T = Troubleshooting

** No specific model number is recommended, any variable AC power supply which meets the listed critical specifications may be used.

Table 1-4 Recommended Test Equipment cont.

| Instrument | Critical Specifications | Recommended Model | Use* |
|---|---|---|--------------|
| Probe, Oscilloscope | Impedance: 10 M Ω Division Ratio: 10:1 Maximum Voltage: 500 Vdc | HP 10014A Alternatives: HP 10016B HP 10004A HP 10005D | A,F, T |
| HP 3562A Service Kit | Digital Extender Brd (HP 03562-66540) Analog Extender Brd (HP 03562-66541) Input/Analog Ext Brd (HP 03562-66542) Common Mode Cable (HP 03562-61620) Input Extender Cable (HP 03562-61621) SMB to BNC adapter cable (HP 03585-61616) | HP 03562-84401 | P,A,O F,T |
| Feedthrough Terminations (2) (1) | 50 Ω : \pm 1% at dc 600 Ω : \pm 1% at dc | HP 11048C Alternative: HP 10100C HP 11095A | P,O |
| Cables (2) | BNC to BNC: length \leq 30 cm | HP 8120-1838 Alternative: HP 11170A | P,O |
| Adapters | BNC female to Banana male BNC (f) to dual banana male BNC Tee (m)(f)(f) | Pomona Elect. Model 1296 HP 1251-2277 HP 1250-0781 | P,O |
| Resistors (2) (1) | Value 1 k Ω Accuracy: 1% Power: 0.25W Value: 100 k Ω Accuracy: 1% Power: 0.25W | HP 0757-0280 HP 0757-0465 | P |

* P = Performance Tests, A = Adjustments, O = Operational Verification,
F = Fault Isolation, T = Troubleshooting

SECTION II

PERFORMANCE TESTS

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SECTION II

PERFORMANCE TESTS

2-1 INTRODUCTION

This section contains the operational verification and the performance tests. The operational verification provides a high level of confidence regarding instrument operation and should be used for incoming and after-repair inspections. The completion of all the performance tests verifies that the HP 3562A conforms to its published specifications. One or more of the performance tests should be done after some repairs. Refer to "Service," Section VIII, for this information.

Note: Tables and figures beginning with "(OV)" are used in the operational verification tests.

2-2 CALIBRATION CYCLE

To verify that the HP 3562A is meeting its published specifications, the performance tests must be done every twelve months.

PART A OPERATIONAL VERIFICATION

2-3 INTRODUCTION

These tests check selected specifications in their worst case conditions to provide a high level of confidence regarding instrument operation. This brief verification procedure should be used for incoming and after-repair inspections. The operational verification takes approximately two hours to complete.

2-4 HOW TO USE PART A

1. Start each operational verification test by setting the test equipment to the preset conditions listed in the "Initial Equipment Setup," paragraph 2-6.
2. There are two types of keys on the HP 3562A, hard keys and soft keys. In this section the hard keys are in bold text, and the soft keys are in regular text.

For example:

FREQ FREQ SPAN **10** kHz

This example instructs you to press the hard key **FREQ** and the soft key FREQ SPAN. After pressing the soft key FREQ SPAN enter 10 kHz.

3. Refer to figure 2-1 for the position of the X and Y marker readings.
4. Record the results of each of the operational verification tests on the "Operation Verification Test Record," paragraph 2-16. This test record may be reproduced without written permission of Hewlett-Packard.
5. If the HP 3562A fails a test, use the "If Test Fails Check:" paragraph at the end of each test.

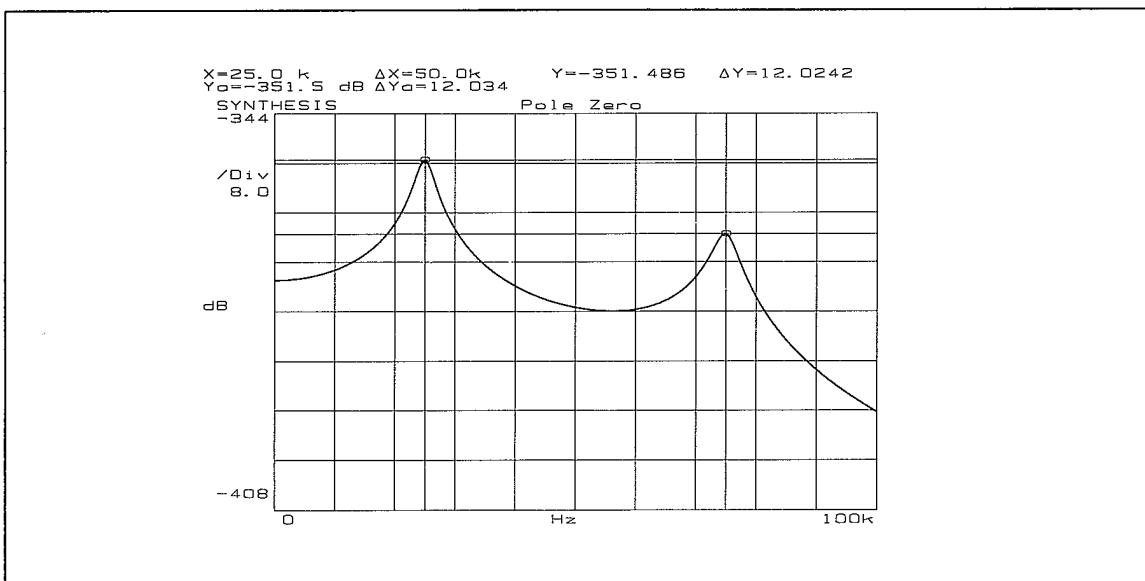


Figure 2-1 (OV) Marker Positions

2-5 REQUIRED TEST EQUIPMENT

The recommended test equipment is listed in table 1-4. If the recommended equipment is not available, a substitute may be used which meets or exceeds the required characteristics given in table 1-4.

2-6 INITIAL EQUIPMENT SETUP

When the recommended test equipment of table 1-4 is used to complete the operational verification, the instruments listed below must be set to the preset conditions listed before beginning the test. In each test, any unspecified parameters should be set to the following conditions:

HP 3325A frequency synthesizer

| | | |
|------------|------|---------------|
| Function | | SINE WAVE (~) |
| Frequency | | 1 kHz |
| Amplitude | | 1 mVrms |
| Phase | | 0 Degrees |
| dc Offset | | 0V |
| Modulation | | OFF |
| Sweep | | OFF |

Fluke 5200 ac calibrator

| | | |
|-----------------|------|----------|
| Frequency | | 1 kHz |
| Amplitude | | .01 Vrms |
| Voltage Error % | | OFF |
| Vernier | | 0 |
| Mode | | OPER |
| Control | | LOCAL |
| Phase Lock | | OFF |
| Sense | | INTERNAL |

2-7 SELF TEST

This test determines if the HP 3562A is operating correctly. No tests should be attempted until the instrument passes this test.

Required Test Equipment

None

Procedure

1. Press the HP 3562A keys as follows:

SPCL FCTN SELF TEST

2. This test takes about 0.5 minutes to complete.
3. When "SELF TEST PASSES" is displayed in the lower right corner of the display, check PASS on the Operational Verification Test Record.

If Test Fails:

Go to "Fault Isolation Section", Section VII.

2-8 DC OFFSET

This test measures the level of the dc offset generated with auto cal on.

Required Test Equipment

- (2) 50 Ω feedthrough terminations HP 11048C

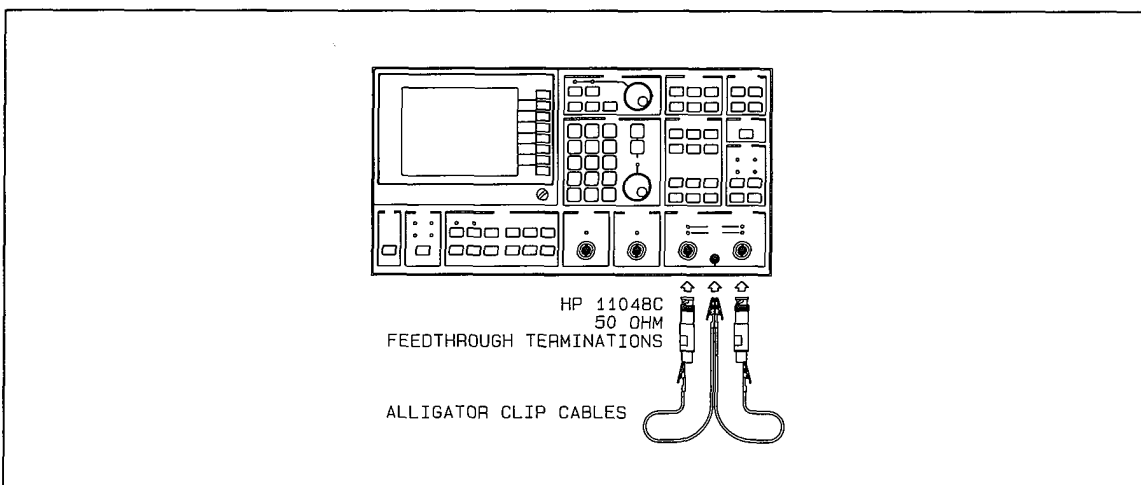


Figure 2-2 (OV) DC Offset Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-2. Keep the leads to chassis ground as short as possible.
- B. Press the HP 3562A keys as follows:

| | | | | |
|------------------|-------|--------------------|-------|--------------|
| PRESET | | RESET | | |
| CAL | | AUTO ON | | |
| | | SINGLE CAL | | |
| WINDOW | | UNIFORM | | |
| AVG | | 2 | | ENTER |
| | | STABLE | | |
| FREQ | | 1 kHz | | |
| UNITS | | P SPEC UNITS | | VOLTS RMS |
| | | | | VOLTS |
| A & B | | | | |
| X | | X VALUE | | 0 Hz |
| RANGE | | - 51 dBVrms | | |
| START | | | | |

- C. Record the Ya marker reading on the Operational Verification Test Record for the CHAN 1 measured value.
- D. Record the Yb marker reading on the Operational Verification Test Record for CHAN 2 measured value.

If Test Fails Check:

| | |
|---------------------------------|---|
| Adjustments Section III | Track and Hold Offset Adjustment Input DC Offset Adjustment |
| Troubleshooting Section VIII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards |

2-9 AMPLITUDE ACCURACY and FLATNESS

This test measures the amplitude accuracy and flatness of the HP 3562A using the amplitude reference of the ac calibrator.

Required Test Equipment

- Frequency Synthesizer HP 3325A
- AC Calibrator Fluke 5200A

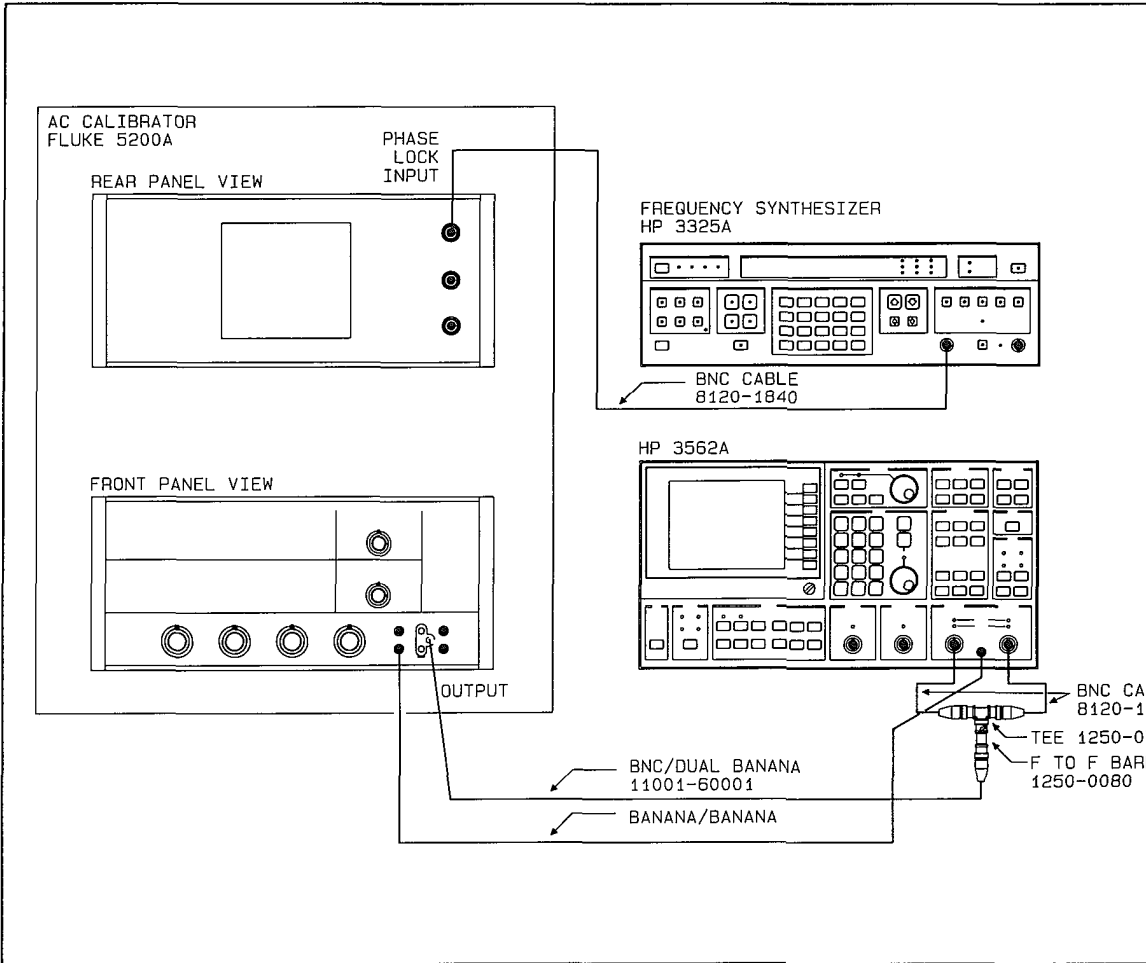


Figure 2-3(OV) Amplitude Accuracy and Flatness Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-3 . Refer to "Initial Equipment Setup," section 2-6, for unspecified parameters.
- B. Set the test instruments initially as follows:

Frequency Synthesizer

Amplitude 1 Vrms
 Frequency 1 kHz
 Function Sine Wave

AC Calibrator

Phase Lock ON
 Sense INTERNAL
 Mode OPER
 Frequency 1 kHz
 Amplitude 2.7698 Vrms

- C. Press the HP 3562A keys as follows:

PRESET RESET

CAL SINGLE
 CAL

WINDOW FLAT TOP

AVG 4 ENTER
 STABLE

UNITS P SPEC VOLTS
 UNITS RMS
 VOLTS

A & B

Table 2-1 (OV) Amplitude Accuracy and Flatness

| HP 3562A Range Setting | Signal Frequency | ac Calibrator Amplitude | Specification | |
|------------------------------|---------------------|----------------------------|---------------|-------------|
| | | | Lower Limit | Upper Limit |
| 9 dBVrms | 1 kHz | 2.8184 Vrms | 8.849 dBV | 9.151 dBV |
| 9 dBVrms | 99 kHz | 2.8184 Vrms | 8.849 dBV | 9.151 dBV |
| 0 dBVrms | 1 kHz | 1.0000 Vrms | -.1513 dBV | .1513 dBV |
| 0 dBVrms | 99 kHz | 1.0000 Vrms | -.1513 dBV | .1513 dBV |
| -13 dBVrms | 1 kHz | .22387 Vrms | -13.15 dBV | -12.85 dBV |
| -13 dBVrms | 99 kHz | .22387 Vrms | -13.15 dBV | -12.85 dBV |

D. For each of the frequencies listed in table 2-1 perform steps 1 through 7:

1. Press the HP 3562A keys as follows:

RANGE To range setting in table

FREQ CENTER FREQ To signal frequency
in table

2. Set the ac calibrator to the signal frequency.

3. Set the frequency synthesizer to the signal frequency.

4. Set the ac calibrator's amplitude.

5. Press the HP 3562A keys as follows:

START

SPCL
MARKER **MRKR** →
PEAK

6. Record the Ya marker reading on the Operational Verification Test Record for CHAN 1.

7. Record the Yb marker reading on the Operational Verification Test Record for CHAN 2.

If Test Fails Check:

| | |
|-------------|-------------------------------------|
| Adjustments | 2nd Pass Gain Adjustment |
| Section III | ADC Offset and Reference Adjustment |
| | Input Flatness Adjustment |
| | Input Attenuator Adjustments |
| | Calibrator Adjustment |

| | |
|-----------------|--|
| Troubleshooting | A33, A35 Input Boards |
| Section VII | A32, A34 Analog Digital Converter Boards |
| | A30 Analog Source Board |

2-10 AMPLITUDE AND PHASE MATCH

This test determines if the HP 3562A's amplitude and phase match between channel 1 and channel 2 are within the specified limits.

Required Test Equipment

BNC Tee HP 1250-0781

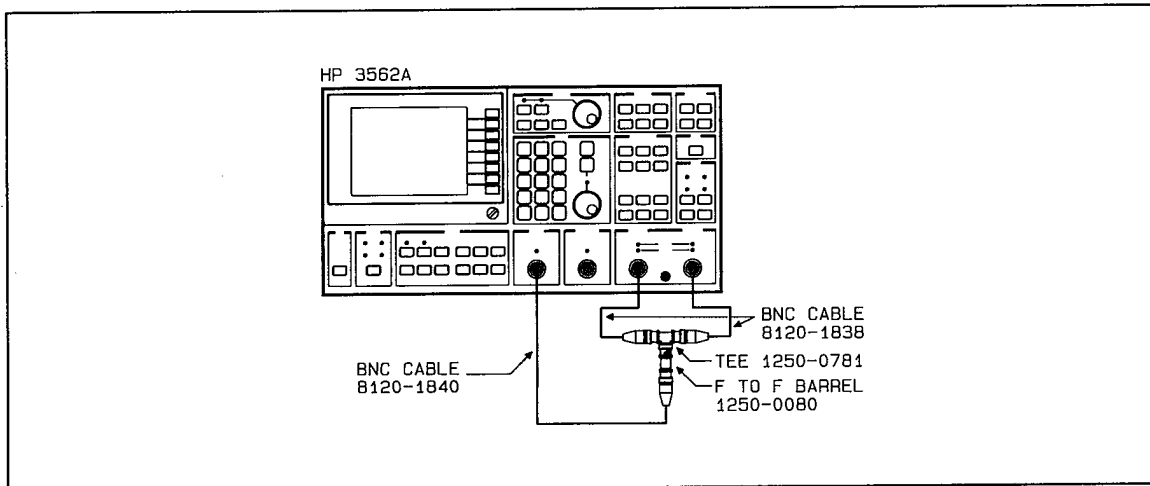


Figure 2-4 (OV) Amplitude and Phase Match Test Setup

Procedure

- A. Connect the HP 3562A as shown in figure 2-4. The cables to channel 1 and channel 2 must be the same length.
- B. Press the HP 3562A keys as follows:

| | | |
|-------------------------|-------|-----------------|
| PRESET | | RESET |
| CAL | | SINGLE CAL |
| INPUT COUPLE | | CHAN1 AC |
| | | CHAN2 AC |
| | | GROUND CHAN1 |
| | | GROUND CHAN2 |

```

SELECT
TRIG      . . . .  0 V
              . . . .  SOURCE TRIG

WINDOW   . . . .  UNIFRM

AVG       . . . .  16      . . . .  ENTER
              . . . .  STABLE

SOURCE    . . . .  PRIODC
              . . . .  CHIRP

MEAS
DISP     . . . .  FREQ RESP

SCALE     . . . .  X FIXD
              . . . .  SCALE      . . . .  .375, 100 kHz
    
```

C. Perform steps 1 through 6:

1. Press the HP 3562A keys as follows:

```

RANGE     . . . .  -47 dBVrms

SOURCE    . . . .  SOURCE LEVEL . . . .  -49 dBVrms

SCALE     . . . .  Y FIXD
              . . . .  SCALE      . . . .  -.2, .2 dB

START

Y         . . . .  -.1, .1 dB
    
```

2. If the measurement is within the marker band, check PASS on the Operation Verification Test Record for part 1.

3. Press the HP 3562A keys as follows:

```

RANGE     . . . .  0 dBVrms

SOURCE    . . . .  SOURCE LEVEL. . . .  0 dBVrms

START

Y         . . . .  -.1,.1 dB
    
```

4. If the measurement is within the marker band, check PASS on the Operation Verification Test Record for part 2.

5. Press the HP 3562A keys as follows:

RANGE **10** dBVrms
SOURCE SOURCE LEVEL **10** dBVrms
START
Y **-.1,.1** dB

6. If the measurement is within the marker band, check PASS on the Operation Verification Test Record for part 3.

D. Perform steps 1 through 6:

1. Press the HP 3562A keys as follows:

RANGE **-47** dBVrms
SOURCE SOURCE LEVEL **-49** dBVrms
COORD PHASE
START
SCALE Y FIXD
SCALE **-1, 1** Degree
Y Y VALUE **-.5, .5** Degree

2. If the measurement is within the marker band, check PASS on the Operation Verification Test Record for part 4.

3. Press the HP 3562A keys as follows:

RANGE **0** dBVrms
SOURCE SOURCE LEVEL **0** dBVrms
START
Y Y VALUE **-.5,.5** Degree

4. If the measurement is within the marker band, check PASS on the Operation Verification Test Record for part 5.

5. Press the HP 3562A keys as follows:

RANGE **10 dBVrms**

SOURCE **SOURCE LEVEL** **10 dBVrms**

START

Y **Y VALUE** **-.5, .5 Degree**

6. If the measurement is within the marker band, check PASS on the Operation Verification Test Record for part 6.

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments Section III | 2nd Pass Gain Adjustment ADC Offset and Reference Adjustment Input Flatness Adjustment Input Attenuator Adjustments Calibrator Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards A30 Analog Source Board |

2-11 FREQUENCY ACCURACY

This test measures the frequency accuracy of the HP 3562A.

Required Test Equipment

Frequency Synthesizer HP 3325A
 50Ω feedthrough termination HP 11048C

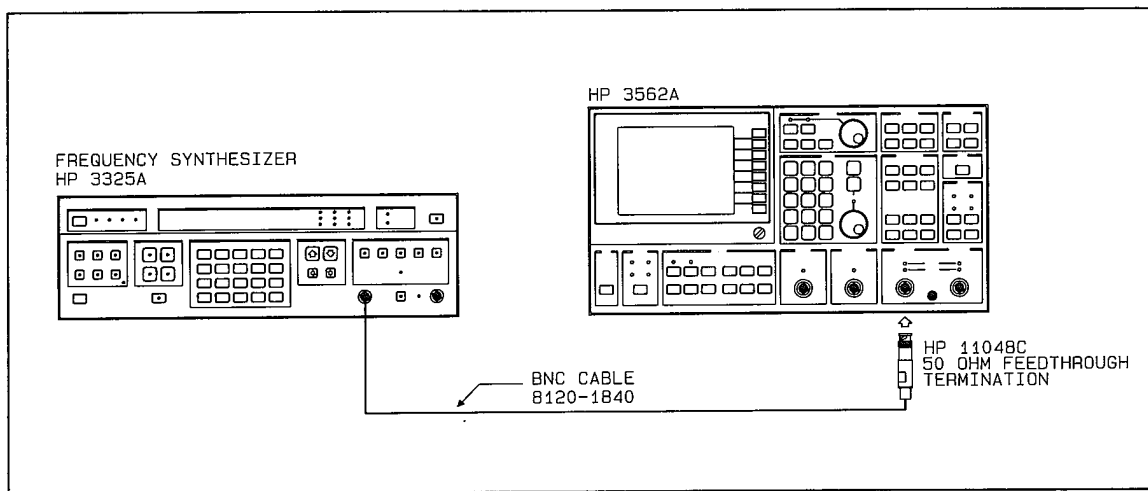


Figure 2-5 (OV) Frequency Accuracy Test Setup

Procedure

- A. Connect the test equipment as shown in figure 2-5. Refer to "Initial Equipment Setup," section 2-6, for unspecified parameters.
- B. Set the test instruments initially as follows:

Frequency Synthesizer

| | | |
|-----------|------|-----------|
| Frequency | | 99 kHz |
| Amplitude | | 1 Vrms |
| Function | | Sine Wave |

- C. Press the HP 3562A keys as follows:

| | | |
|---------------|------|--------------------------------|
| PRESET | | RESET |
| CAL | | SINGLE CAL |
| RANGE | | 0 dBVrms |
| FREQ | | CENTER FREQ 99 kHz |
| AVG | | 2 ENTER |
| | | STABLE |

START

X

- D. Record the X marker reading as the measured value on the Operational Verification Test Record.

If Test Fails Check:

| | |
|----------------------------|--------------------------------|
| Adjustments Section III | 20.48 MHz Reference Adjustment |
|----------------------------|--------------------------------|

| | |
|--------------------------------|-------------------|
| Troubleshooting Section VII | A31 Trigger Board |
|--------------------------------|-------------------|

2-12 COMMON MODE REJECTION

This test measures the capability of the 3562A to ignore a signal which appears simultaneously and in phase at the high and low input of a single channel.

Required Test Equipment

- Frequency Synthesizer HP 3325A
- Common Mode Cable HP 03562-61620

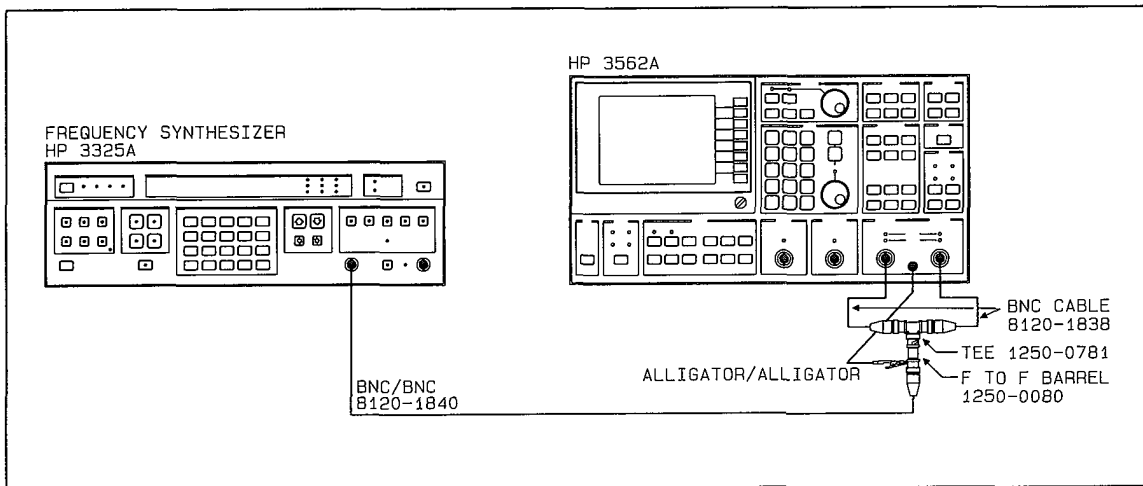


Figure 2-6 (OV) Common Mode Rejection Test Setup #1

Procedure

- A. Connect the test instruments as shown in figure 2-6. Refer to "Initial Equipment Setup", paragraph 2-6, for unspecified parameters.
- B. Set the frequency synthesizer as follows:

Function Sine Wave
 High Voltage
 Output ON

- C. Press the HP 3562A keys as follows:

PRESET RESET

CAL SINGLE
 CAL

AVG **16** ENTER

. STABLE

WINDOW FLAT TOP

A & B

UNITS P SPEC VOLTS
 UNITS RMS

. VOLTS

Table 2-2 (OV) Common Mode Rejection

| Signal Amplitude | Signal Frequency | Range Setting #1 | Range Setting #2 | Specification |
|------------------|------------------|------------------|------------------|---------------|
| 5.680 Vrms | 66 Hz | 16 dBVrms | -8 dBVrms | ≤80 dB |
| 3.413 Vrms | 500 Hz | 11 dBVrms | -12 dBVrms | ≤65 dB |

- D. For each of the frequencies listed in table 2-2 perform steps 1 through 9:
 - 1. Set the Frequency Synthesizer as follows:

Amplitude To signal amplitude in table
 Frequency To signal frequency in table

2. Press the HP 3562A keys as follows:

| | | | | |
|------------------------|-------|------------------------------|-------|---------------------------------|
| FREQ | | CENTER FREQ | | To signal frequency in table |
| RANGE | | To range setting #1 in table | | |
| START | | | | |
| SPCL MARKER | | MRKR | → | PEAK |

- Record the Ya marker amplitude reading on the Operation Verification Test Record as the first measurement for CHAN 1.
- Record the Yb marker amplitude reading on the Operation Verification Test Record as the first measurement for CHAN 2.

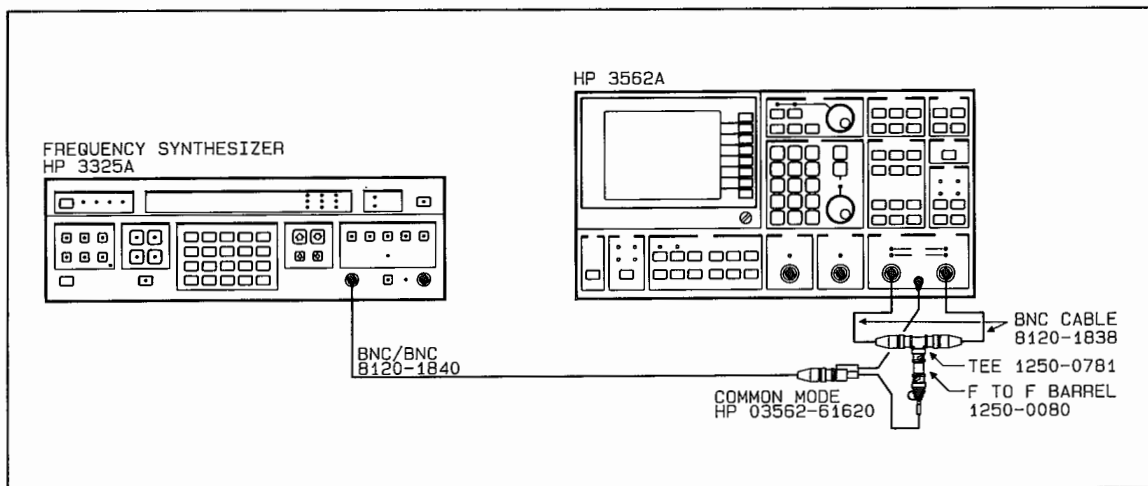


Figure 2-7 (OV) Common Mode Rejection Test Setup #2

5. Connect the test instruments as shown in figure 2-7.
6. Press the HP 3562A keys as follows:

| | | |
|--------------|---------|------------------------------|
| RANGE | | To range setting #2 in table |
| START | | |
| SCALE | | Y AUTO SCALE |
| X | | To signal frequency in table |
7. When the average is complete, record the Ya amplitude reading on the Operation Verification Test Record as the second measurement for CHAN 1.
8. Record the Yb amplitude reading on the Operation Verification Test Record as the second measurement for CHAN 2.
9. Calculate the relative value for both channels:

$$\begin{array}{r} \text{First} \\ \text{Measurement} \end{array} - \begin{array}{r} \text{Second} \\ \text{Measurement} \end{array} = \text{Relative Value}$$

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments Section III | Input dc Offset Adjustment Calibrator Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A30 Analog Source |

2-13 SINGLE CHANNEL PHASE ACCURACY

This test measures the phase accuracy of the HP 3562A relative to the phase of the trigger signal. The frequency synthesizer is used to input a square wave to one channel and the external trigger input.

Required Test Equipment

| | | |
|-----------------------------|---------|--------------|
| Frequency Synthesizer | | HP 3325A |
| 50Ω feedthrough termination | | HP 11048C |
| 2 BNC Tees | | HP 1250-0781 |

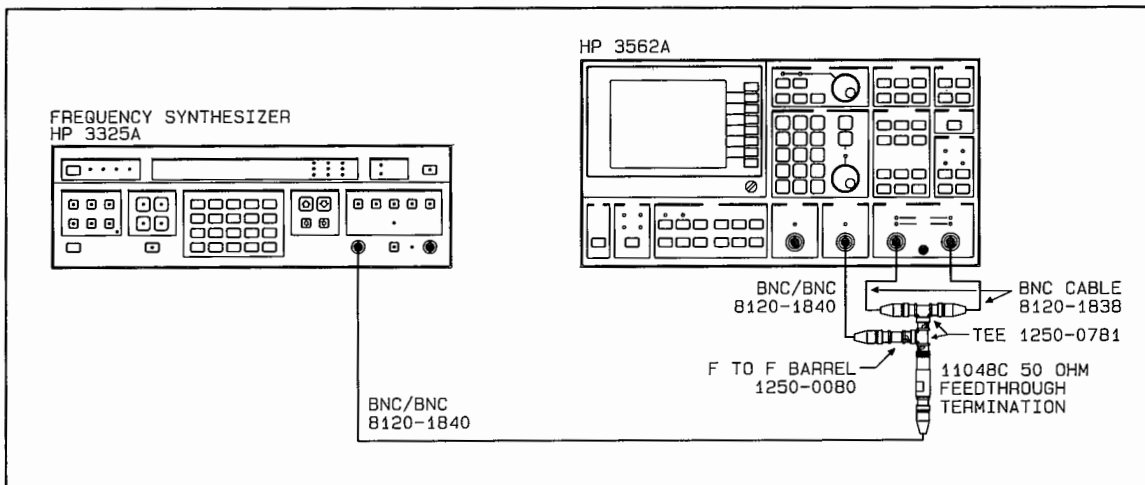


Figure 2-8 (OV) Single Channel Phase Accuracy Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-8. Refer to "Initial Equipment Setup," section 2-6, for unspecified parameters.
- B. Set the test instruments initially as follows:

Frequency Synthesizer

| | | |
|-----------|-------|-------------|
| Frequency | | 9 kHz |
| Amplitude | | 1 Vrms |
| DC Offset | | 0 Vdc |
| Function | | Square Wave |

C. Press the HP 3562A keys as follows:

| | | | |
|------------------------|-------|-----------------|------------------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| SELECT MEAS | | POWER SPEC | |
| AVG | | 5 | ENTER |
| | | STABLE | |
| | | TIM AV ON | |
| WINDOW | | UNIFRM | |
| SELECT TRIG | | 0 V | |
| | | EXT | |
| MEAS DISP | | FILTRD INPUT | AVRG |
| | | | LINEAR SPEC 1 |
| B | | | LINEAR SPEC 2 |
| A & B | | | |
| COORD | | PHASE | |
| START | | | |
| X | | 9 kHz | |

D. Record the Ya marker reading on the Operational Verification Test Record for CHAN 1.

E. Record the Yb marker reading on the Operational Verification Test Record for CHAN 2.

F. Set the frequency Synthesizer as follows:

| | | |
|-----------|-------|--------|
| Frequency | | 99 kHz |
|-----------|-------|--------|

G. Press the HP 3562A keys as follows:

SELECT
TRIG **CHAN1**
INPUT

START

X **99 kHz**

H. Record the Ya marker reading on the Operational Verification Test Record for CHAN 1.

I. Record the Yb marker reading on the Operational Verification Test Record for CHAN 2.

If Test Fails Check:

| | |
|-----------------|--|
| Adjustments | None |
| Troubleshooting | A33, A35 Input Boards |
| Section VII | A32, A34 Analog Digital Converter Boards |
| | A31 Trigger Board |
| | A6 Digital Filter Controller |
| | A1 Digital Source |

2-14 NOISE AND SPURIOUS SIGNAL LEVEL

This test measures the level of the noise floor and any spurious signals generated within the HP 3562A.

Required Test Equipment

(2) 50Ω feedthrough terminations HP 11048C

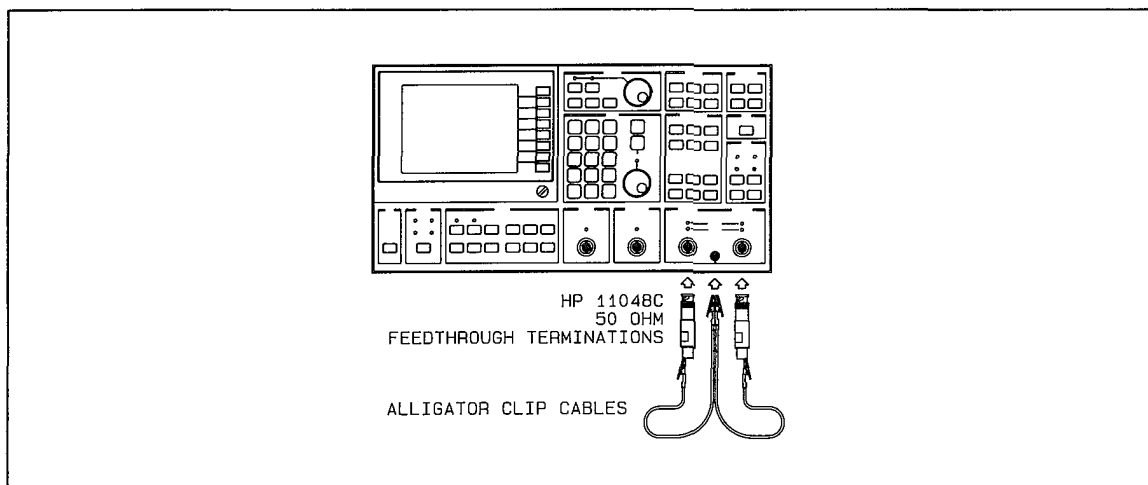


Figure 2-9 (OV) Noise and Spurious Signal Level Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-9. Keep the leads from the feed-through terminations to chassis ground as short as possible.
- B. Press the HP 3562A keys as follows:

| | | | |
|-------------------------|------|-----------------|-------------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| RANGE | | - 51 dBVrms | |
| INPUT COUPLE | | CHAN 1 AC | |
| | | CHAN 2 AC | |
| FREQ | | FREQ SPAN | 1 kHz |
| | | START FREQ | 20 Hz |
| AVG | | 20 | ENTER |
| | | STABLE | |
| WINDOW | | UNIFRM | |
| UNITS | | P SPEC UNITS | VOLTS RMS |
| | | | VOLTS |

- C. Perform steps 1 through 4:

- 1. Press the HP 3562A keys as follows:

| | |
|------------------------|----------------------|
| START | |
| SCALE | Y AUTO SCALE |
| SPCL MARKER | MRKR → PEAK |

- 2. If the Ya marker reading is less than or equal to -131 dBVrms check PASS on the Operation Verification Test Record for CHAN 1.

3. Press the HP 3562A keys as follows:

B

SCALE Y AUTO
SCALE

**SPCL
MARKER** MRKR →
PEAK

4. If the Yb marker reading is less than or equal to -131 dBVrms check PASS on the Operation Verification Test Record for CHAN 2.

Table 2-3 (OV) Spurious Signals

| Start Frequency | Frequency Span | Specification |
|-----------------|----------------|-----------------|
| 20 Hz | 1 kHz | ≤ -131 dBV |
| 1 kHz | 10 kHz | ≤ -131 dBV |
| 90 kHz | 10 kHz | ≤ -131 dBV |

D. For the rest of the start frequencies in table 2-3 perform steps 1 through 4:

1. Press the HP 3562A keys as follows:

FREQ START FREQ To start frequency in table

A FREQ SPAN To frequency span in table

START

**SPCL
MARKER** MRKR →
PEAK

2. If the Ya marker reading is less than or equal to -131 dBVrms check PASS on the Operation Verification Test Record for CHAN 1.

3. Press the HP 3562A keys as follows:

B

SPCL
MARKER MRKR →
 PEAK

4. If the Yb marker reading is less than or equal to -131 dBVrms check PASS on the Operation Verification Test Record for CHAN 2.

Table 2-4 (OV) Noise Level

| Start Frequency | Frequency Span | Specification |
|-----------------|----------------|-------------------------------------|
| 20 Hz | 1 kHz | ≤ -134 dBV/ $\sqrt{\text{Hz}}$ |
| 1 kHz | 50 kHz | ≤ -144 dBV/ $\sqrt{\text{Hz}}$ |
| 50 kHz | 50 kHz | ≤ -144 dBV/ $\sqrt{\text{Hz}}$ |

E. Press the HP 3562A keys as follows:

WINDOW FLAT TOP
UNITS P SPEC $V/\sqrt{\text{Hz}}$
 UNITS

F. For each of the start frequencies listed in table 2-4 perform steps 1 through 5:

1. Press the HP 3562A keys as follows:

FREQ START FREQ To start frequency in table
 FREQ SPAN To frequency span in table

START

2. When the average is complete, press the HP 3562A keys as follows:

A

SPCL
MARKER MRKR →
 PEAK

3. If the Ya marker reading is less than or equal to the specification, check PASS on the Operation Verification Test Record for CHAN 1.

4. Press the HP 3562A keys as follows:

B

**SPCL
MARKER**

.....

**MRKR →
PEAK**

5. If the Yb marker reading is less than or equal to the specification, check PASS on the Operation Verification Test Record for CHAN 2.

If Test Fails Check:

Adjustments 2nd Pass Gain Adjustment
Section III ADC Offset and Reference Adjustment

Troubleshooting A33, A35 Input Boards
Section VII A32, A34 Analog Digital Converter
 A5 Digital Filter
 A4 Local Oscillator

2-15 SOURCE AMPLITUDE ACCURACY AND FLATNESS

This test measures the amplitude accuracy and flatness of the HP 3562A source.

Required Test Equipment

None

Procedure

A. Connect the HP 3562A source to channel 1.

B. Press the HP 3562A keys as follows:

PRESET

.....

RESET

CAL

.....

**SINGLE
CAL**

INPUT

COUPLE

.....

**GROUND
CHAN 1**

RANGE

.....

5 V


```

MEAS
MODE      . . . . .  SWEPT
                   SINE           . . . . .  LINEAR
                                           SWEEP

SOURCE

. . . . .  SOURCE LEVEL . . . . .  4.47 V

UNITS      . . . . .  P SPEC           . . . . .  VOLTS
                   UNITS                   RMS

                                           . . . . .  VOLTS

FREQ       . . . . .  STOP
                   FREQ           . . . . .  65 kHz

START
    
```

C. When the sweep is complete perform steps 1 and 2:

1. Press the HP 3562A keys as follows:

```

SCALE      . . . . .  Y FIXD
                   SCALE           . . . . .  9,11 dB
    
```

2. If the trace is between the 9 dB and the 11 dB limits, check PASS on the Operation Verification Test Record for the 0 to 65 kHz span.

D. Press the HP 3562A keys as follows:

```

FREQ       . . . . .  START
                   FREQ           . . . . .  65 kHz
    
```

START

E. When the sweep is complete perform stage 1 and 2:

1. Press the HP 3562A keys as follows:

```

SCALE      . . . . .  Y FIXD
                   SCALE           . . . . .  8.5, 11 dB
    
```

2. If the trace is between the 8.5 dB and the 11 dB limits, check PASS on the Operation Verification Test Record for the 65 kHz to 100 kHz span.

If Test Fails Check:

| | |
|---------------------------------|-------------------------|
| Adjustments | None |
| Troubleshooting Section VIII | A30 Analog Source Board |

2-16 OPERATIONAL VERIFICATION TEST RECORD

| | |
|----------------------|-------------|
| 2-7 Self Test | PASS |
|----------------------|-------------|

| 2-8 DC Offset | | | |
|----------------------|----------------|--------|---------------|
| Range Setting | Measured Value | | Specification |
| | CHAN 1 | CHAN 2 | |
| -51 dBV | | | < -71 dBV |

| 2-9 Amplitude Accuracy and Flatness | | | | | |
|--|------------------|---------------|-------------|----------------|--------|
| CHAN 1 and CHAN 2 Floating | | | | | |
| Range Setting | Signal Frequency | Specification | | Measured Value | |
| | | Lower Limit | Upper Limit | CHAN 1 | CHAN 2 |
| 9 dBV | 1 kHz | 8.849 dBV | 9.151 dBV | | |
| 9 dBV | 99 kHz | 8.849 dBV | 9.151 dBV | | |
| 0 dBV | 1 kHz | -0.1513 dBV | 0.1513 dBV | | |
| 0 dBV | 99 kHz | -0.1513 dBV | 0.1513 dBV | | |
| -13 dBV | 1 kHz | -13.15 dBV | -12.85 dBV | | |
| -13 dBV | 99 kHz | -13.15 dBV | -12.85 dBV | | |

| 2-10 Amplitude and Phase Match | | | | | | |
|---------------------------------------|------|------|-------------------------|------|------|---------------------|
| Range Setting | Part | PASS | Amplitude Specification | Part | PASS | Phase Specification |
| -49 dBV | 1 | | ±0.1 dB | 4 | | ±0.5° |
| 0 dBV | 2 | | ±0.1 dB | 5 | | ±0.5° |
| 10 dBV | 3 | | ±0.1 dB | 6 | | ±0.8° |

| 2-11 Frequency Accuracy | | | |
|--------------------------------|---------------|-------------|----------------|
| Signal Frequency | Specification | | Measured Value |
| | Lower Limit | Upper Limit | |
| 99,000 Hz | 98.996 kHz | 99.004 kHz | |

| 2-12 Common Mode Rejection | | | | |
|----------------------------|--------------------------|---------------------------|-----------------------|----------------|
| First Measurement – | | Second Measurement = | | Relative Value |
| Signal Frequency | First Measurement CHAN 1 | Second Measurement CHAN 1 | Measured Value CHAN 1 | Specification |
| 66 Hz | | | | ≥80 dB |
| 500 Hz | | | | ≥65 dB |
| Signal Frequency | First Measurement CHAN 2 | Second Measurement CHAN 2 | Measured Value CHAN 2 | Specification |
| 66 Hz | | | | ≥80 dB |
| 500 Hz | | | | ≥65 dB |

| 2-13 Single Channel Phase Accuracy | | | | | | |
|------------------------------------|---------|--------|---------------|-------------|----------------|--------|
| Signal Frequency | Trigger | | Specification | | Measured Value | |
| | Slope | Type | Lower Limit | Upper Limit | CHAN 1 | CHAN 2 |
| 9 kHz | POS | EXT | –92.5° | –87.5° | | |
| 99 kHz | POS | CHAN 1 | –102° | –78.0° | | |

| 2-14 Noise and Spurious Signal Level | | | | | |
|--------------------------------------|----------------|-------------|-------------|----------------|--|
| Spurious Signals | | | | | |
| Start Frequency | Frequency Span | PASS CHAN 1 | PASS CHAN 2 | Specification | |
| 20 Hz | 1 kHz | | | ≤ –131 dBV | |
| 1 kHz | 10 kHz | | | ≤ –131 dBV | |
| 90 kHz | 10 kHz | | | ≤ –131 dBV | |
| Noise Level | | | | | |
| Start Frequency | Frequency Span | PASS CHAN 1 | PASS CHAN 2 | Specification | |
| 20 Hz | 1 kHz | | | ≤ –134 dBV/√Hz | |
| 1 kHz | 50 kHz | | | ≤ –144 dBV/√Hz | |
| 50 kHz | 50 kHz | | | ≤ –144 dBV/√Hz | |

| 2-15 Source Amplitude Accuracy and Flatness | |
|---|------|
| 0 Hz to 65 kHz | PASS |
| 65 kHz to 100 kHz | PASS |

PART B PERFORMANCE TESTS

2-17 INTRODUCTION

To verify the the HP 3562A is meeting its published specifications, the performance tests must be done in the order listed every twelve months. Use the "Operational Verification," part A, for incoming and after-repair inspections. The performance tests take approximately eight hours to complete.

2-18 HOW TO USE PART B

1. Start each performance test by setting the test equipment to the preset conditions listed in the "Initial Equipment Setup," paragraph 2-20.
2. There are two types of keys on the HP 3562A, hard keys and soft keys. In this section the hard keys are in bold text, and the soft keys are in regular test.

For example:

FREQ FREQ SPAN **10 kHz**

This example instructs you to press the hard key **FREQ** and the soft key **FREQ SPAN**. After pressing the soft key **FREQ SPAN** enter 10 kHz.

3. Refer to figure 2-10 for the position of the X and Y marker readings.
4. Record the results of each of the performance tests on the "Performance Test Record," paragraph 2-42. This test record may be reproduced without written permission of Hewlett-Packard.
5. If the HP 3562A fails a test, use the "If Test Fails Check:" paragraph at the end of each test.

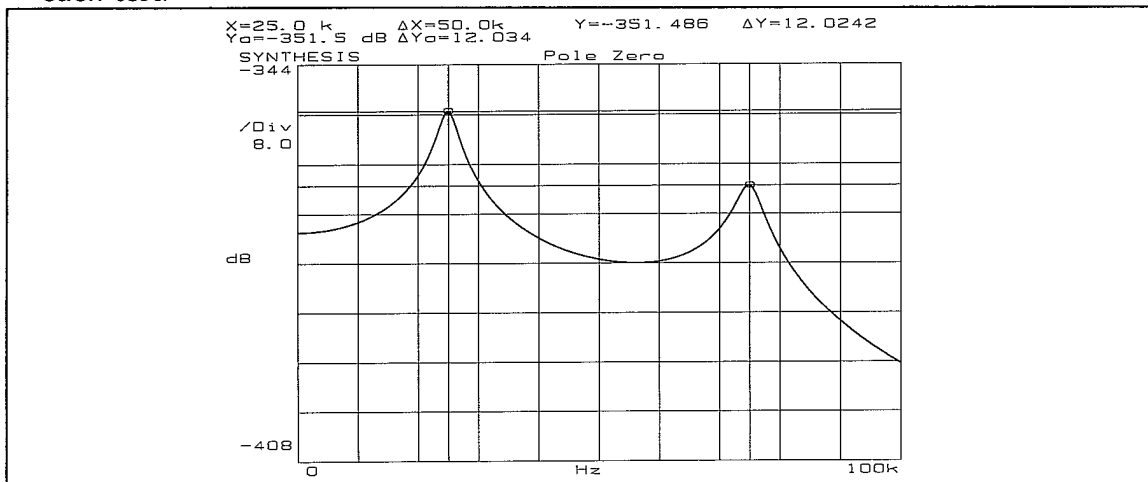


Figure 2-10 Marker Positions

2-19 REQUIRED TEST EQUIPMENT

The recommended test equipment is listed in table 1-4. If the recommended equipment is not available, a substitute may be used which meets or exceeds the required characteristics given in table 1-4.

2-20 INITIAL EQUIPMENT SETUP

When the recommended test equipment of table 1-4 is used to complete the performance tests, the instruments listed below must be set to the preset conditions listed before beginning the test. In each test, any unspecified parameters should be set to the following conditions:

HP 3325A Frequency Synthesizer

| | | |
|------------|-------|---------------|
| Function | | SINE WAVE (~) |
| Frequency | | 1 kHz |
| Amplitude | | 1 mVrms |
| Phase | | 0 Degrees |
| dc Offset | | 0V |
| Modulation | | OFF |
| Sweep | | OFF |

Fluke 5200 AC Calibrator

| | | |
|-----------------|-------|----------|
| Frequency | | 1 kHz |
| Amplitude | | .01 Vrms |
| Voltage Error % | | OFF |
| Vernier | | 0 |
| Mode | | OPER |
| Control | | LOCAL |
| Phase Lock | | OFF |
| Sense | | INTERNAL |

HP 3456A Digital Voltmeter

| | | |
|-----------------|---------|-----------|
| Function | | ac V (~V) |
| Range | | AUTO |
| Trigger | | INTERNAL |
| Sample Rate | | MAXIMUM |
| High Resolution | | ON |
| Auto Cal | | ON |

2-21 SELF TEST

This test determines if the HP 3562A is operating correctly. No tests should be attempted until the instrument passes this test.

Required Test Equipment

None

Procedure

1. Press the HP 3562A keys as follows:

SPCL FCTN **SELF TEST**

2. This test takes about 0.5 minutes to complete.
3. When "SELF TEST PASSES" is displayed in the lower right corner of the display, check PASS on the Performance Test Record.

If Test Fails:

Go to "Fault Isolation," Section VII.

2-22 DC OFFSET

This test measures the level of the dc offset generated within the HP 3562A with auto on.

Specification

For range settings between +27 dBV and -35 dBV the DC offset will be greater than 30 dB below the range setting. For range settings between -36 dBV and -51 dBV the offset will be greater than 20 dB below the range setting.

Required Test Equipment

(2) 50Ω feedthrough terminations HP 11048C

Table 2-5 DC Offset

| Range Setting | Specification |
|---------------|---------------|
| 7 dBVrms | < -23 dBV |
| -35 dBVrms | < -65 dBV |
| -51 dBVrms | < -71 dBV |

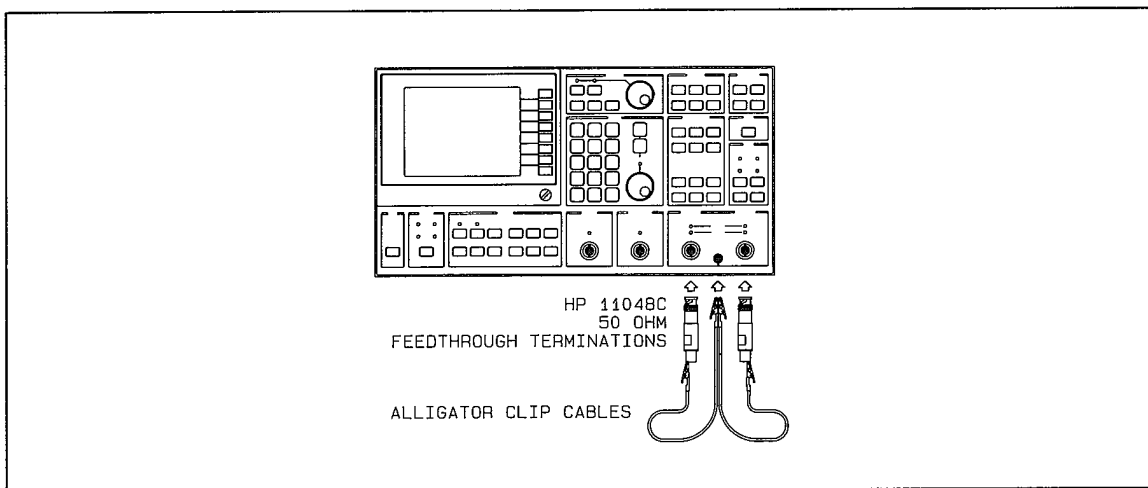


Figure 2-11 DC Offset Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-11. Keep the leads to chassis ground as short as possible.

B. Press the HP 3562A keys as follows:

| | | | | |
|------------------|-------|-----------------|-------|--------------|
| PRESET | | RESET | | |
| CAL | | AUTO ON | | |
| | | SINGLE CAL | | |
| WINDOW | | UNIFRM (NONE) | | |
| AVG | | 2 | | ENTER |
| | | STABLE | | |
| FREQ | | 1 kHz | | |
| UNITS | | P SPEC UNITS | | VOLTS RMS |
| A & B | | | | VOLTS |
| X | | 0 Hz | | |

C. For each of the range settings listed in table 2-5, perform steps 1 through 3:

1. Press the HP 3562A keys as follows:

| | | |
|--------------|-------|---------------------------------|
| RANGE | | To range setting in table |
|--------------|-------|---------------------------------|

START

2. Record the Ya marker reading on the performance test record for the CHAN 1 measured value.
3. Record the Yb marker reading on the performance test record for the CHAN 2 measured value.

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments Section III | Track and Hold Offset Adjustment Input DC Offset Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards |

2-23 AMPLITUDE ACCURACY and FLATNESS

This test measures the amplitude accuracy and flatness of the HP 3562A using the amplitude reference of the ac calibrator.

Specification

If the measurement of a signal is between the BNC center conductor and BNC shell and the amplitude is equal to the range setting, the marker amplitude reading will not deviate from the actual signal amplitude by more than:

| Range Setting | Accuracy |
|--------------------|---|
| +27 dBV to -40 dBV | ± 0.15 dB $\pm 0.015\%$ Range Setting |
| -41 dBV to -51 dBV | ± 0.25 dB $\pm 0.025\%$ Range Setting |

If the measurement of a signal includes a signal between the BNC shell and the chassis, the marker amplitude reading will not deviate from the actual signal amplitude by more than:

| Range Setting | Accuracy |
|--------------------|--|
| +27 dBV to -40 dBV | ± 0.50 dB $\pm .015\%$ Range Setting |
| -41 dBV to -51 dBV | ± 0.60 dB $\pm .025\%$ Range Setting |

Required Test Equipment

| | | |
|-----------------------|------|--------------|
| Frequency Synthesizer | | HP 3325A |
| AC Calibrator | | Fluke 5200A |
| BNC Tee | | HP 1250-0781 |

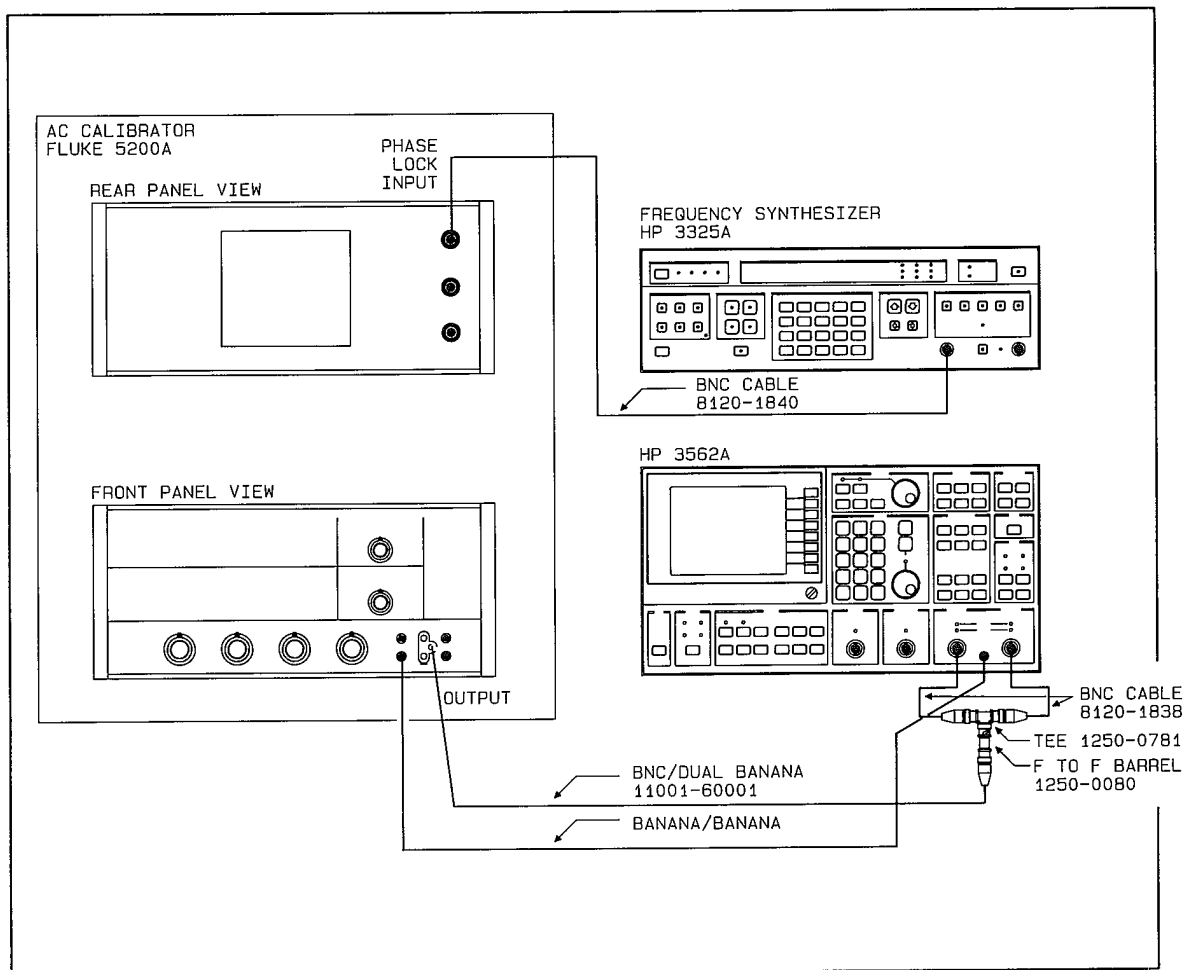


Figure 2-12 Amplitude Accuracy and Flatness Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-12. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.
- B. Set the test instruments initially as follows:

Frequency Synthesizer

| | | |
|-----------|------|-----------|
| Amplitude | | 0.5 Vrms |
| Frequency | | 1 kHz |
| Function | | Sine Wave |

AC Calibrator

| | | |
|------------|------|-------------|
| Phase Lock | | ON |
| Sense | | INTERNAL |
| Mode | | OPER |
| Frequency | | 1 kHz |
| Amplitude | | 2.8184 Vrms |

C. Press the HP 3562A keys as follows:

| | | | | |
|-------------------------|-------|------------------|-------|--------------|
| PRESET | | RESET | | |
| CAL | | SINGLE CAL | | |
| INPUT COUPLE | | GROUND CHAN 1 | | |
| | | GROUND CHAN 2 | | |
| WINDOW | | FLAT TOP | | |
| AVG | | 4 | | ENTER |
| | | STABLE | | |
| UNITS | | P SPEC UNITS | | VOLTS RMS |
| | | | | VOLTS |

A & B

**Table 2-6 Amplitude Accuracy and Flatness
Measurement One**

| BNC shell grounded | | | | |
|------------------------------|---------------------|----------------------------|---------------|-------------|
| HP 3562A Range Setting | Signal Frequency | AC Calibrator Amplitude | Specification | |
| | | | Lower Limit | Upper Limit |
| 9 dBVrms | 1 kHz | 2.8184 Vrms | 8.849 dBV | 9.151 dBV |
| 9 dBVrms | 99 kHz | 2.8184 Vrms | 8.849 dBV | 9.151 dBV |
| -13 dBVrms | 1 kHz | .22387 Vrms | -13.15 dBV | -12.85 dBV |
| -13 dBVrms | 50 kHz | .22387 Vrms | -13.15 dBV | -12.85 dBV |
| -13 dBVrms | 90 kHz | .22387 Vrms | -13.15 dBV | -12.85 dBV |
| -13 dBVrms | 99 kHz | .22387 Vrms | -13.15 dBV | -12.85 dBV |
| -23 dBVrms | 1 kHz | 70.795 mVrms | -23.15 dBV | -22.85 dBV |
| -23 dBVrms | 99 kHz | 70.795 mVrms | -23.15 dBV | -22.85 dBV |
| -26 dBVrms | 1 kHz | 50.119 mVrms | -26.15 dBV | -25.85 dBV |
| -21 dBVrms | 1 kHz | 89.125 mVrms | -21.15 dBV | -20.85 dBV |
| -17 dBVrms | 1 kHz | .14125 Vrms | -17.15 dBV | -16.85 dBV |
| -14 dBVrms | 1 kHz | .19953 Vrms | -14.15 dBV | -13.85 dBV |
| -11 dBVrms | 1 kHz | .28184 Vrms | -11.15 dBV | -10.85 dBV |

D. For each of the frequencies listed in table 2-6 perform steps 1 through 7.

1. Press the HP 3562A keys as follows:

RANGE To range setting in table

FREQ **CENTER FREQ** To signal frequency
in table

2. Set the ac calibrator to the signal frequency.

3. Set the frequency synthesizer to the signal frequency.

4. Set the ac calibrator's amplitude.

5. Press the HP 3562A keys as follows:

START

SPCL

MARKER **MRKR** →
PEAK

6. Record the Ya marker reading on the Performance Test Record for the measured value CHAN 1.

7. Record the Yb marker reading on the Performance Test Record for the measured value CHAN 2.

**Table 2-7 Amplitude Accuracy and Flatness
Measurement Two**

| BNC shell grounded | | | | |
|------------------------------|---------------------|----------------------------|---------------|-------------|
| HP 3562A Range Setting | Signal Frequency | AC Calibrator Amplitude | Specification | |
| | | | Lower Limit | Upper Limit |
| -51 dBVrms | 1 kHz | 2.8184 mVrms | -51.25 dBV | -50.75 dBV |
| -49 dBVrms | 1 kHz | 3.5481 mVrms | -49.25 dBV | -48.75 dBV |
| -47 dBVrms | 1 kHz | 4.4668 mVrms | -47.25 dBV | -46.75 dBV |
| -45 dBVrms | 1 kHz | 5.6234 mVrms | -45.25 dBV | -44.75 dBV |
| -43 dBVrms | 1 kHz | 7.0795 mVrms | -43.25 dBV | -42.75 dBV |
| -41 dBVrms | 1 kHz | 8.9125 mVrms | -41.25 dBV | -40.75 dBV |
| -39 dBVrms | 1 kHz | 11.220 mVrms | -39.25 dBV | -38.75 dBV |

E. Repeat part D using table 2-7 for measurement two.

F. Press the HP 3562A keys as follows:

```

INPUT
COUPLE  . . . .  FLOAT
                                     CHAN 1

                                     . . . .  FLOAT
                                               CHAN 2
    
```

G. Reverse the banana plug connector at the ac calibrator so the high input signal goes to the BNC shell of HP 3562A's input channels. The BNC center conductor should be grounded for each channel.

Table 2-8 Amplitude Accuracy and Flatness Measurement Three

| BNC center conductor grounded | | | | |
|-------------------------------|------------------|-------------------------|---------------------------|---------------------------|
| HP 3562A Range Setting | Signal Frequency | AC Calibrator Amplitude | Specification Lower Limit | Specification Upper Limit |
| 8 dBVrms | 1 kHz | 2.4570 Vrms | 7.499 dBV | 8.501 dBV |
| 8 dBVrms | 99 kHz | 2.4570 Vrms | 7.499 dBV | 8.501 dBV |
| -11 dBVrms | 1 kHz | .27701 Vrms | -11.50 dBV | -10.50 dBV |
| -13 dBVrms | 1 kHz | .21404 Vrms | -13.50 dBV | -12.50 dBV |
| -13 dBVrms | 50 kHz | .21404 Vrms | -13.50 dBV | -12.50 dBV |
| -13 dBVrms | 90 kHz | .21404 Vrms | -13.50 dBV | -12.50 dBV |
| -13 dBVrms | 99 kHz | .21404 Vrms | -13.50 dBV | -12.50 dBV |
| -27 dBVrms | 1 kHz | 43.702 mVrms | -27.50 dBV | -26.50 dBV |
| -27 dBVrms | 99 kHz | 43.702 mVrms | -27.50 dBV | -26.50 dBV |

H. Repeat part D using table 2-8 for measurement three.

If Test Fails Check:

- | | |
|--------------------------------|--|
| Adjustments Section III | 2nd Pass Gain Adjustment AC Offset and Reference Adjustment Input Flatness Adjustment Input Attenuator Adjustments Calibrator Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards A30 Analog Source Board |

2-24 AMPLITUDE LINEARITY

This test measures the amplitude linearity of the HP 3562A by using the amplitude reference of the ac calibrator.

Specification

If the measurement of a signal is between the BNC center conductor and BNC shell and the amplitude is equal to the range setting, the marker amplitude reading will not deviate from the actual signal amplitude by more than:

| Range Setting | Accuracy |
|--------------------|---|
| +27 dBV to -40 dBV | ± 0.15 dB $\pm 0.015\%$ Range Setting |
| -41 dBV to -51 dBV | ± 0.25 dB $\pm 0.025\%$ Range Setting |

If the measurement of a signal includes a signal between the BNC shell and the chassis, the marker amplitude reading will not deviate from the actual signal amplitude by more than:

| Range Setting | Accuracy |
|--------------------|--|
| +27 dBV to -40 dBV | ± 0.50 dB $\pm .015\%$ Range Setting |
| -41 dBV to -51 dBV | ± 0.60 dB $\pm .025\%$ Range Setting |

Required Test Equipment

| | | |
|-----------------------|------|--------------|
| Frequency Synthesizer | | HP 3325A |
| AC Calibrator | | Fluke 5200A |
| BNC | | HP 1250-0781 |

Procedure

- A. Connect the test instruments as shown in figure 2-13. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.
- B. Set the test instruments initially as follows:

Frequency Synthesizer

| | | |
|-----------|------|--------|
| Frequency | | 10 kHz |
| Amplitude | | 1 Vrms |

AC Calibrator

| | | |
|------------|------|----------|
| Frequency | | 10 kHz |
| Amplitude | | 10 Vrms |
| Phase Lock | | ON |
| Sense | | INTERNAL |
| Mode | | OPER |

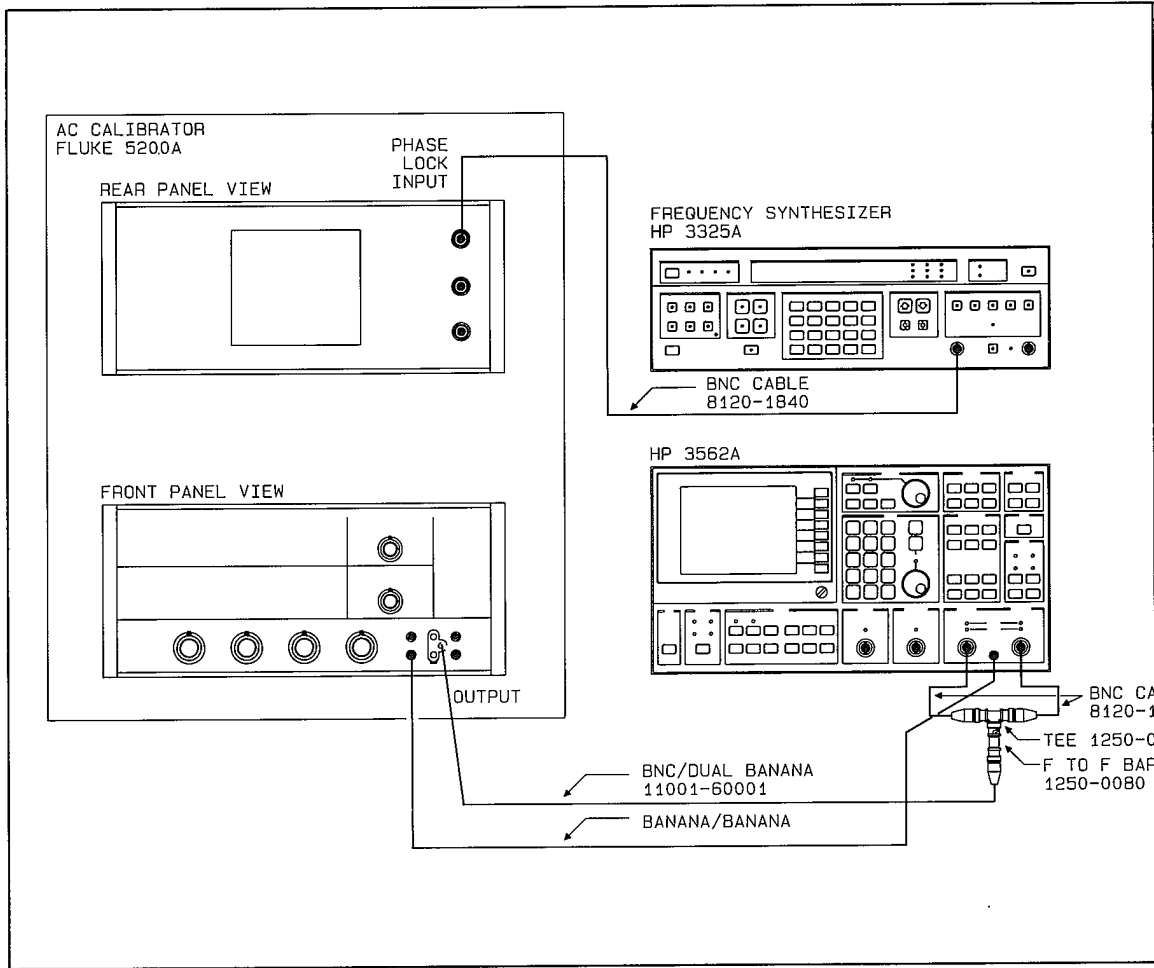


Figure 2-13 Amplitude Linearity Test Setup

C. Press the HP 3562A keys as follows:

| | | | |
|---------------|-------|--------------------|---------------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| WINDOW | | FLAT TOP | |
| AVG | | 4 | ENTER |
| | | STABLE | |
| RANGE | | 21 dBVrms | |
| FREQ | | CENTER FREQ | 10 kHz |

```

INPUT
COUPLE      . . . .  GROUND
                  CHAN 1

                  . . . .  GROUND
                  CHAN 2

UNITS      . . . .  P SPEC      . . . .  VOLTS
                  UNITS          . . . .  RMS

                  . . . .  VOLTS

A & B

COORD     . . . .  MAG
                  (LIN)

SCALE     . . . .  Y AUTO SCALE
    
```

Table 2-9 Amplitude Linearity

| AC Calibrator Amplitude | Specification BNC shell grounded | | Specification BNC center conductor grounded | |
|----------------------------|-------------------------------------|--------------|--|--------------|
| | Upper Limit | Lower Limit | Upper Limit | Lower Limit |
| 10.00 Vrms | 10.18 Vrms | 9.827 Vrms | 10.59 Vrms | 9.439 Vrms |
| 1.000 Vrms | 1.019 Vrms | 981.4 mVrms | 1.061 Vrms | 942.6 mVrms |
| 100.0 mVrms | 103.2 mVrms | 96.79 mVrms | 107.4 mVrms | 92.91 mVrms |
| 10.00 mVrms | 11.67 mVrms | 8.329 mVrms | 12.09 mVrms | 7.941 mVrms |
| 3.1623 mVrms | 4.717 mVrms | 1.608 mVrms | 4.850 mVrms | 1.485 mVrms |
| 1.000 mVrms | 2.517 mVrms | -517.1 uVrms | 2.559 mVrms | -555.9 uVrms |

D. For each of the amplitudes listed in table 2-9 perform steps 1 through 4.

1. Set the ac calibrator's amplitude.
2. Press the HP 3562A keys as follows:

START

SPCL

MARKER MRKR →
PEAK

3. Record the Ya marker reading on the Performance Test Record for the measured value CHAN 1.
4. Record the Yb marker reading on the Performance Test Record for the measured value CHAN 2.

E. Press the HP 3562A keys as follows:

| | | |
|---------------|-------|--------|
| INPUT | | |
| COUPLE | | FLOAT |
| | | CHAN 1 |
| | | FLOAT |
| | | CHAN 2 |

F. Reverse the banana plug connector at the ac calibrator so the high input signal goes to the BNC shell of HP 3562A's input channels. The BNC center conductor should be grounded for each channel.

G. Repeat part D for BNC center conductor grounded.

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments Section III | 2nd Pass Gain Adjustment ADC Offset and Reference Adjustment Input Flatness Adjustment Input Attenuator Adjustments Calibrator Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards A30 Analog Source Board |

2-25 AMPLITUDE AND PHASE MATCH

This test determines if the HP 3562A's amplitude and phase match between channel 1 and channel 2 are within the specified limits.

Specification

BNC shell of both channels grounded:

The amplitude deviation between channels will be no more than ± 0.1 dB, and the phase deviation no more than ± 0.5 degrees.

BNC center conductor of both channels grounded:

The amplitude deviation between channels will be no more than ± 0.8 dB, and the phase deviation no more than ± 8.5 degrees.

Required Test Equipment

BNC TEE HP 1250-0781

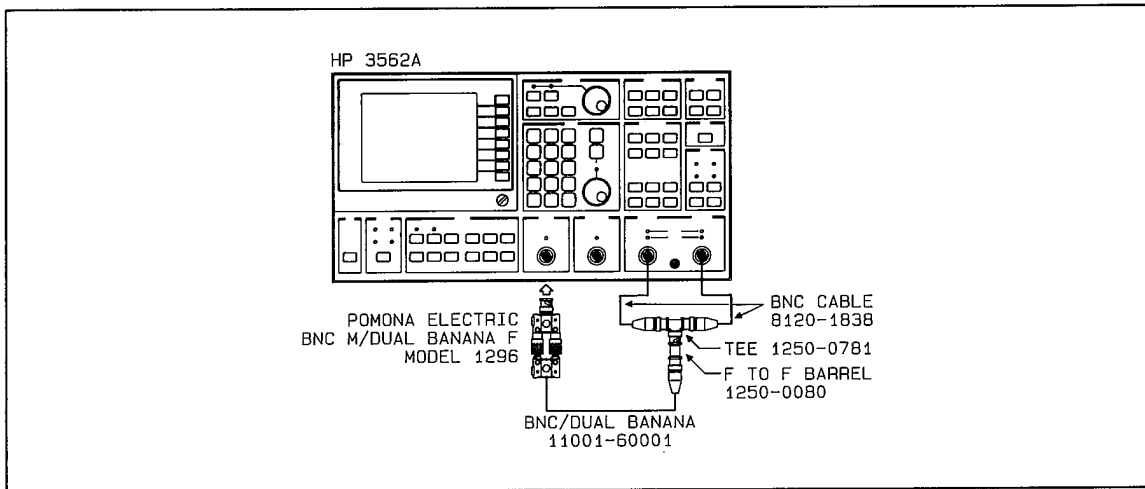


Figure 2-14 Amplitude and Phase Match Test Setup

Procedure

- A. Connect the HP 3562A as shown in figure 2-14. The cables to channel 1 and channel 2 must be the same length.
- B. Press the HP 3562A keys as follows:

| | | |
|-------------------------|-------|-----------------|
| PRESET | | RESET |
| CAL | | SINGLE CAL |
| INPUT COUPLE | | CHAN1 AC |
| | | CHAN2 AC |
| | | GROUND CHAN1 |
| | | GROUND CHAN2 |
| SELECT TRIG | | 0 V |
| | | SOURCE TRIG |

```

WINDOW  . . . .  UNIFRM
AVG      . . . .  16          . . . .  ENTER
          . . . .  STABLE
SOURCE  . . . .  PRIODC
          . . . .  CHIRP
MEAS
DISP    . . . .  FREQ RESP
SCALE   . . . .  X FIXD
          . . . .  SCALE          . . . .  .375, 100 kHz
    
```

C. Perform steps 1 through 6:

1. Press the HP 3562A keys as follows:

```

RANGE   . . . .  -47 dBVrms
SOURCE  . . . .  SOURCE LEVEL . . . .  -49 dBVrms
SCALE   . . . .  Y FIXD
          . . . .  SCALE          . . . .  -.2, .2 dB
START
Y       . . . .  -.1, .1 dB
    
```

2. If the measurement is within the marker band, check PASS on the Performance Test Record for part 1.

3. Press the HP 3562A keys as follows:

```

RANGE   . . . .  0 dBVrms
SOURCE  . . . .  SOURCE LEVEL . . . .  0 dBVrms
START
Y       . . . .  -.1,.1 dB
    
```

4. If the measurement is within the marker band, check PASS on the Performance Test Record for part 2.

5. Press the HP 3562A keys as follows:

RANGE **10** dBVrms
SOURCE SOURCE LEVEL **10** dBVrms
START
Y **-.1,.1** dB

6. If the measurement is within the marker band, check PASS on the Performance Test Record for part 3.

D. Perform steps 1 through 6:

1. Press the HP 3562A keys as follows:

RANGE **-47** dBVrms
SOURCE SOURCE LEVEL **-49** dBVrms
COORD PHASE
START
SCALE Y FIXD
SCALE **-1, 1** Degree
Y Y VALUE **-.5, .5** Degree

2. If the measurement is within the marker band, check PASS on the Performance Test Record for part 4.

3. Press the HP 3562A keys as follows:

RANGE **0** dBVrms
SOURCE SOURCE LEVEL **0** dBVrms
START
Y Y VALUE **-.5,.5** Degree

4. If the measurement is within the marker band, check PASS on the Performance Test Record for part 5.

5. Press the HP 3562A keys as follows:

RANGE **10** dBVrms
SOURCE SOURCE LEVEL **10** dBVrms
START
Y Y VALUE **-.5, .5** Degree

6. If the measurement is within the marker band, check PASS on the Performance Test Record for part 6.

E. Reverse one of the banana plug connectors so the center conductor of each channel's BNC is grounded.

F. Perform steps 1 through 4:

1. Press the HP 3562A keys as follows:

INPUT
COUPLE FLOAT
 CHAN1
 FLOAT
 CHAN2
COORD MAG(dB)
SCALE Y FIXD
 SCALE **-1,1** dB
RANGE **-13** dBVrms
SOURCE SOURCE LEVEL **-13** dBVrms
START
Y Y VALUE **-.8, .8** dB

2. If the measurement is within the marker band, check PASS on the Performance Test Record for part 7.

3. Press the HP 3562A keys as follows:

RANGE **8** dBVrms
SOURCE SOURCE LEVEL **8** dBVrms
START
Y Y VALUE **-.8, .8** dB

4. If the measurement is within the marker band, check PASS on the Performance Test Record for part 8.

G. Perform steps 1 through 4:

1. Press the HP 3562A keys as follows:

RANGE **-13** dBVrms
SOURCE SOURCE LEVEL **-13** dBVrms
COORD PHASE
START
SCALE Y FIXD
 SCALE **-10, 10** Degree
Y Y VALUE **-8.5, 8.5** degree

2. If the measurement is within the marker band, check PASS on the Performance Test Record for part 9.

3. Press the HP 3562A keys as follows:

RANGE **8** dBVrms
SOURCE SOURCE LEVEL **8** dBVrms
START
Y Y VALUE **-8.5, 8.5** Degree

4. If the measurement is within the marker band, check PASS on the Performance Test Record for part 10.

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments Section III | 2nd Pass Gain Adjustment ADC Offset and Reference Adjustment Input Flatness Adjustment Input Attenuator Adjustments Calibrator Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards A30 Analog Source Board |

2-26 ANTI-ALIAS FILTER RESPONSE

Signals with frequencies greater than 156 kHz may be shifted down into the 100 kHz frequency range as a result of the HP 3562A's 256 kHz sample rate. This test measures the ability of the 100 kHz low pass anti-alias filter to reject frequencies 156 kHz and greater.

NOTE

The HP 3325A may produce some spurious signals in the 0 to 100 kHz span. Ignore signals at frequencies other than those listed in the table when performing this test.

Specification

All signals aliasing into the 0 to 100 kHz frequency span will be attenuated at least 80 dB below the range setting.

Required Test Equipment

| | | |
|-----------------------------|-------|--------------|
| Frequency Synthesizer | | HP 3325A |
| 50Ω feedthrough termination | | HP 11048C |
| BNC Tee | | HP 1250-0781 |

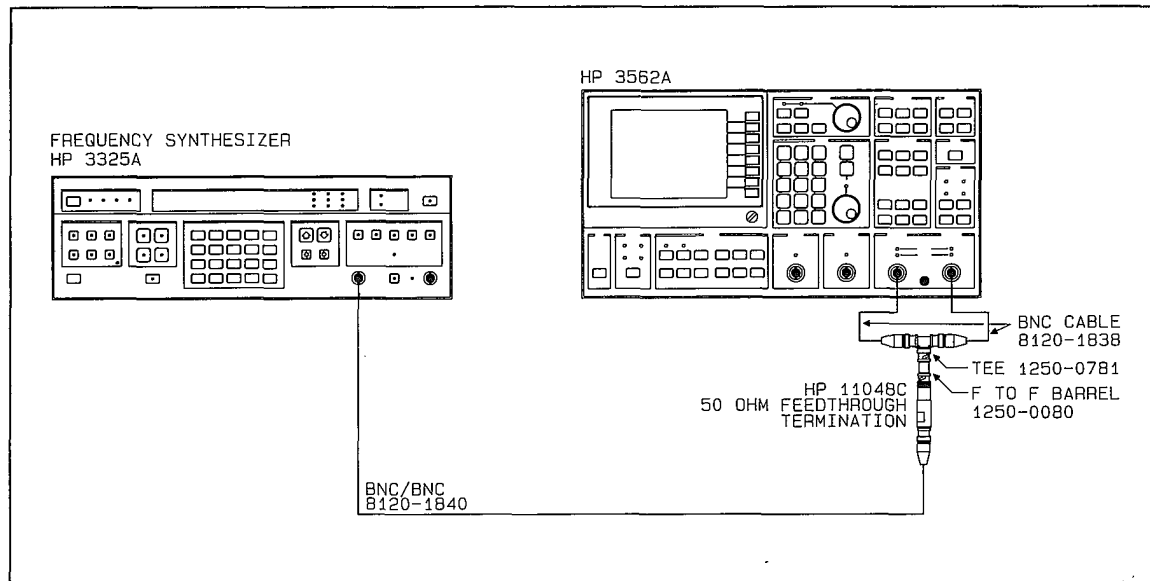


Figure 2-15 Anti-Alias Filter Response Test Setup

Procedure

A. Connect the test instruments as shown in figure 2-15. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set the test instruments initially as follows:

Frequency Synthesizer

| | | |
|-----------|------|-----------|
| Amplitude | | 1 Vrms |
| Frequency | | 156 kHz |
| Function | | Sine Wave |

C. Press the HP 3562A keys as follows:

| | | | |
|-------------------------|------|-----------------|-------------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| RANGE | | 1 Vrms | |
| AVG | | 16 | ENTER |
| | | STABLE | |
| WINDOW | | FLAT TOP | |
| INPUT COUPLE | | GROUND CHAN1 | |
| | | GROUND CHAN2 | |
| A & B | | | |
| UNITS | | P SPEC UNITS | VOLTS RMS |
| | | | VOLTS |

Table 2-10 Anti-Alias Filter

| Signal Frequency | Alias Frequency |
|------------------|-----------------|
| 156 kHz | 100 kHz |
| 184 kHz | 72 kHz |
| 206 kHz | 50 kHz |
| 267 kHz | 11 kHz |

D. For each of the signal frequencies listed in table 2-10 perform steps 1 through 4:

1. Set the frequency synthesizer to the signal frequency in table.
2. Press the HP 3562A keys as follows:

START

X To alias frequency in table

3. If the Ya reading is less than or equal to -80 dBVrms check PASS on the Performance Test Record for CHAN 1.
4. If the Yb reading is less than or equal to -80 dBVrms check PASS on the Performance Test Record for CHAN 2.

If Test Fails Check:

| | |
|---------------------------------|--|
| Adjustments Section III | None |
| Troubleshooting Section VIII | A32, A34 Analog Digital Converter Boards |

2-27 FREQUENCY ACCURACY

This test measures the frequency accuracy of the HP 3562A.

Specification

The frequency reading will not deviate from the actual signal frequency by more than 0.004%.

Required Test Equipment

| | | |
|-----------------------------|---------|-----------|
| Frequency Synthesizer | | HP 3325A |
| 50Ω feedthrough termination | | HP 11048C |

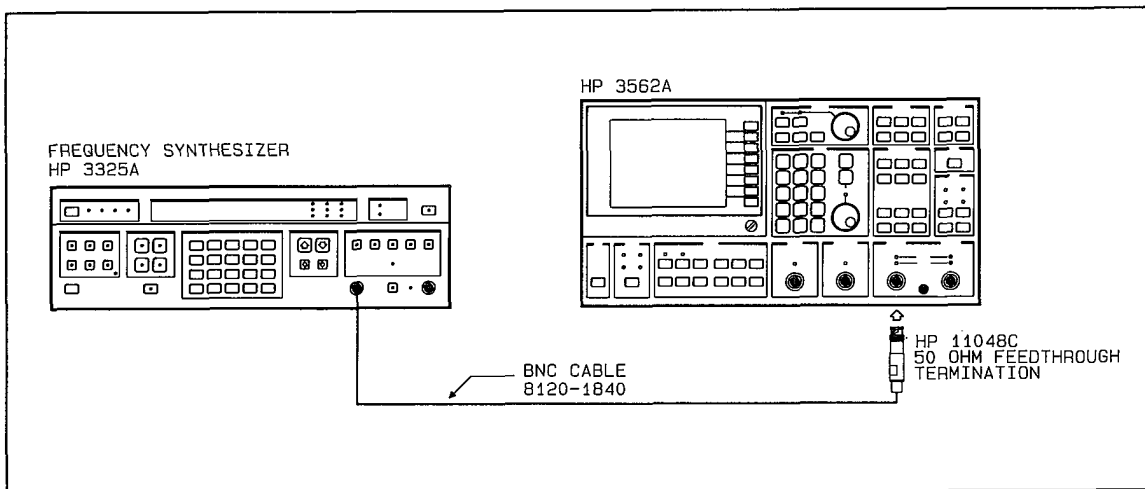


Figure 2-16 Frequency Accuracy Test Setup

Procedure

- A. Connect the test equipment as shown in figure 2-16. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.
- B. Set the test instruments initially as follows:

Frequency Synthesizer

| | | |
|-----------|------|-----------|
| Frequency | | 99 kHz |
| Amplitude | | 1 Vrms |
| Function | | Sine Wave |

- C. Press the HP 3562A keys as follows:

| | | |
|---------------|------|-------------------------|
| PRESET | | RESET |
| CAL | | SINGLE CAL |
| RANGE | | 0 dBVrms |
| FREQ | | CENTER FREQ 99 kHz |
| | | FREQ SPAN5 kHz |
| AVG | | 2 ENTER |
| | | STABLE |

START

X

D. Record the X marker reading as the measured value on the Performance Test Record.

If Test Fails Check:

| | |
|---------------------------------|--------------------------------|
| Adjustments Section III | 20.48 MHz Reference Adjustment |
| Troubleshooting Section VIII | A31 Trigger Board |

2-28 INPUT COUPLING INSERTION LOSS

This test measures the insertion loss at 1 Hz due to the ac coupling capacitors. The amplitude of a 1 Hz signal is measured in both ac and dc coupled modes. The insertion loss is calculated as:

$$\frac{\text{dc Coupled Amplitude}}{\text{ac Coupled Amplitude}} = \text{Insertion Loss}$$

Specification

The insertion loss at 1 Hz due to the ac coupling capacitors will be less than 3 dB (41.3%).

Required Test Equipment

| | | |
|-----------------------------|------|--------------|
| Frequency Synthesizer | | HP 3325A |
| 50Ω feedthrough termination | | HP 11048C |
| BNC Tee | | HP 1250-0781 |

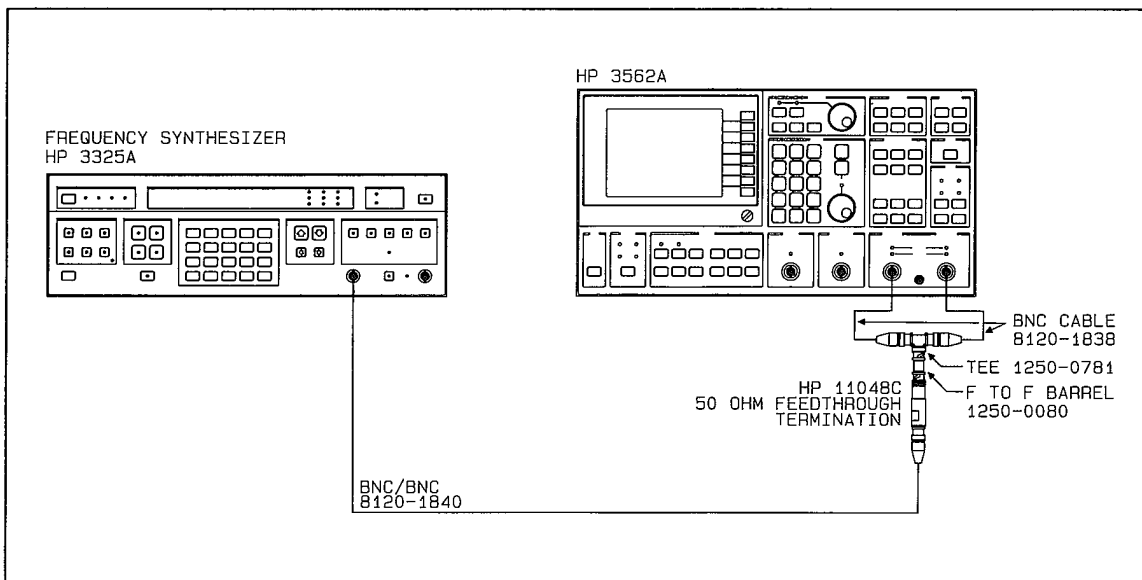


Figure 2-17 Input Coupling Insertion Loss Test Setup

Procedure

A. Connect the test equipment as shown in figure 2-17. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set the frequency synthesizer initially as follows:

Frequency Synthesizer

Frequency 1 Hz
 Amplitude 1 Vrms
 Function Sine Wave

C. Press the HP 3562A keys as follows:

PRESET RESET

CAL SINGLE
 CAL

RANGE 1 Vrms

FREQ FREQ SPAN **100 Hz**

WINDOW UNIFRM

AVG **4** ENTER
 STABLE

UNITS P SPEC VOLTS
 UNITS RMS
 VOLTS

INPUT COUPLE CHAN1
 AC

START

X 1 Hz X MRKR
 SCALE

SAVE RECALL SAVE DATA # **1** ENTER

INPUT COUPLE CHAN1
 DC

START

MATH DIV SAVED 1

(NOTE: Ignore math overflow message.)

D. Record the Ya reading on the Performance Test Record for channel 1.

E. Press the HP 3562A keys as follows:

B

**INPUT
COUPLE** CHAN2
AC

START

**SAVE
RECALL** SAVE DATA # **2** ENTER

**INPUT
COUPLE** CHAN2
DC

START

MATH DIV SAVED 2

F. Record the Yb reading on the Performance Test Record for channel 2.

If Test Fails Check:

| | |
|---------------------------------|-----------------------|
| Adjustments | None |
| Troubleshooting Section VIII | A33, A35 Input Boards |

2-29 SINGLE CHANNEL PHASE ACCURACY

This test measures the phase accuracy of the HP 3562A relative to the phase of the trigger signal. The frequency synthesizer is used to input a square wave to one channel and the external trigger input.

Specification

When the BNC shell of a channel is grounded, the marker phase reading will not deviate from the actual phase of the signal relative to the trigger by more than:

| Frequency Range | Phase Deviation |
|-------------------|-----------------|
| 0 Hz to <10 kHz | ±2.5 degrees |
| 10 kHz to 100 kHz | ±12.0 degrees |

When the BNC center conductor of a channel is grounded, the marker phase reading will not deviate from the actual phase of the signal relative to the trigger by more than:

| Frequency Range | Phase Deviation |
|-------------------|-----------------|
| 0 to <10 kHz | ±6.5 degrees |
| 10 kHz to 100 kHz | ±16.0 degrees |

Required Test Equipment

| | | |
|-----------------------------|------|--------------|
| Frequency Synthesizer | | HP 3325A |
| 50Ω feedthrough termination | | HP 11048C |
| (2) BNC Tees | | HP 1250-0781 |

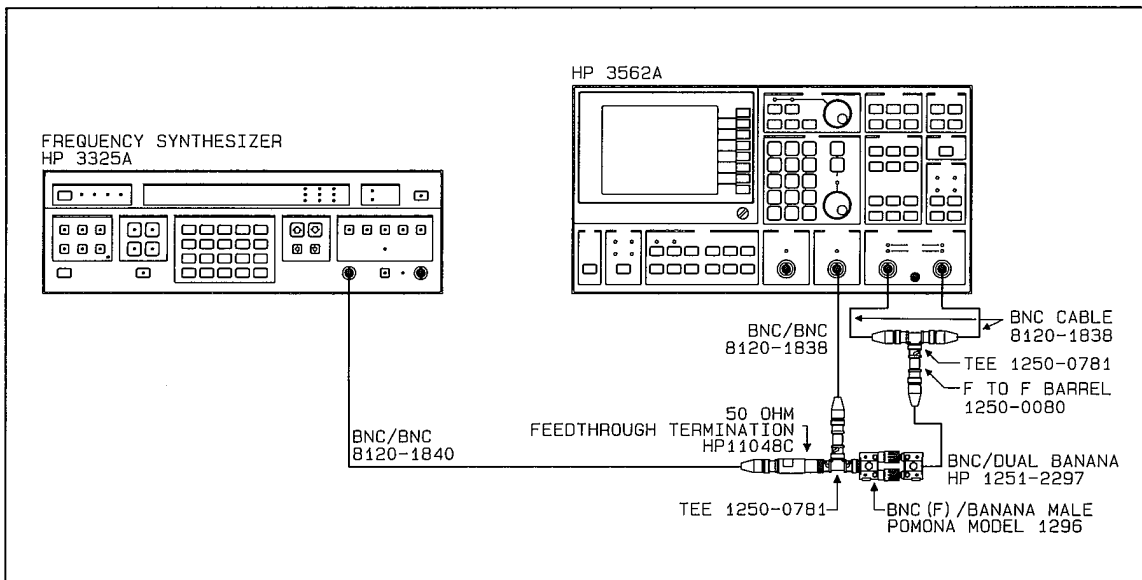


Figure 2-18 Single Channel Phase Accuracy Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-18. Refer to "Initial Equipment Setup", paragraph 2-20, for unspecified parameters.
- B. Set the test instruments initially as follows:

Frequency Synthesizer

| | | |
|-----------|------|-------------|
| Frequency | | 9 kHz |
| Amplitude | | 1 Vrms |
| DC Offset | | 0 Vdc |
| Function | | Square Wave |

C. Press the HP 3562A keys as follows:

| | | | |
|-------------------------|-------|-----------------|-------------------------------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| SELECT MEAS | | POWER SPEC | |
| INPUT COUPLE | | GROUND CHAN1 | |
| | | GROUND CHAN2 | |
| AVG | | 5 | ENTER |
| | | STABLE | |
| | | TIM AV ON | |
| WINDOW | | UNIFRM | |
| SELECT TRIG | | 0 V | |
| MEAS DISP | | FILTRD INPUT | AVR LINEAR SPEC 1 |
| B | | | LINEAR SPEC 2 |
| A & B | | | |
| COORD | | PHASE | |

Table 2-11 Single Channel Phase Accuracy

| Signal Frequency | Trigger Slope | Trigger Type |
|------------------|---------------|--------------|
| 9 kHz | POS | INPUT CHAN 1 |
| 9 kHz | POS | INPUT CHAN 2 |
| 9 kHz | POS | EXTERNAL |
| 9 kHz | NEG | EXTERNAL |
| 99 kHz | POS | INPUT CHAN 1 |
| 99 kHz | POS | INPUT CHAN 2 |
| 99 kHz | POS | EXTERNAL |

D. For each of the frequencies listed in table 2-11 perform steps 1 through 4:

1. Set the frequency Synthesizer as follows:

Frequency To signal frequency in table

2. Press the HP 3562A keys as follows:

SELECT

TRIG To trigger slope in table

. To trigger type in table

START

X To signal frequency in table

3. Record the Ya marker reading on the Performance Test Record for CHAN 1 measured value, BNC shell grounded.

4. Record the Yb marker reading on the Performance Test Record for CHAN 2 measured value, BNC shell grounded.

E. Reverse one of the banana plug connectors so the center conductor of each channel's BNC is grounded.

F. Press the HP 3562A keys as follows:

| | | |
|---------------|-------|--------|
| INPUT | | |
| COUPLE | | FLOAT |
| | | CHAN 1 |
| | | FLOAT |
| | | CHAN 2 |

G. Repeat part D for the BNC center conductors grounded.

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments | None |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards A31 Trigger Board A6 Digital Filter Controller A1 Digital Source |

2-30 INPUT IMPEDANCE

This test measures the input impedance of the HP 3562A as a series resistance and capacitance. The digital multimeter is used to measure the input resistance directly. The input capacitance is then measured by inputting a 100 kHz signal from the frequency synthesizer. This equation is used to calculate the capacitance:

$$C = \left[\left(\frac{V_{in}}{V_c} - 1 \right) \right] 15.9 \text{ pF} - 1.59 \text{ pF}$$

Note

An LCR meter (HP 4261A, HP 4332A) can be used to measure the input capacitance directly.

Specification

Input Resistance (R) = 1 MΩ ± 50 kΩ (5%)

Input Capacitance (C) = <100 pF

Required Test Equipment

| | | |
|-----------------------------|-------|--------------|
| Frequency Synthesizer | | HP 3325A |
| Digital Voltmeter | | HP 3456A |
| 100 kΩ Resistor | | HP 0757-0465 |
| 50Ω feedthrough termination | | HP 11048C |

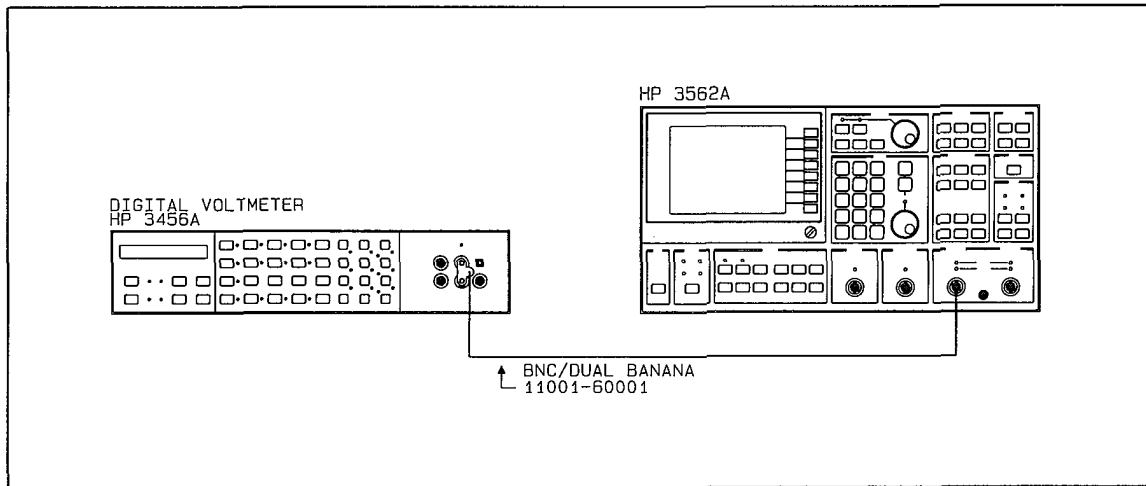


Figure 2-19 Input Resistance Test Setup

Procedure

A. Connect the test instruments as shown in figure 2-19. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set the digital voltmeter initially as follows:

| | | |
|----------|------|------------|
| Function | | 2 WIRE OHM |
| Range | | AUTO |
| Trigger | | INTERNAL |

C. Press the HP 3562A keys as follows:

| | | |
|-------------------------|------|------------------|
| PRESET | | RESET |
| CAL | | SINGLE CAL |
| INPUT COUPLE | | GROUND CHAN 1 |
| | | GROUND CHAN 2 |
| RANGE | | 20 dBVrms |

Table 2-12 Resistance Measurement

| Range Setting | Specification | |
|---------------|----------------|-----------------|
| | Lower Limit | Upper Limit |
| 20 dBVrms | 950 k Ω | 1050 k Ω |
| 0 dBVrms | 950 k Ω | 1050 k Ω |
| -13 dBVrms | 950 k Ω | 1050 k Ω |

D. For each of the range settings listed in table 2-12 perform steps 1 and 2:

1. Press the HP 3562A keys as follows:

RANGE To the range setting in table

2. Record the digital voltmeter reading on the Performance Test Record.

E. Change the BNC input connector to channel 2 and repeat part D.

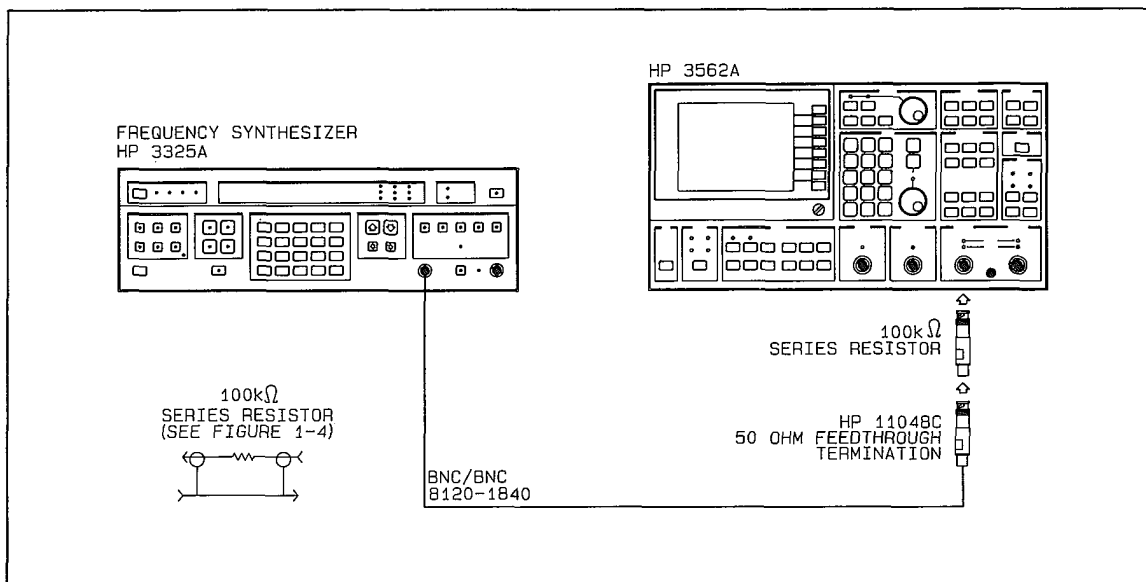


Figure 2-20 Input Capacitance Test Setup

F. Connect the test instruments as shown in figure 2-20.

G. Set the frequency synthesizer initially as follows:

Frequency 100 kHz

Amplitude 1 Vrms

H. Press the HP 3562A keys as follows:

| | | | |
|-------------------------|-------|------------------|--------------------|
| PRESET | | RESET | |
| CAL | | AUTO OFF | |
| AVG | | 16 | ENTER |
| | | STABLE | |
| INPUT COUPLE | | CHAN 1 AC | |
| | | CHAN 2 AC | |
| | | GROUND CHAN 1 | |
| | | GROUND CHAN 2 | |
| RANGE | | 0 dBVrms | |
| START | | | |
| UNITS | | P SPEC UNITS | VOLTS RMS |
| | | | VOLTS |
| COORD | | MAG(LIN) | |
| X | | 100 kHz | |

I. Record the Ya amplitude reading in the Vc position of the Performance Test Record for CHAN 1.

J. Perform steps 1 through 3:

1. Connect the 50Ω feedthrough to channel 2.
2. Press the HP 3562A keys as follows:

B

START

COORD MAG(LIN)

- 3. Record the Yb amplitude reading in the Vc position of the Performance Test Record for CHAN 2.
- K. Remove the 100 kΩ resistor from the signal path and connect the BNC cable with the 50Ω termination directly to the HP 3562A's channel 1 input connector.
- L. Perform steps 1 and 2:
 - 1. Press the HP 3562A keys as follows:
 - A**
 - START**
 - 2. Record the Ya amplitude reading in the Vin position of the Performance Test Record for CHAN 1.
- M. Perform steps 1 through 3:
 - 1. Connect the 50Ω feedthrough to channel 2.
 - 2. Press the HP 3562A keys as follows:
 - B**
 - START**
 - 3. Record the Yb amplitude reading in the Vin position of the Performance Test Record for CHAN 2.
- N. Use the equation given on the Performance Test Record to calculate the input capacitance.

If Test Fails Check:

| | |
|---------------------------------|-----------------------|
| Adjustments | None |
| Troubleshooting Section VIII | A33, A35 Input Boards |

2-31 HARMONIC DISTORTION

This test measures the harmonic distortion generated in the HP 3562A when a full scale input is present.

Specification

The relative amplitude of all harmonics will be at least 80 dB below the fundamental amplitude.

Required Test Equipment

- Low Distortion Oscillator HP 339A
- 600Ω feedthrough termination HP 11095A

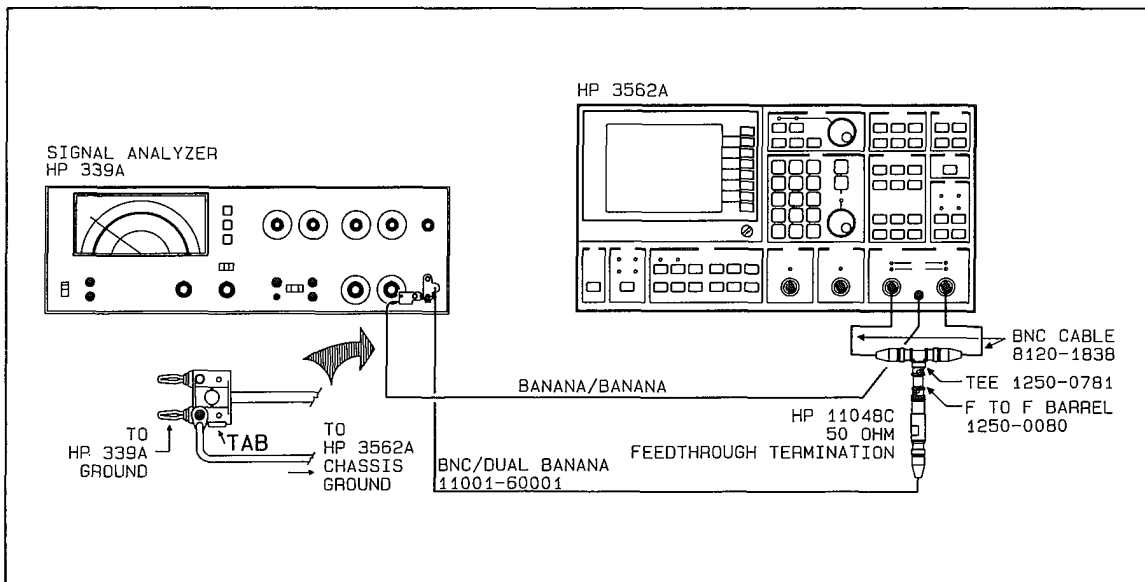


Figure 2-21 Harmonic Distortion Test Setup #1

Procedure

- A. Connect the test instruments as shown in figure 2-21. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set the low distortion oscillator initially as follows:

Frequency 49 kHz
 Amplitude 1 Vrms

C. Press the HP 3562A keys as follows:

PRESET RESET

CAL SINGLE
 CAL

RANGE 0 dBVrms

INPUT COUPLE CHAN 1
 AC

. . . . CHAN 2
 AC

. . . . GROUND
 CHAN 1

. . . . GROUND
 CHAN 2

WINDOW FLAT TOP

UNITS P SPEC VOLTS
 UNITS RMS

. . . . VOLTS

Table 2-13 Harmonic Frequencies

| HP 339A Coarse Frequency | SIGNAL FREQUENCY | Harmonic Number | Harmonic Frequency |
|--------------------------------|---------------------|--------------------|-----------------------|
| 49 kHz | 49500 Hz | 2nd | 99 kHz |
| 32 kHz | 33000 Hz | 3rd | 99 kHz |
| 24 kHz | 24750 Hz | 4th | 99 kHz |
| 19 kHz | 19800 Hz | 5th | 99 kHz |

D. For each of the signal frequencies listed in table 2-13 perform steps 1 through 7:

1. Set the low distortion oscillator as follows:

Frequency To coarse frequency in table

2. Press the HP 3562A keys as follows:

FREQ CENTER
FREQ To signal frequency in
table

AVG AVG OFF

START

SINGLE

X To signal frequency in table

3. Adjust the low distortion oscillator's frequency vernier until it equals the signal frequency.
4. Adjust the low distortion oscillator's amplitude vernier until $Y_a = 0$ dBVrms ± 0.1 dBVrms.
5. Press the HP 3562A keys as follows:

A & B

AVG 4 ENTER

. . . . STABLE

FREQ MAX SPAN

START

X 99 kHz

6. Record the Y_a marker amplitude reading on the Performance Test Record as the harmonic frequency amplitude for channel 1.
7. Record the Y_b marker amplitude reading on the Performance Test Record as the harmonic frequency amplitude for channel 2.

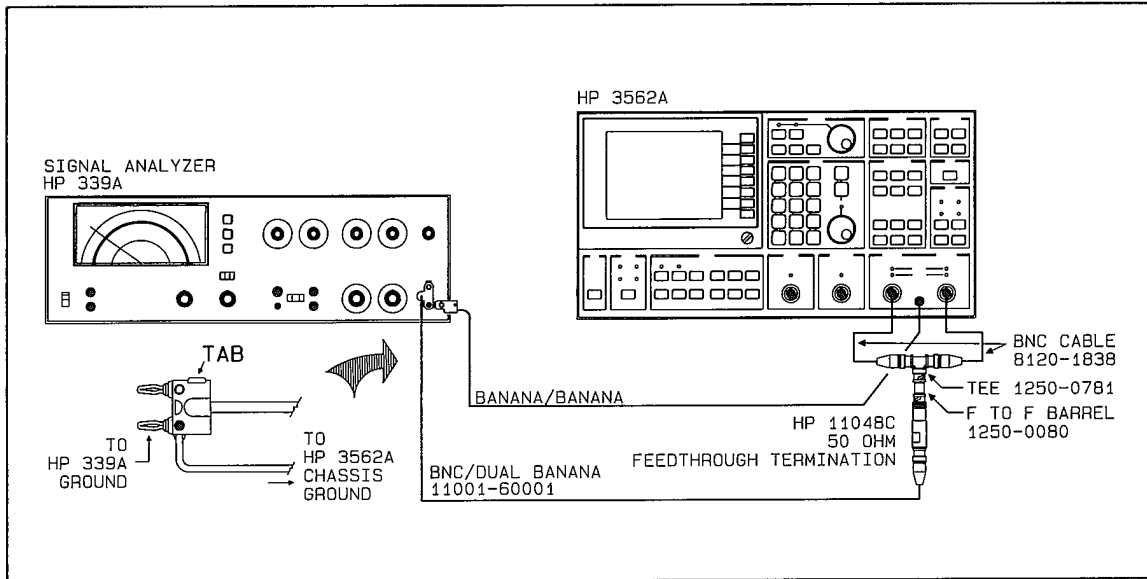


Figure 2-22 Harmonic Distortion Test setup #2

E. For measurement two, connect the test instruments as shown in figure 2-22. The chassis ground cable must go to the ground terminal of the low distortion oscillator.

F. Press the HP 3562A keys as follows:

| | | |
|---------------|------|--------|
| INPUT | | |
| COUPLE | | FLOAT |
| | | CHAN 1 |
| | | FLOAT |
| | | CHAN 2 |

G. Repeat part D for measurement two.

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments Section III | 2nd Pass Gain Adjustment ADC Offset and Reference Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards |

2-32 INTERMODULATION DISTORTION

This test measures the level of the intermodulation distortion products generated within the HP 3562A to the 4th order.

NOTE

The HP 3325A may produce some spurious signals in the 0 to 100 kHz span. Ignore signals at frequencies other than those listed in the tables when performing this test.

Specification

The amplitude of all intermodulation products will be at least 80 dB below the fundamental amplitude.

Required Test Equipment

- | | | |
|----------------------------------|-------|--------------|
| (2) Frequency Synthesizers | | HP 3325A |
| (2) 50Ω feedthrough terminations | | HP 11048C |
| (2) 1 kΩ resistors | | HP 0757-0465 |
| (2) BNC Tee | | HP 1250-0781 |

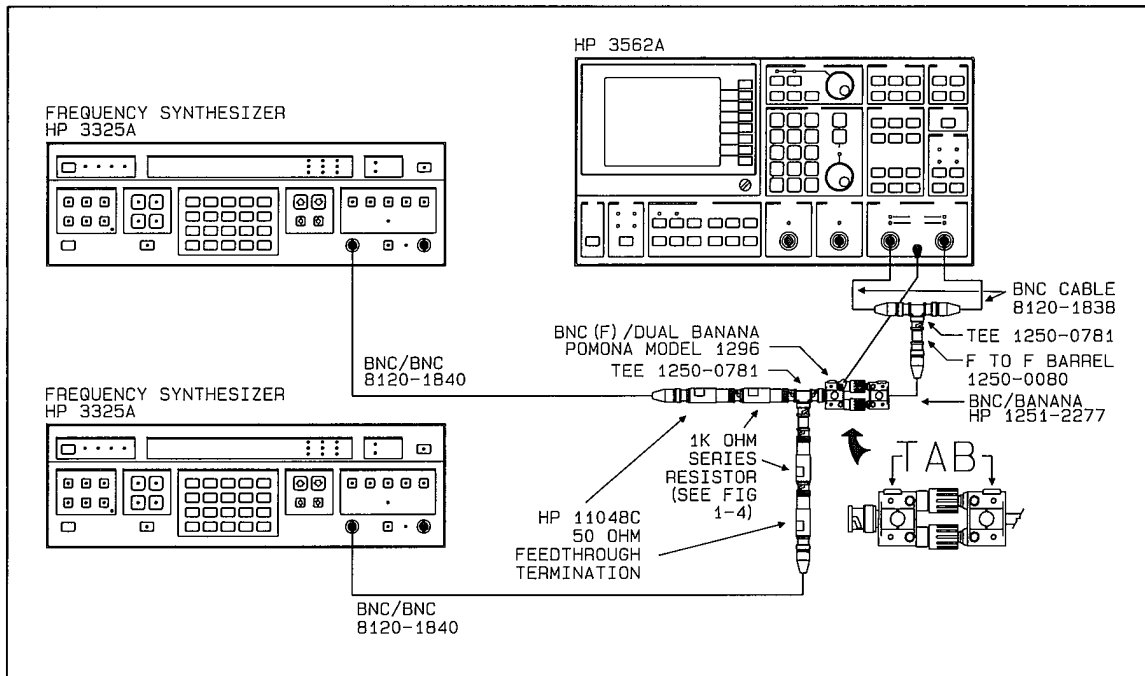


Figure 2-23 Intermodulation Distortion Test Setup #1

Procedure

A. Connect the test instruments as shown in figure 2-23. Keep the connecting cables as short as possible. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set the test instruments initially as follows:

Frequency Synthesizer #1

| | | |
|-----------|------|-----------|
| Frequency | | 20 kHz |
| Amplitude | | 1 Vrms |
| Function | | Sine Wave |

Frequency Synthesizer #2

| | | |
|-----------|------|-----------|
| Frequency | | 26 kHz |
| Amplitude | | 1 Vrms |
| Function | | Sine Wave |

C. Perform steps 1 through 5:

1. Press the HP 3562A keys as follows:

| | | | |
|-------------------------|------|------------------|-------------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| RANGE | | 2 Vrms | |
| INPUT COUPLE | | GROUND CHAN 1 | |
| | | GROUND CHAN 2 | |
| WINDOW | | FLAT TOP | |
| FREQ | | CENTER FREQ | 20 kHz |
| UNITS | | P SPEC UNITS | VOLTS RMS |
| | | | VOLTS |
| A & B | | | |
| X | | 20 kHz | |

- 2. Adjust the amplitude of frequency synthesizer #1 until Ya=0 dBVrms ± 50 mdB.
- 3. Press the HP 3562A keys as follows:

X 26 kHz

- 4. Adjust the amplitude of frequency synthesizer #2 until Ya=0 dBVrms ± 50 mdB.
- 5. Press the HP 3562A keys as follows:

AVG 16 ENTER

. . . . STABLE

SCALE Y FIXD
SCALE -100, .1 dB

Table 2-14 Intermodulation Distortion Measurement One

| Fundamental Frequencies | | Harmonic Frequency |
|-------------------------|--------|--------------------|
| F1 | F2 | |
| 20 kHz | 26 kHz | 6 kHz |
| 20 kHz | 26 kHz | 14 kHz |
| 20 kHz | 26 kHz | 12 kHz |
| 20 kHz | 26 kHz | 8 kHz |

- D. For each of the harmonic frequencies listed in table 2-14 perform steps 1 through 3:

- 1. Press the HP 3562A keys as follows:

FREQ CENTER FREQ To harmonic frequency
in table

START

X To harmonic frequency in table

- 2. If the Ya marker reading is less than or equal to -80 dBVrms, check PASS on the Performance Test Record for measurement one, channel 1 with the BNC shell grounded.
- 3. If the Yb marker reading is less than or equal to -80 dBVrms, check PASS on the Performance Test Record for measurement one, channel 2 with the BNC shell grounded.

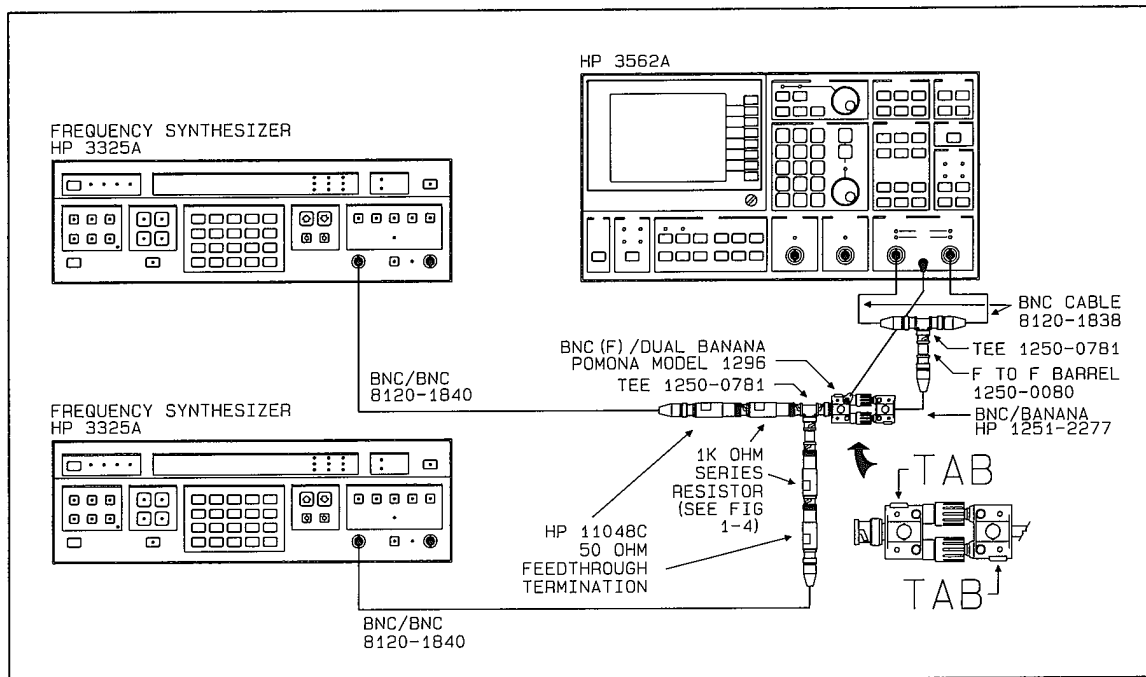


Figure 2-24 Intermodulation Distortion Test Setup #2

E. Perform steps 1 and 2:

1. Connect the test instruments as shown in figure 2-24 so the center conductor of each channel's BNC is grounded.
2. Press the HP 3562A keys as follows:

| | | |
|---------------|------|--------|
| INPUT | | |
| COUPLE | | FLOAT |
| | | CHAN 1 |
| | | FLOAT |
| | | CHAN 2 |

F. For each of the harmonic frequencies listed in table 2-14 perform steps 1 through 3:

1. Press the HP 3562A keys as follows:

FREQ CENTER FREQ To harmonic frequency
in table

START

X To harmonic frequency in table

2. If the Ya marker reading is less than or equal to -80 dBVrms, check PASS on the Performance Test Record for measurement one, channel 1 with the BNC center conductor grounded.

3. If the Yb marker reading is less than or equal to -80 dBVrms, check PASS on the Performance Test Record for measurement one, channel 2 with the BNC center conductor grounded.

G. Connect the test instruments as shown in figure 2-23.

H. Set the test instruments as follows:

Frequency Synthesizer #1

Frequency 89 kHz

Frequency Synthesizer #2

Frequency 99 kHz

I. Perform steps 1 through 5:

1. Press the HP 3562A keys as follows:

AVG AVG OFF

FREQ CENTER FREQ **89** kHz

START

X **89** kHz

2. Adjust the amplitude of frequency synthesizer #1 until $Y_a = 0$ dB ± 50 mdB.

3. Press the HP 3562A keys as follows:

FREQ CENTER FREQ **99** kHz

X **99** kHz

4. Adjust the amplitude of frequency synthesizer #2 until $Y_a = 0 \text{ dB} \pm 50 \text{ mdB}$.
5. Press the HP 3562A keys as follows:

AVG **STABLE**

Table 2-15 Intermodulation Distortion Measurement Two

| Fundamental Frequencies | | Harmonic Frequency |
|-------------------------|--------|--------------------|
| F1 | F2 | |
| 89 kHz | 99 kHz | 10 kHz |
| 89 kHz | 99 kHz | 79 kHz |
| 89 kHz | 99 kHz | 20 kHz |
| 89 kHz | 99 kHz | 69 kHz |

- J. For each of the harmonic frequencies listed in table 2-15 perform steps 1 through 3:

1. Press the HP 3562A keys as follows:

FREQ **CENTER FREQ** To harmonic frequency in table

START

X To harmonic frequency in table

2. If the Y_a marker reading is less than or equal to -80 dBVrms , check PASS on the Performance Test Record for measurement two, channel 1 with the BNC shell floating.
3. If the Y_b marker reading is less than or equal to -80 dBVrms , check PASS on the Performance Test Record for measurement two, channel 2 with the BNC shell floating.

- K. Connect the test instruments as shown in figure 2-24 so the center conductor of each channel's BNC is grounded.

- L. For each of the harmonic frequencies listed in table 2-15 perform steps 1 through 3:

1. Press the HP 3562A keys as follows:

FREQ **CENTER FREQ** To harmonic frequency in table

START

X To harmonic frequency in table

2. If the Ya marker reading is less than or equal to -80 dBVrms, check PASS on the Performance Test Record for measurement two, channel 1 with the BNC center conductor grounded.
3. If the Yb marker reading is less than or equal to -80 dBVrms, check PASS on the Performance Test Record for measurement two, channel 2 with the BNC center conductor grounded.

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments Section III | 2nd Pass Gain Adjustment ADC Offset and Reference Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter Boards |

2-33 NOISE AND SPURIOUS SIGNAL LEVEL

This test measures the level of the noise floor and any spurious signals generated within the HP 3562A.

Specification

When the input is terminated with a 50Ω load, the amplitude of all spurious signals must be at least 80 dB below the range setting. When using a flat top window and a 50Ω load, the average noise level must be less than:

| Frequency | Noise Level |
|------------------|-------------------------------------|
| 20 Hz to 1 kHz | $-134 \text{ dBV}/\sqrt{\text{Hz}}$ |
| 1 kHz to 100 kHz | $-144 \text{ dBV}/\sqrt{\text{Hz}}$ |

Required Test Equipment

(2) 50Ω feedthrough terminations HP 11048C

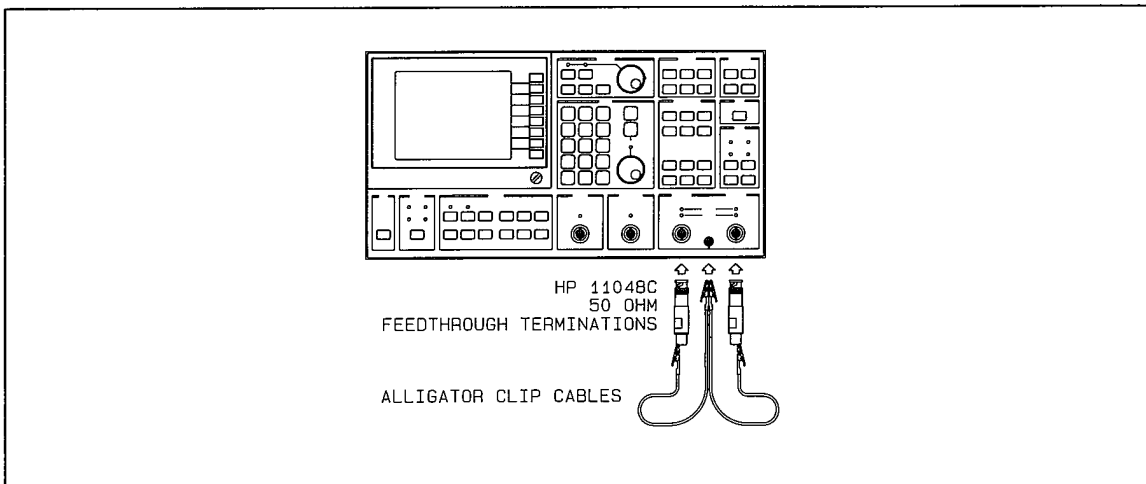


Figure 2-25 Noise and Spurious Signal Level Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-25. Keep the leads from the feedthrough terminations to chassis ground as short as possible.
- B. Press the HP 3562A keys as follows:

| | | | | |
|-------------------------|-------|-----------------|-------|--------------|
| PRESET | | RESET | | |
| CAL | | SINGLE CAL | | |
| RANGE | | -51 dBVrms | | |
| INPUT COUPLE | | CHAN 1 AC | | |
| | | CHAN 2 AC | | |
| FREQ | | FREQ SPAN | | 1 kHz |
| | | START FREQ | | 20 Hz |
| AVG | | 20 | | ENTER |
| | | STABLE | | |
| WINDOW | | UNIFORM | | |
| UNITS | | P SPEC UNITS | | VOLTS RMS |
| | | | | VOLTS |

- C. Perform steps 1 through 4:

- 1. Press the HP 3562A keys as follows:

| | | |
|------------------------|-------|-----------------|
| START | | |
| SCALE | | Y AUTO SCALE |
| SPCL MARKER | | MRKR → PEAK |

- 2. If the Ya marker reading is less than or equal to -131 dBVrms, check PASS on the Performance Test Record for CHAN 1.

3. Press the HP 3562A keys as follows:

B

SCALE Y AUTO
SCALE

SPCL
MARKER MRKR →
PEAK

4. If the Yb marker reading is less than or equal to -131 dBVrms, check PASS on the Performance Test Record for CHAN 2.

Table 2-16 Spurious Signals

| Start Frequency | Frequency Span | Specification |
|-----------------|----------------|-----------------|
| 20 Hz | 1 kHz | ≤ -131 dBV |
| 1 kHz | 10 kHz | ≤ -131 dBV |
| 10 kHz | 10 kHz | ≤ -131 dBV |
| 20 kHz | 10 kHz | ≤ -131 dBV |
| 30 kHz | 10 kHz | ≤ -131 dBV |
| 40 kHz | 10 kHz | ≤ -131 dBV |
| 50 kHz | 10 kHz | ≤ -131 dBV |
| 60 kHz | 10 kHz | ≤ -131 dBV |
| 70 kHz | 10 kHz | ≤ -131 dBV |
| 80 kHz | 10 kHz | ≤ -131 dBV |
| 90 kHz | 10 kHz | ≤ -131 dBV |

D. For the rest of the start frequencies in table 2-16 perform steps 1 through 4:

1. Press the HP 3562A keys as follows:

FREQ START FREQ To start frequency in table
. . . . FREQ SPAN To frequency span in table

A

START

SPCL

MARKER MRKR →
PEAK

2. If the Ya marker reading is less than or equal to -131 dBVrms, check PASS on the Performance Test Record for CHAN 1.
3. Press the HP 3562A keys as follows:

B

SPCL

MARKER MRKR →
PEAK

4. If the Yb marker reading is less than or equal to -131 dBVrms, check PASS on the Performance Test Record for CHAN 2.

Table 2-17 Noise Level

| Start Frequency | Frequency Span | Specification |
|-----------------|----------------|-------------------------------------|
| 20 Hz | 1 kHz | ≤ -134 dBV/ $\sqrt{\text{Hz}}$ |
| 1 kHz | 50 kHz | ≤ -144 dBV/ $\sqrt{\text{Hz}}$ |
| 50 kHz | 50 kHz | ≤ -144 dBV/ $\sqrt{\text{Hz}}$ |

- E. Press the HP 3562A keys as follows:

WINDOW FLAT TOP

UNITS P SPEC $V/\sqrt{\text{Hz}}$
UNITS

- F. For each of the start frequencies listed in table 2-17 perform steps 1 through 5:

1. Press the HP 3562A keys as follows:

FREQ START FREQ To start frequency in table

. . . . FREQ SPAN To frequency span in table

START

- When the average is complete, press the HP 3562A keys as follows:

A

SPCL
MARKER MRKR →
 PEAK

- If the Ya marker reading is less than or equal to the specification, check PASS on the Performance Test Record for CHAN 1.
- Press the HP 3562A keys as follows:

B

SPCL
MARKER MRKR →
 PEAK

- If the Yb marker reading is less than or equal to the specification, check PASS on the Performance Test Record for CHAN 2.

If Test Fails Check:

| | |
|--------------------------------|--|
| Adjustments Section III | 2nd Pass Gain Adjustment ADC Offset and Reference Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A32, A34 Analog Digital Converter A5 Digital Filter A4 Local Oscillator |

2-34 CROSS TALK

The cross talk test measures the amount of energy in one channel that has been coupled across from the other channel. This is accomplished by placing a high signal level on one channel and then measuring the relative signal amplitude on the other channel.

Specification

When a 50 Ω termination is used, the cross talk between channels will be at least 140 dB below the input signal level.

Required Test Equipment

| | |
|---|-----------|
| Frequency Synthesizer | HP 3325A |
| 50 Ω feedthrough termination | HP 11048C |

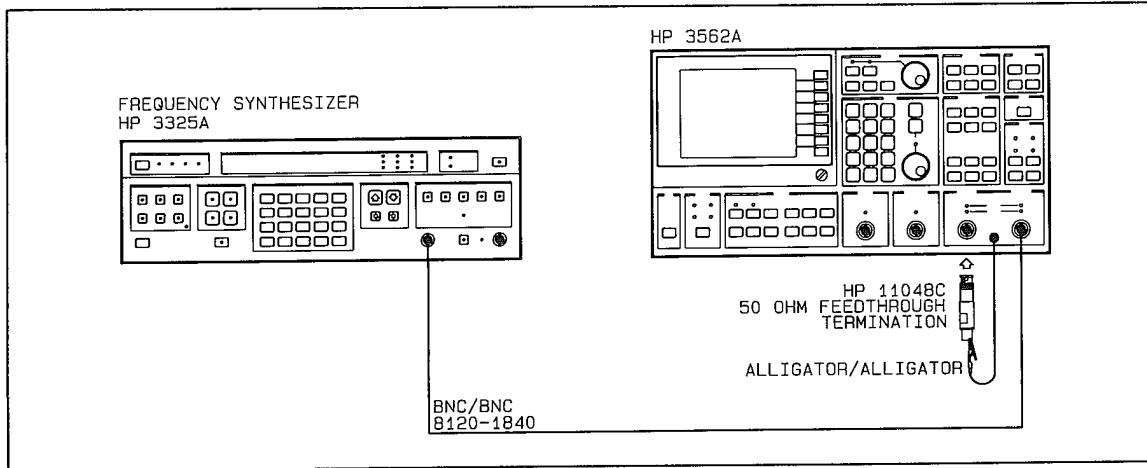


Figure 2-26 Cross Talk Channel 1 Test Setup

Procedure

A. Connect the test instruments as shown in figure 2-26. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set the frequency synthesizer as follows:

- Amplitude 14 Vrms
- High Voltage
- Output ON
- Frequency 100 kHz
- Function Sine Wave

C. Press the HP 3562A keys as follows:

- PRESET** RESET
- CAL** SINGLE CAL
- FREQ** CENTER FREQ **99 kHz**
- WINDOW** FLAT TOP
- AVG** **16** ENTER
- STABLE
- RANGE** AUTO 1 AUTO 2
- UP & DWN UP & DWN
- START**
- A & B**
- X** 100 kHz

SCALE Y FIXD
SCALE -140,23 dB

B
Y

D. Using the marker knob, move the Y marker to the center of the X marker dot and press the HP 3562A keys as follows:

**HOLD Y
UPPER**

A

E. Using the marker knob, move the Y marker to the center of the X marker dot.

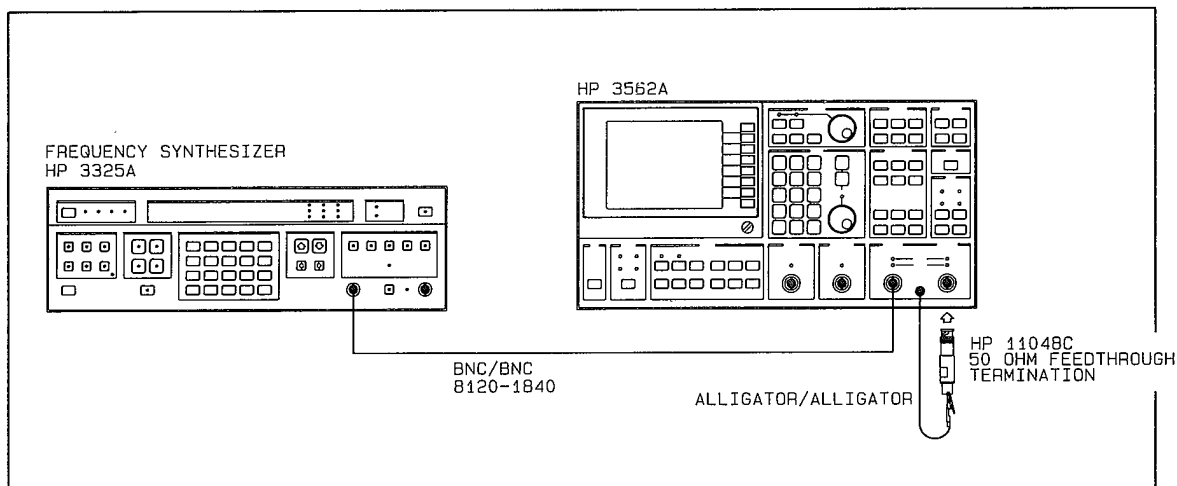


Figure 2-27 Cross Talk Channel 2 Test Setup

F. If the delta Y is greater than or equal to 140 dB, check PASS on the Performance Test Record for channel 1.

G. Connect the test instruments as shown in figure 2-27.

H. Press the HP 3562A keys as follows:

Y OFF

START

A & B

X 100 kHz

A

Y

- I. Using the marker knob, move the Y marker to the center of the X marker dot and press the HP 3562A keys as follows:

**HOLD Y
UPPER**

B

- J. Using the marker knob, move the Y marker the center of the X marker dot.
- K. If the delta Y is greater than or equal to 140 dB, check PASS on the Performance Test Record for channel 2.

If Test Fails Check:

| | |
|---------------------------------|-----------------------|
| Adjustments | None |
| Troubleshooting Section VIII | A33, A35 Input Boards |

2-35 COMMON MODE REJECTION

This test measures the capability of the 3562A to ignore a signal which appears simultaneously and in phase at the high and low input of a single channel.

Specification

When a common mode signal is input to a single channel, the relative value compared to the amplitude of the input single will be:

| Frequency | Specification |
|-----------------|---------------|
| 0 Hz to 66 Hz | ≤80 dB |
| 66 Hz to 500 Hz | ≤65 dB |

Required Test Equipment

| | | |
|-----------------------|---------|----------------|
| Frequency Synthesizer | | HP 3325A |
| Common Mode Cable | | HP 03562-61620 |

Procedure

- A. Connect the test instruments as shown in figure 2-28. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.
- B. Set the frequency synthesizer as follows:

| | | |
|--------------|---------|-----------|
| Function | | Sine Wave |
| High Voltage | | |
| Output | | ON |

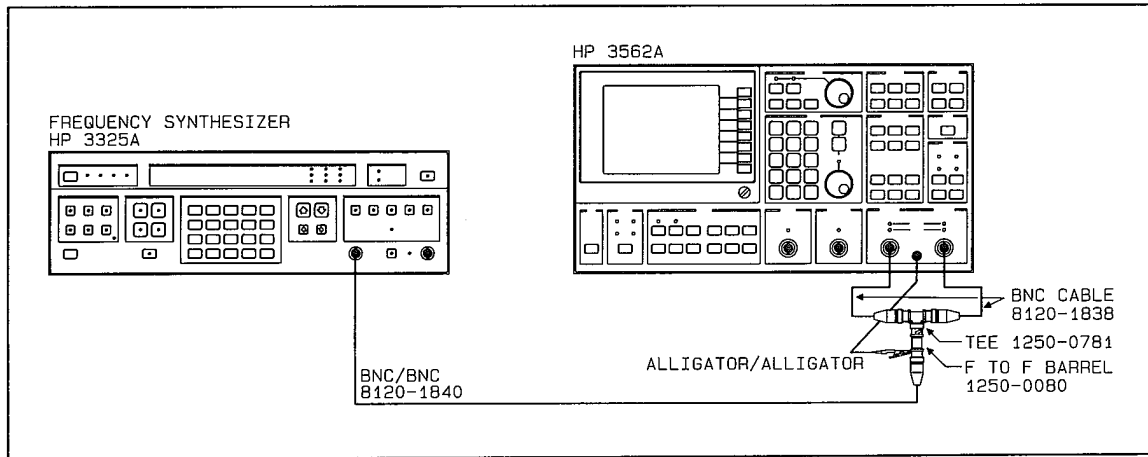


Figure 2-28 Common Mode Rejection Test Setup #1

C. Press the HP 3562A keys as follows:

PRESET **RESET**

CAL **SINGLE CAL**

AVG **16** **ENTER**

. **STABLE**

WINDOW **FLAT TOP**

A & B

UNITS **P SPEC UNITS** **VOLTS RMS**

. **VOLTS**

Table 2-18 Common Mode Rejection

| Signal Amplitude | Signal Frequency | Range Setting #1 | Range Setting #2 | Specification |
|------------------|------------------|------------------|------------------|---------------|
| 5.680 Vrms | 66 Hz | 16 dBVrms | -8 dBVrms | ≤80 dB |
| 3.413 Vrms | 500 Hz | 11 dBVrms | -12 dBVrms | ≤65 dB |

D. For each of the frequencies listed in table 2-18 perform steps 1 through 9:

1. Set the Frequency Synthesizer as follows:

Amplitude To signal amplitude in table

Frequency To signal frequency in table

2. Press the HP 3562A keys as follows:

FREQ CENTER FREQ To signal frequency in table

RANGE To range setting #1 in table

START

SPCL MARKER MRKR →
PEAK

3. Record the Ya marker amplitude reading on the Performance Test Record as the first measurement for CHAN 1.

4. Record the Yb marker amplitude reading on the Performance Test Record as the first measurement for CHAN 2.

5. Connect the test instruments as shown in figure 2-29.

6. Press the HP 3562A keys as follows:

RANGE To range setting #2 in table

START

SCALE Y AUTO
SCALE

X To signal frequency in table

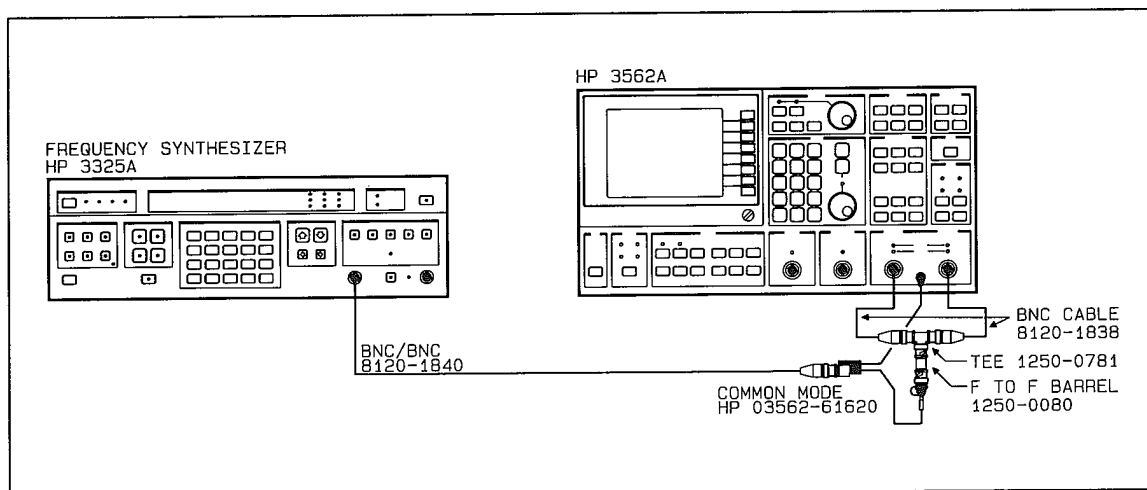


Figure 2-29 Common Mode Rejection Test Setup #2

7. When the average is complete, record the Ya amplitude reading on the Performance Test Record as the second measurement for CHAN 1.
8. Record the Yb amplitude reading on the Performance Test Record as the second measurement for CHAN 2.
9. Calculate the relative value for both channels:

$$\begin{matrix} \text{First} \\ \text{Measurement} \end{matrix} - \begin{matrix} \text{Second} \\ \text{Measurement} \end{matrix} = \text{Relative Value}$$

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments Section III | Input dc Offset Adjustment Calibrator Adjustment |
| Troubleshooting Section VII | A33, A35 Input Boards A30 Analog Source |

2-36 EXTERNAL REFERENCE TEST

This test determines if the external reference input will lock on to an external signal that is within the specified range.

Specification

The HP 3562A will lock to external signals of 1, 2, 5, and 10 MHz ±0.01%. The amplitude of the signal must be between 0 dBm and +20 dBm.

Required Test Equipment

Frequency Synthesizer HP 3325A

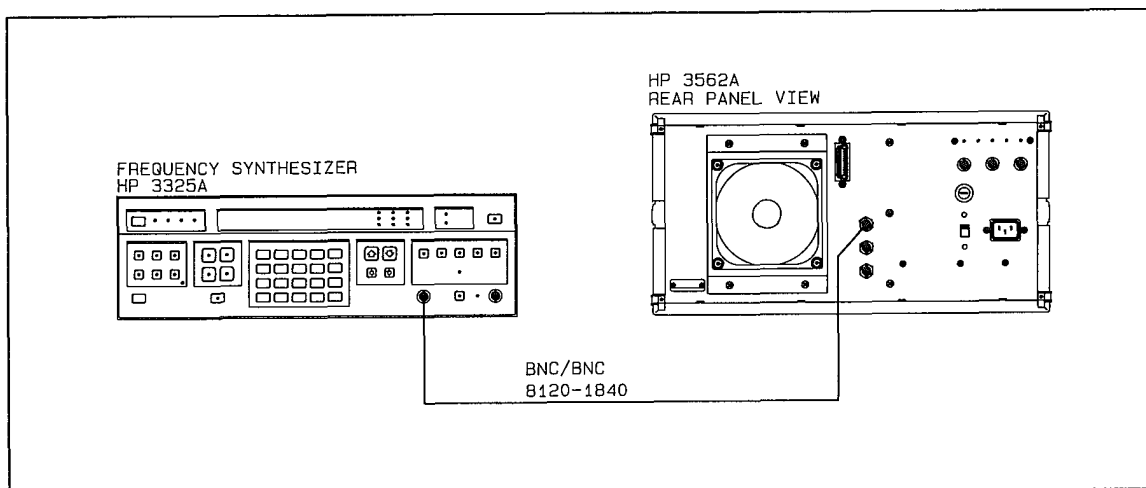


Figure 2-30 External Reference Test Setup

Procedure

A. Connect the HP 3562A as shown in figure 2-30. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set frequency synthesizer as follows:

| | |
|---------------------|-----------|
| Frequency | 1.000 MHz |
| Amplitude | 0 dBm |
| Function | Sine Wave |

C. Press the HP 3562A keys as follows:

| | |
|-------------------------|---------------|
| PRESET | RESET |
| CAL | SINGLE CAL |

D. Perform steps 1 through 3:

1. Press "FREQ" on the 3325A.
2. Using the modify arrows on the 3325A, slowly decrease the frequency in 100 Hz steps until the 'Source Not Locked' message is displayed.
3. Record the frequency value on the Performance Test Record.

E. Set the Frequency Synthesizer as follows:

| | |
|---------------------|------------|
| Frequency | 10.000 MHz |
|---------------------|------------|

F. Perform steps 1 through 4:

1. Press "**PRESET**" on the HP 3562A.
2. Press "FREQ" on the 3325A.
3. Using the modify arros on the 3325A, slowly increase the frequency in 1 kHz steps until the 'Source Not Locked' message is displayed.
4. Record the frequency value on the Performance Test Record.

If Test Fails Check:

| | |
|---------------------------------|--------------------------------|
| Adjustments Section III | 20.48 MHz Reference Adjustment |
| Troubleshooting Section VIII | A31 Trigger Board |

2-37 SOURCE RESIDUAL OFFSET

This test measures the level of residual offset generated by the source at the 0V offset setting.

Specification

The source residual offset will be no more than 10 mV at the 0V offset setting.

Required Test Equipment

Digital Voltmeter HP 3456A

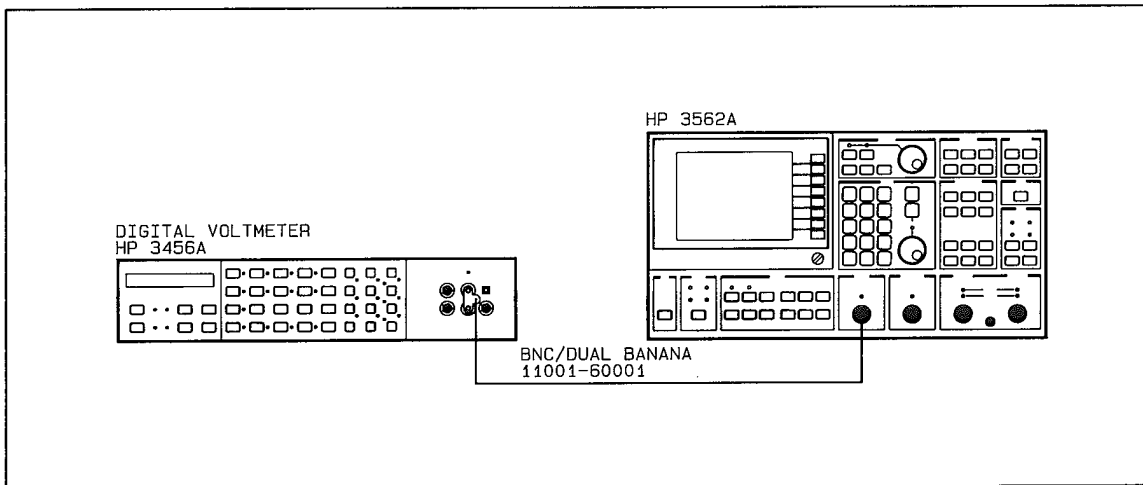


Figure 2-31 Source Residual Offset Test Setup

Procedure

A. Connect the test instruments as shown in figure 2-31. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set the digital voltmeter as follows:

| | | |
|----------|-----------|----------|
| Function | | dc (≡V) |
| Trigger | | Internal |
| Range | | Auto |

C. Press the HP 3562A keys as follows:

| | | | |
|---------------|-----------|------------------------|----------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| SOURCE | | SOURCE LEVEL | 1 V |
| | | FIXED SINE | 100 kHz |

D. Record the digital voltmeter reading on the Performance Test Record for the 1V setting.

E. Press the HP 3562A keys as follows:

SOURCE **SOURCE LEVEL** **5 V**

F. Record the digital voltmeter reading on the Performance Test Record for the 5V setting.

If Test Fails Check:

| | |
|---------------------------------|-------------------------|
| Adjustments | None |
| Troubleshooting Section VIII | A30 Analog Source Board |

2-38 SOURCE AMPLITUDE ACCURACY AND FLATNESS

This test measures the amplitude accuracy and flatness of the HP 3562A source.

Specification

The amplitude reading will not deviate from the source amplitude setting by more than 1 dB (12.2%) when terminated into 1 MΩ for frequencies between 0 Hz and 65 kHz, and +1 dB, -1.5 dB for frequencies between 65 kHz and 100 kHz.

Procedure

A. Connect the HP 3562A source to channel 1.

B. Press the HP 3562A keys as follows:

| | | | |
|---------------------|---------|----------------------|-----------------------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| INPUT COUPLE | | GROUND CHAN 1 | |
| RANGE | | 5 Vpk | |
| MEAS MODE | | SWEPT SINE | LINEAR SWEEP |
| SOURCE | | ON | |
| | | SOURCE LEVEL | 4.47 V |

UNITS P SPEC UNITS VOLTS RMS

FREQ STOP FREQ VOLTS
 65 kHz

START

C. When the sweep is complete perform steps 1 and 2:

1. Press the HP 3562A keys as follows:

SCALE Y FIXD SCALE **9,11 dB**

2. If the trace is between the 9 dB and the 11 dB limits, check PASS on the Performance Test Record for the 0 to 65 kHz span.

D. Press the HP 3562A keys as follows:

FREQ START FREQ **65 kHz**

START

E. When the sweep is complete perform steps 1 and 2:

1. Press the HP 3562A keys as follows:

SCALE Y FIXD SCALE **8.5, 11 dB**

2. If the trace is between the 8.5 dB and the 11 dB limits, check PASS on the Performance Test Record for the 65 kHz to 100 kHz span.

If Test Fails Check:

Troubleshooting A30 Analog Source Board
 Section VIII

2-39 SOURCE OUTPUT RESISTANCE CHARACTERIZATION (Optional)

This test measures the output impedance of the analog source as a series resistance.

Specification

The output impedance of the source is 50 Ω Nominal

Required Test Equipment

50 Ω feedthrough termination HP 11048C
 BNC cable HP 11170A

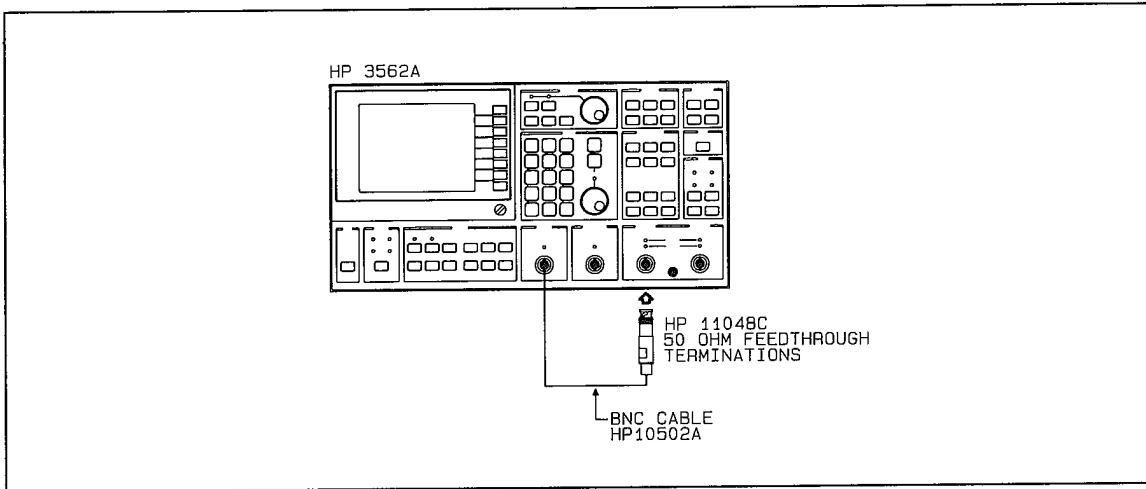


Figure 2-32 Source Output Resistance Test Setup

Procedure

- A. Connect the test instruments as shown in figure 2-32.
- B. Press the HP 3562A keys as follows:

| | | | |
|---------------------|-------|----------------------|---------------------------|
| PRESET | | RESET | |
| CAL | | SINGLE CAL | |
| INPUT COUPLE | | GROUND CHAN 1 | CHAN 1 AC |
| MEAS MODE | | SWEPT SINE | LINEAR SWEEP |
| SOURCE | | SOURCE LEVEL | 1 Vrms |
| START | | | |
| COORD | | MAG (LIN) | |
| UNITS | | SWEPT UNITS | VOLTS |
| SCALE | | Y AUTO SCALE | |

C. When the sweep is complete press the HP 3562A keys as follows:

SAVE
RECALL SAVE DATA # 1 ENTER

D. Remove the 50Ω termination from the signal path and connect the output of the source directly to channel 1.

E. Press the HP 3562A keys as follows:

START

F. When the sweep is complete press the HP 3562A keys as follows:

MATH SUB SAVED 1
 DIV SAVED 1
 MPY 50, 0

2-40 SOURCE DISTORTION

This test measures the level of any spurious signals generated by the HP 3562A source.

Specification

When the source is set between dc and 10 kHz, the distortion will be at least 60 dB below the signal level. When the source is set between 10 kHz and 100 kHz, the distortion will be at least 40 dB below the signal level.

Required Test Equipment

None

Procedure

A. Connect the HP 3562A source to channel 1.

B. Press the HP 3562A keys as follows:

PRESET RESET
CAL SINGLE
 CAL
INPUT
COUPLE CHAN 1
 AC
 GROUND
 CHAN 1


```

WINDOW  . . . .  FLAT TOP

AVG      . . . .  4          . . . .  ENTER

          . . . .  STABLE

SCALE   . . . .  X FIXD
          . . . .  SCALE      . . . .  .375, 100 kHz
    
```

Table 2-19 Source Distortion

| Range Setting | Source Amplitude | Source Frequency | Delta Y Value |
|---------------|------------------|------------------|---------------|
| 25 mVpk | 25 mVpk | 10 kHz | 60 dB |
| 5 Vpk | 5 Vpk | 10 kHz | 60 dB |
| 25 mVpk | 25 mVpk | 99 kHz | 40 dB |
| 5 Vpk | 5 Vpk | 99 kHz | 40 dB |

C. For each of the range settings listed in table 2-19 perform steps 1 through 5:

1. Press the HP 3562A keys as follows:

Y OFF

RANGE To range setting in table

SOURCE **SOURCE LEVEL** To source amplitude in table

. . . . **FIXED SINE** To source frequency in table

START

SCALE **Y AUTO SCALE**

SPCL MARKER **MRKR → PEAK**

Y

2. Using the marker knob, move the Y marker to the center of the X marker dot.

3. Press the HP 3562A keys as follows:

Y **HOLD Y UPPER**

4. Using the marker knob, move the Y marker until the delta Y reading equals the delta Y value in the table.
5. If there is no distortion above the lower Y marker line, check PASS on the Performance Test Record.

If Test Fails Check:

| | |
|--------------------------------|--|
| Adjustments Section III | Source dc Offset Adjustment |
| Troubleshooting Section VII | A30 Analog Source Board A4 Local Oscillator Board |

2-41 SOURCE ENERGY MEASUREMENT

This test measures the in-band energy of the HP 3562A noise source using the power marker function of the HP 3562A and a true rms voltmeter.

Specification

The percentage in-band energy of the random noise will be at least 70%. The percentage in-band energy of the chirp will be at least 85%.

Required Test Equipment

| | | |
|-------------------|------|--------------|
| Digital Voltmeter | | HP 3456A |
| BNC Tee | | HP 1250-0781 |

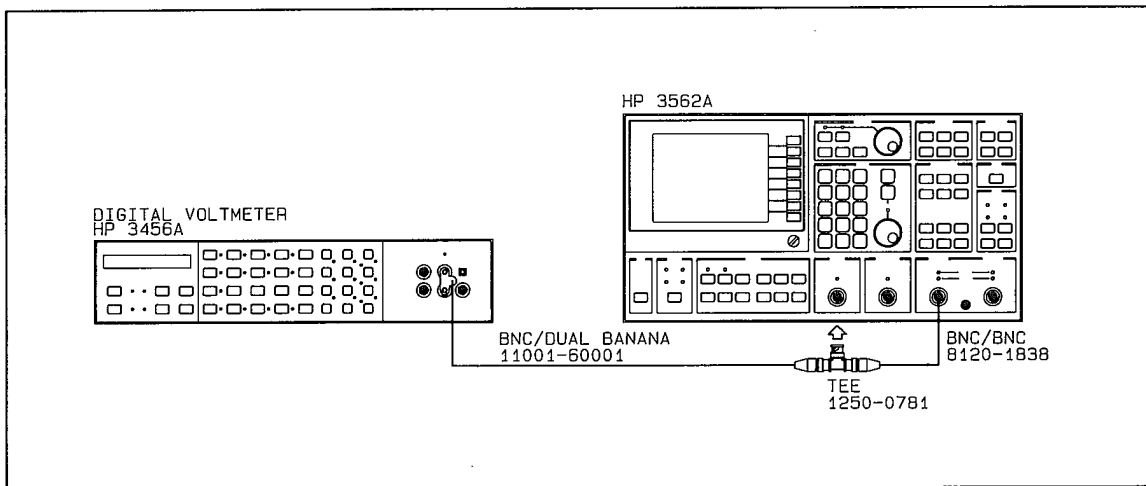


Figure 2-33 Source Energy Measurement Test Setup

Procedure

A. Connect the test instruments as shown in figure 2-33. Refer to "Initial Equipment Setup," paragraph 2-20, for unspecified parameters.

B. Set the test instruments initially as follows:

Digital Voltmeter

Function ac V (~V)
 Trigger Internal

C. Press the HP 3562A keys as follows:

PRESET RESET

CAL SINGLE
 CAL

**INPUT
 COUPLE** GROUND
 CHAN 1

WINDOW UNIFRM (NONE)

RANGE 1 Vrms

SOURCE SOURCE LEVEL 1 Vrms

FREQ FREQ SPAN 1 kHz
 CENTER FREQ 5 kHz

AVG **160** ENTER
 STABLE

START

UNITS P SPEC VOLTS
 UNITS RMS
 VOLTS

COORD MAG(LIN)

**SPCL
 MARKER** POWER

D. Perform steps 1 through 3:

1. Take at least 160 averages by pressing the HP 3456A keys as follows:

MATH

2

**RDGS
STORE**

2. After the "RDGS STORE" annunciator turns off, press the HP 3456A keys as follows:

HOLD

**RDGS
STORE**

RECALL

0

3. Record the voltmeter average on the Performance Test Record.

E. Record the HP 3562A power measurement on the Performance Test Record.

F. Press the HP 3562A keys as follows:

SOURCE **PRIO DC CHIRP**

**SELECT
TRIG** **SOURCE
TRIG**

START

**SPCL
MARKER** **POWER**

G. Repeat parts D and E.

H. The percentage in-band energy for random noise and chirp are calculated using the following formula:

$$\frac{\sqrt{\text{HP 3562A Reading}}}{\text{Voltmeter Reading}} \times 100 = \text{percentage in-band energy}$$

If Test Fails Check:

| | |
|--------------------------------|---|
| Adjustments | None |
| Troubleshooting Section VII | A30 Analog Source Board A1 Digital Source Board A4 Local Oscillator Board |

2-42 PERFORMANCE TEST RECORD

| | |
|----------------|------|
| 2-21 Self Test | PASS |
|----------------|------|

| 2-22 DC Offset | | | |
|------------------|----------------|--------|---------------|
| Range Setting | Measured Value | | Specification |
| | CHAN 1 | CHAN 2 | |
| 7 dBV | | | < -23 dBV |
| -35 dBV | | | < -65 dBV |
| -51 dBV | | | < -71 dBV |

| 2-23 Amplitude Accuracy and Flatness Measurement One | | | | | |
|---|------------------|---------------|-------------|----------------|--------|
| BNC shell grounded | | | | | |
| Range Setting | Signal Frequency | Specification | | Measured Value | |
| | | Lower Limit | Upper Limit | CHAN 1 | CHAN 2 |
| 9 dBV | 1 kHz | 8.849 dBV | 9.151 dBV | | |
| 9 dBV | 99 kHz | 8.849 dBV | 9.151 dBV | | |
| -13 dBV | 1 kHz | -13.15 dBV | -12.85 dBV | | |
| -13 dBV | 50 kHz | -13.15 dBV | -12.85 dBV | | |
| -13 dBV | 90 kHz | -13.15 dBV | -12.85 dBV | | |
| -13 dBV | 99 kHz | -13.15 dBV | -12.85 dBV | | |
| -23 dBV | 1 kHz | -23.15 dBV | -22.85 dBV | | |
| -23 dBV | 99 kHz | -23.15 dBV | -22.85 dBV | | |
| -26 dBV | 1 kHz | -26.15 dBV | -25.85 dBV | | |
| -21 dBV | 1 kHz | -21.15 dBV | -20.85 dBV | | |
| -17 dBV | 1 kHz | -17.15 dBV | -16.85 dBV | | |
| -14 dBV | 1 kHz | -14.15 dBV | -13.85 dBV | | |
| -11 dBV | 1 kHz | -11.15 dBV | -10.85 dBV | | |
| 2-23 Amplitude Accuracy and Flatness Measurement Two | | | | | |
| BNC shell grounded | | | | | |
| Range Setting | Signal Frequency | Specification | | Measured Value | |
| | | Lower Limit | Upper Limit | CHAN 1 | CHAN 2 |
| -51 dBV | 1 kHz | -51.25 dBV | -50.75 dBV | | |
| -49 dBV | 1 kHz | -49.25 dBV | -48.75 dBV | | |
| -47 dBV | 1 kHz | -47.25 dBV | -46.75 dBV | | |
| -45 dBV | 1 kHz | -45.25 dBV | -44.75 dBV | | |
| -43 dBV | 1 kHz | -43.25 dBV | -42.75 dBV | | |
| -41 dBV | 1 kHz | -41.25 dBV | -40.75 dBV | | |
| -39 dBV | 1 kHz | -39.25 dBV | -38.75 dBV | | |

| 2-23 Amplitude Accuracy and Flatness Measurement Three | | | | | |
|---|------------------|---------------|-------------|----------------|--------|
| BNC center conductor grounded | | | | | |
| Range Setting | Signal Frequency | Specification | | Measured Value | |
| | | Lower Limit | Upper Limit | CHAN 1 | CHAN 2 |
| 8 dBV | 1 kHz | 7.499 dBV | 8.501 dBV | | |
| 8 dBV | 99 kHz | 7.499 dBV | 8.501 dBV | | |
| -11 dBV | 1 kHz | -11.50 dBV | -10.50 dBV | | |
| -13 dBV | 1 kHz | -13.50 dBV | -12.50 dBV | | |
| -13 dBV | 50 kHz | -13.50 dBV | -12.50 dBV | | |
| -13 dBV | 90 kHz | -13.50 dBV | -12.50 dBV | | |
| -13 dBV | 99 kHz | -13.50 dBV | -12.50 dBV | | |
| -27 dBV | 1 kHz | -27.50 dBV | -26.50 dBV | | |
| -27 dBV | 99 kHz | -27.50 dBV | -26.50 dBV | | |

| 2-24 Amplitude Linearity | | | | | |
|-------------------------------|---------------|-------------------|-------------------------|--------|--|
| Signal Frequency = 10 kHz | | | Range Setting = 10 Vrms | | |
| BNC shell grounded | | | | | |
| Amplitude | Specification | | Measured Value | | |
| | Upper Limit | Lower Limit | CHAN 1 | CHAN 2 | |
| 10.00 Vrms | 10.18 Vrms | 9.827 Vrms | | | |
| 1.000 Vrms | 1.019 Vrms | 981.4 mVrms | | | |
| 100.0 mVrms | 103.2 mVrms | 96.79 mVrms | | | |
| 10.00 mVrms | 11.67 mVrms | 8.329 mVrms | | | |
| 3.1623 mVrms | 4.717 mVrms | 1.608 mVrms | | | |
| 1.000 mVrms | 2.517 mVrms | -517.1 μ Vrms | | | |
| BNC center conductor grounded | | | | | |
| 10.00 Vrms | 10.59 Vrms | 9.439 Vrms | | | |
| 1.000 Vrms | 1.061 Vrms | 942.6 mVrms | | | |
| 100.0 mVrms | 107.4 mVrms | 92.91 mVrms | | | |
| 10.00 mVrms | 12.09 mVrms | 7.941 mVrms | | | |
| 3.1623 mVrms | 4.850 mVrms | 1.485 mVrms | | | |
| 1.000 mVrms | 2.559 mVrms | -555.9 μ Vrms | | | |

| 2-25 Amplitude and Phase Match | | | | | | |
|--------------------------------|------|------|-------------------------|------|------|---------------------|
| BNC shell grounded | | | | | | |
| Range Setting | Part | PASS | Amplitude Specification | Part | PASS | Phase Specification |
| -49 dBV | 1 | | ± 0.1 dB | 4 | | $\pm 0.5^\circ$ |
| 0 dBV | 2 | | ± 0.1 dB | 5 | | $\pm 0.5^\circ$ |
| 10 dBV | 3 | | ± 0.1 dB | 6 | | $\pm 0.5^\circ$ |
| BNC center conductor grounded | | | | | | |
| -13 dBV | 7 | | ± 0.8 dB | 9 | | $\pm 8.5^\circ$ |
| 8 dBV | 8 | | ± 0.8 dB | 10 | | $\pm 8.8^\circ$ |

| 2-26 Anti-Alias Filter Response | | | | |
|---------------------------------|-----------------|-------------|-------------|---------------|
| Signal Frequency | Alias Frequency | PASS CHAN 1 | PASS CHAN 2 | Specification |
| 156 kHz | 100 kHz | | | ≤ -80 dB |
| 184 kHz | 72 kHz | | | ≤ -80 dB |
| 206 kHz | 50 kHz | | | ≤ -80 dB |
| 267 kHz | 11 kHz | | | ≤ -80 dB |

| 2-27 Frequency Accuracy | | | |
|-------------------------|---------------|-------------|----------------|
| Signal Frequency | Specification | | Measured Value |
| | Lower Limit | Upper Limit | |
| 99,000 Hz | 98.996 kHz | 99.004 kHz | |

| 2-28 Input Coupling Insertion Loss | | | |
|------------------------------------|---------------|----------------|---------------|
| Channel 1 | | Channel 2 | |
| Insertion Loss | Specification | Insertion Loss | Specification |
| | <3 dB | | <3 dB |

| 2-29 Single Channel Phase Accuracy | | | | | | |
|------------------------------------|---------|--------|---------------|-------------|----------------|--------|
| BNC shell grounded | | | | | | |
| Signal Frequency | Trigger | | Specification | | Measured Value | |
| | Slope | Type | Lower Limit | Upper Limit | CHAN 1 | CHAN 2 |
| 9 kHz | POS | CHAN 1 | -92.5° | -87.5° | | |
| 9 kHz | POS | CHAN 2 | -92.5° | -87.5° | | |
| 9 kHz | POS | EXT | -92.5° | -87.5° | | |
| 9 kHz | NEG. | EXT | 87.5° | 92.5° | | |
| 99 kHz | POS | CHAN 1 | -102° | -78.0° | | |
| 99 kHz | POS | CHAN 2 | -102° | -78.0° | | |
| 99 kHz | POS | EXT | -102° | -78.0° | | |

| BNC center conductor grounded | | | | | | |
|-------------------------------|---------|--------|---------------|-------------|----------------|--------|
| Signal Frequency | Trigger | | Specification | | Measured Value | |
| | Slope | Type | Lower Limit | Upper Limit | CHAN 1 | CHAN 2 |
| 9 kHz | POS | CHAN 1 | -96.5° | -83.5° | | |
| 9 kHz | POS | CHAN 2 | -96.5° | -83.5° | | |
| 9 kHz | POS | EXT | -96.5° | -83.5° | | |
| 9 kHz | NEG | EXT | 83.5° | 96.5° | | |
| 99 kHz | POS | CHAN 1 | -106° | -74.0° | | |
| 99 kHz | POS | CHAN 2 | -106° | -74.0° | | |
| 99 kHz | POS | EXT | -106° | -74.0° | | |

| 2-30 Input Impedance | | | | |
|---|------------------|-------------------|------------------|--------|
| Resistance Measurement | | | | |
| Range Setting | Specification | | Measured Value | |
| | Lower Limit | Upper Limit | CHAN 1 | CHAN 2 |
| 20 dBV | 950 kΩ | 1050 kΩ | | |
| 0 dBV | 950 kΩ | 1050 kΩ | | |
| -13 dBV | 950 kΩ | 1050 kΩ | | |
| Capacitance Measurement | | | | |
| Channel 1 | | Channel 2 | | |
| V _{in} = | V _{rms} | V _{in} = | V _{rms} | |
| V _c = | V _{rms} | V _c = | V _{rms} | |
| $C = \left[\begin{array}{c c} \frac{V_{in}}{V_c} & -1 \end{array} \right] 15.9 \text{ pF} \text{ } -1.59 \text{ pF}$ | | | | |
| Measured Value | | Specification | | |
| CHAN 1 | CHAN 2 | | | |
| pF | pF | <100 pF | | |

| 2-31 Harmonic Distortion | | | |
|--------------------------|---|---|---------------|
| Measurement One | | | |
| Signal Frequency | Measured Channel 1 Harmonic Frequency Amplitude | Measured Channel 2 Harmonic Frequency Amplitude | Specification |
| 49500 Hz | | | ≤ -80 dB |
| 33000 Hz | | | ≤ -80 dB |
| 245750 Hz | | | ≤ -80 dB |
| 19800 Hz | | | ≤ -80 dB |
| Measurement Two | | | |
| Signal Frequency | Measured Channel 1 Harmonic Frequency Amplitude | Measured Channel 2 Harmonic Frequency Amplitude | Specification |
| 49500 Hz | | | ≤ -80 dB |
| 33000 Hz | | | ≤ -80 dB |
| 24750 Hz | | | ≤ -80 dB |
| 19800 Hz | | | ≤ -80 dB |

| 2-32 Intermodulation Distortion Measurement One | | | | |
|--|-----------|---------------|-----------|---------------|
| BNC shell grounded | Channel 1 | | Channel 2 | |
| Harmonic Frequency | PASS | Specification | PASS | Specification |
| 6 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 14 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 12 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 8 kHz | | ≤ -80 dB | | ≤ -80 dB |
| BNC center conductor grounded | Channel 1 | | Channel 2 | |
| Harmonic Frequency | PASS | Specification | PASS | Specification |
| 6 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 14 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 12 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 8 kHz | | ≤ -80 dB | | ≤ -80 dB |

| 2-32 Intermodulation Distortion Measurement Two | | | | |
|--|-----------|---------------|-----------|---------------|
| BNC shell floating | Channel 1 | | Channel 2 | |
| Harmonic Frequency | PASS | Specification | PASS | Specification |
| 10 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 79 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 20 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 69 kHz | | ≤ -80 dB | | ≤ -80 dB |
| BNC center conductor grounded | Channel 1 | | Channel 2 | |
| Harmonic Frequency | PASS | Specification | PASS | Specification |
| 10 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 79 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 20 kHz | | ≤ -80 dB | | ≤ -80 dB |
| 69 kHz | | ≤ -80 dB | | ≤ -80 dB |

| 2-33 Noise and Spurious Signal Level | | | | |
|--------------------------------------|----------------|-------------|-------------|-------------------------------------|
| Spurious Signals | | | | |
| Start Frequency | Frequency Span | PASS CHAN 1 | PASS CHAN 2 | Specification |
| 20 Hz | 1 kHz | | | ≤ -131 dBV |
| 1 kHz | 10 kHz | | | ≤ -131 dBV |
| 10 kHz | 10 kHz | | | ≤ -131 dBV |
| 20 kHz | 10 kHz | | | ≤ -131 dBV |
| 30 kHz | 10 kHz | | | ≤ -131 dBV |
| 40 kHz | 10 kHz | | | ≤ -131 dBV |
| 50 kHz | 10 kHz | | | ≤ -131 dBV |
| 60 kHz | 10 kHz | | | ≤ -131 dBV |
| 70 kHz | 10 kHz | | | ≤ -131 dBV |
| 80 kHz | 10 kHz | | | ≤ -131 dBV |
| 90 kHz | 10 kHz | | | ≤ -131 dBV |
| Noise Level | | | | |
| Start Frequency | Frequency Span | PASS CHAN 1 | PASS CHAN 2 | Specification |
| 20 Hz | 1 kHz | | | ≤ -134 dBV/ $\sqrt{\text{Hz}}$ |
| 1 kHz | 50 kHz | | | ≤ -144 dBV/ $\sqrt{\text{Hz}}$ |
| 50 kHz | 50 kHz | | | ≤ -144 dBV/ $\sqrt{\text{Hz}}$ |

| 2-34 Cross Talk | | |
|-----------------|----------------|---------------|
| PASS Channel 1 | PASS Channel 2 | Specification |
| | | ≥ 140 dB |

| 2-35 Common Mode Rejection | | | | | | |
|----------------------------|--------------------------|---|---------------------------|---|-----------------------|---------------|
| First Measurement | | – | Second Measurement | = | Relative Value | |
| Signal Frequency | First Measurement CHAN 1 | | Second Measurement CHAN 1 | | Measured Value CHAN 1 | Specification |
| 66 Hz | | | | | | ≥80 dB |
| 500 Hz | | | | | | ≥65 dB |
| Signal Frequency | First Measurement CHAN 2 | | Second Measurement CHAN 2 | | Measured Value CHAN 2 | Specification |
| 66 Hz | | | | | | ≥80 dB |
| 500 Hz | | | | | | ≥65 dB |

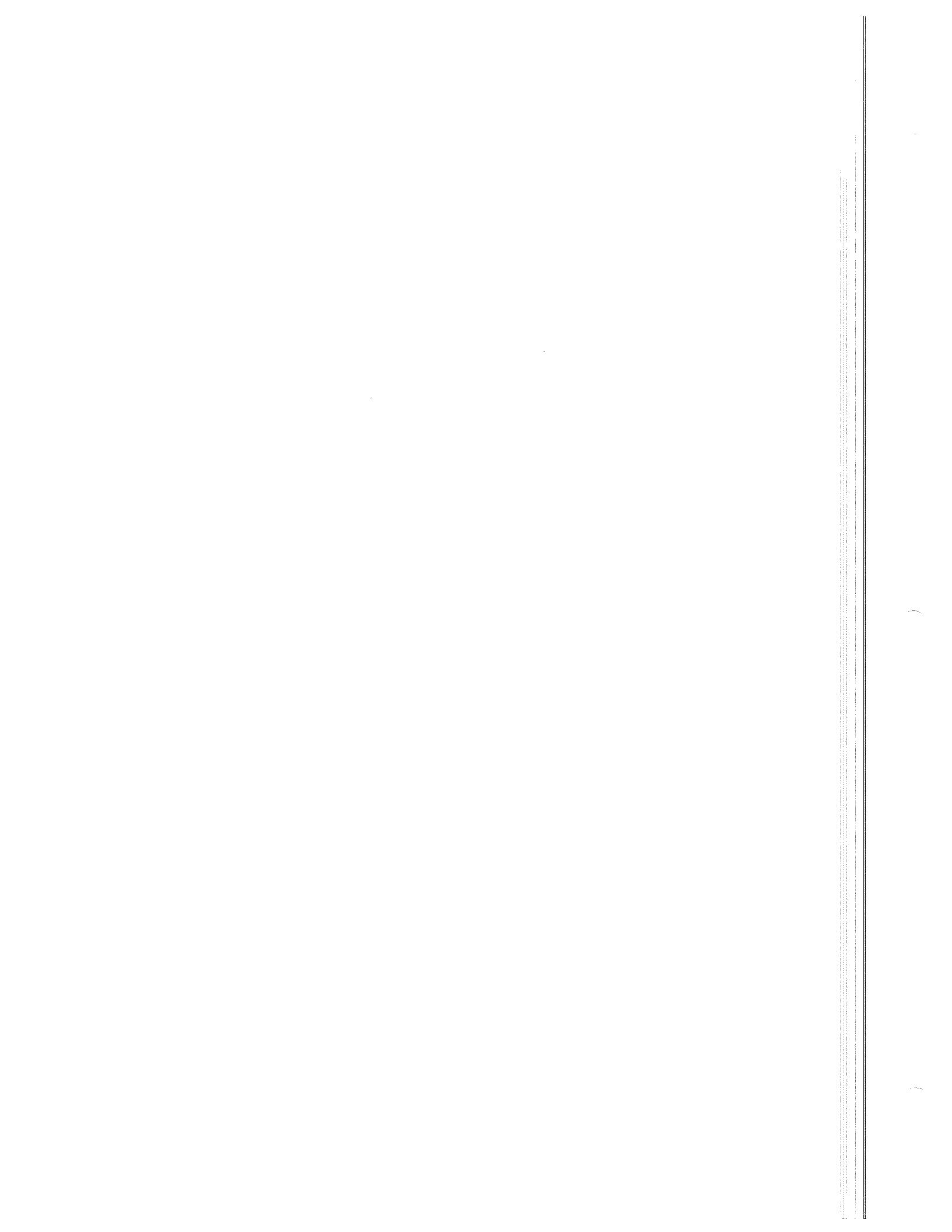
| 2-36 External Reference Test | | |
|------------------------------|----------------|---------------|
| Frequency | Measured Value | Specification |
| 1 MHz | | <999.90 kHz |
| 10 MHz | | >10.001 MHz |

| 2-37 Source Residual Offset | | | |
|-----------------------------|---------------|-------------|----------------|
| Voltage Range Setting | Specification | | Measured Value |
| | Lower Limit | Upper Limit | |
| 1 Vpk | –10 mVpk | 10 mVpk | |
| 5 Vpk | –10 mVpk | 10 mVpk | |

| 2-38 Source Amplitude Accuracy and Flatness | |
|---|------|
| 0 Hz to 65 kHz | PASS |
| 65 kHz to 100 kHz | PASS |

| 2-40 Source Distortion | | | |
|------------------------|------------------|------|---------------|
| Source Amplitude | Source Frequency | PASS | Specification |
| 25 mVpk | 10 kHz | | ≥ 60 dB |
| 5 Vpk | 10 kHz | | ≥ 60 dB |
| 25 mVpk | 99 kHz | | ≥ 40 dB |
| 5 Vpk | 99 kHz | | ≥ 40 dB |

| 2-41 Source Energy Measurement | |
|--|--|
| Random Noise: HP 3562A Reading $(\sqrt{\quad})$ X 100 = $\frac{\quad}{\quad} \geq 70\%$ Voltmeter Average (\quad) % in-band energy | |
| Periodic Chirp: HP 3562A Reading $(\sqrt{\quad})$ X 100 = $\frac{\quad}{\quad} \geq 85\%$ Voltmeter Average (\quad) % in-band energy | |



SECTION III ADJUSTMENTS

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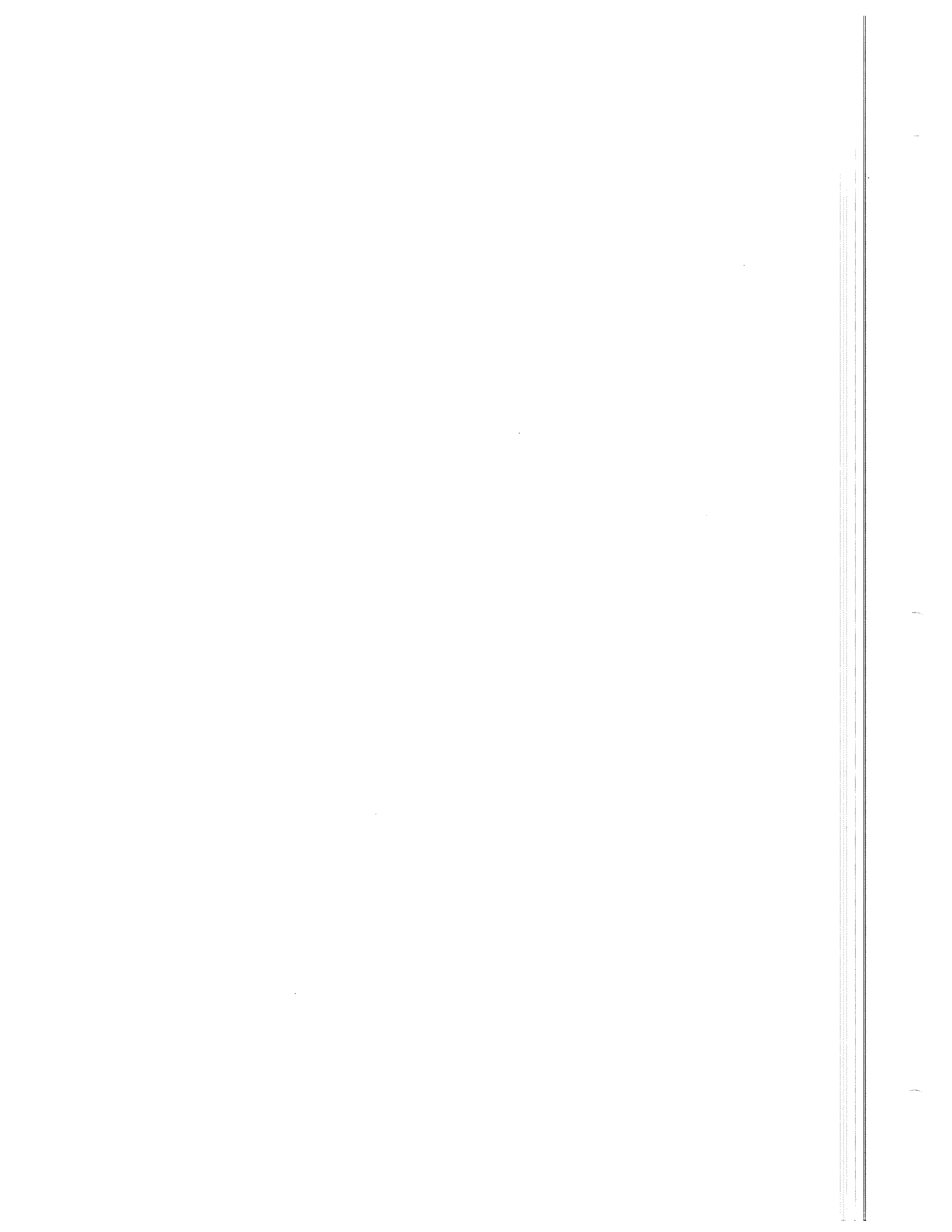
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SECTION III ADJUSTMENTS

3-1 INTRODUCTION

This section describes adjustments and checks required to bring the HP 3562A within the specifications listed in Table 1-1. If adjustments are made to a particular board, all adjustments specified for that board should be made in the order shown in Table 3-1. These procedures should be performed if the specifications of Table 1-1 are not met, if instructed to do so in the troubleshooting section, or after component replacement. These procedures should not be performed as routine maintenance.

NOTE

Allow the HP 3562A to warm up for an hour before performing any adjustments. This is not critical for most of the adjustments due to the automatic calibration feature. It is important when setting the reference and calibrator.

The adjustments described for the ADC and input boards apply to both channel one and channel two of the analyzer front end.

Table 3-1 Adjustment Components

| Adjustment Name | Board | Component |
|------------------------------|------------|-----------|
| Power supply shut-down level | Pwr supply | A18R1 |
| 20.48 MHz reference | Trigger | A31R208 |
| 2nd pass offset | ADC | A32R408 |
| 2nd pass gain | ADC | A32R422 |
| ADC offset | ADC | A32R400 |
| ADC reference | ADC | A32R401 |
| Track-&-hold offset | ADC | A32R408 |
| Input dc offset side A | Input | A33R212 |
| Input dc offset side B | Input | A33R112 |
| Input attenuators: | | |
| side A 40 dB | Input | A33C206 |
| side A 20 dB | Input | A33C202 |
| side B 40 dB | Input | A33C106 |
| side B 20 dB | Input | A33C102 |
| Source dc offset | Source | A30R9 |
| Calibrator gain | Source | A30R10 |

3-2 EQUIPMENT REQUIRED

Table 1-2 lists the equipment required for the adjustment procedures. Any equipment which meets the critical specifications given in the table may be substituted for the recommended model.

3-3 SAFETY CONSIDERATIONS

Although the HP 3562A is designed in accordance with international safety standards, this manual contains information, cautions, and warnings which must be followed to ensure safe operation and to keep the unit in a safe operating condition. Service and adjustments should be performed only by qualified personnel who are aware of the hazards involved.

WARNING

Any interruption of the protective (ground) conductor inside or outside the unit, or disconnection of the protective earth terminal can expose operators to potentially dangerous voltages.

Only fuses of the rated current and specified type should be used for replacement. The use of repaired fuses and short circuiting of fuse holders is not permitted. Whenever fuse protection has been impaired, the HP 3562A must be made inoperative.

Adjustments performed in this section are performed with power applied and the protective covers removed. These adjustments should be performed only by trained service personnel who are aware of the hazards involved (such as fire and electrical shock).

Under no circumstances should an operator remove any covers, screws, shields or in any other way access the interior of the HP 3562A. There are no operator controls inside the instrument.

3-4 POWER SUPPLY ADJUSTMENTS

Description:

The only power supply (A18) adjustment is the line level voltage at which the power supply becomes active. This adjustment should be made only when there has been a failure of the low-line power shut down circuit or the power shut down occurs for line voltages above 81 Vrms when operated on 115 Vac mains power or above 162 Vrms when operated on 230 Vac mains power.

None of the HP 3562A dc power supply voltages are adjustable.

Equipment Required:

- Variable ac power supply
- Oscilloscope HP 1980B
- 10:1 Oscilloscope probe HP 10014A

Procedure:

1. Turn the HP 3562A off, remove the line power cord from the rear panel and place the instrument on its top or side with the bottom panel fully accessible.
2. Remove the HP 3562A bottom cover. None of the internal covers need to be removed.
3. If the mains power voltage selector (on the rear panel) is not in the 115V setting, switch it to 115V.

WARNING

Even with the power switch in the OFF position and the line power cord removed, dangerous voltages may be present on the power supply capacitors.

4. Set the variable ac power supply to output $81 \text{ Vrms} \pm 2 \text{ Vrms}$ and connect the main power cord of the HP 3562A to the variable ac power supply.
5. Configure the scope for dc coupling and connect the scope input to A18**TP12** using a 10:1 probe. See figure 3-1.
6. Turn the HP3562A on.
7. Turn A18**R1** fully CCW and then CW until the signal at TP12 goes low; then turn it CCW until it just goes high. The setting may be tested by lowering the output voltage of the variable ac power supply to 78 Vrms at which point the signal on TP12 should be low.

This completes adjustment of the power supply. If the instrument is normally operated on 230 Vac mains supply, set the rear panel voltage selector to 230V.

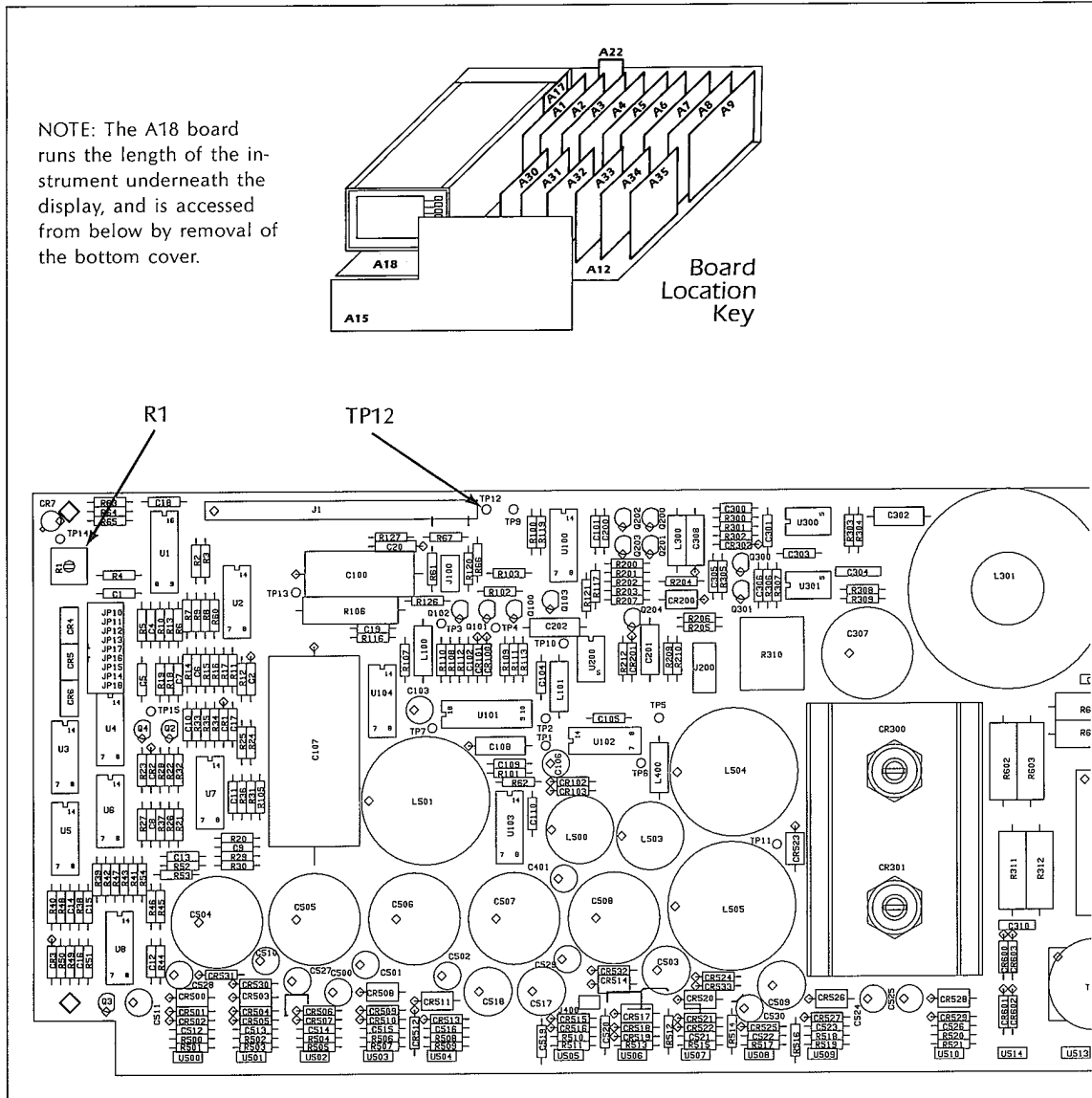


Figure 3-1 Power supply component locator (A18)

3-5 20.48 MHz REFERENCE ADJUSTMENT

Description:

This procedure adjusts the 20.48 MHz frequency reference circuit on the trigger board (A31). This circuit is the source of the timing reference for the ADC boards (A33), the local oscillator (A4) and the main power supply (A18).

Equipment Required:

- Frequency Standard 10 MHz Freq Standard
- Frequency counter HP 5351B
- 1:1 scope probe HP 10083A

CAUTION

Instrument power should always be turned off before any boards are removed or installed. Failing to do so causes circuit failure in most cases.

Procedure

1. Disconnect the line power cord from the rear panel of the HP 3562A.
2. Remove the instrument top cover. This adjustment can be performed without putting the board on an extender board.
3. Move jumper A31**J201** to the test position (connects the lower two pins together).
4. Reconnect the line power cord and turn the power switch ON.

NOTE

Before making this adjustment the HP 3562A must be left on for approximately two hours to allow the reference to come to a stable operating temperature.

5. Connect the frequency standard output to the counter reference input and connect the counter's main counting input to A31**TP10** (VCO output) using the 1:1 probe.
6. Adjust A31**R208** for a counter reading of 20.48 MHz \pm 200 Hz.
7. Remove the power and return A31**J201** to the normal position on the upper two pins.

This completes the adjustment.

3-6 SECOND PASS GAIN ADJUSTMENT

Description:

This procedure adjusts the dc offset of the second pass circuit on the ADC board (A32). This procedure adjusts the dc offsets to prevent nonlinear ADC operation near DAC transition levels. If this adjustment is performed, 3-8 (track and hold offset) must also be done.

Equipment Required:

| | |
|--|----------------|
| Synthesized function generator | HP 3325A |
| Oscilloscope | HP 1980B |
| 1:1 Oscilloscope probe | HP 10083A |
| Extender board (part of kit 03562-84401) | HP 03562-66542 |
| Adapter cable (part of kit 03562-84401) | HP 03585-61616 |
| Capacitive load | (see note) |
| Shorting clip | |

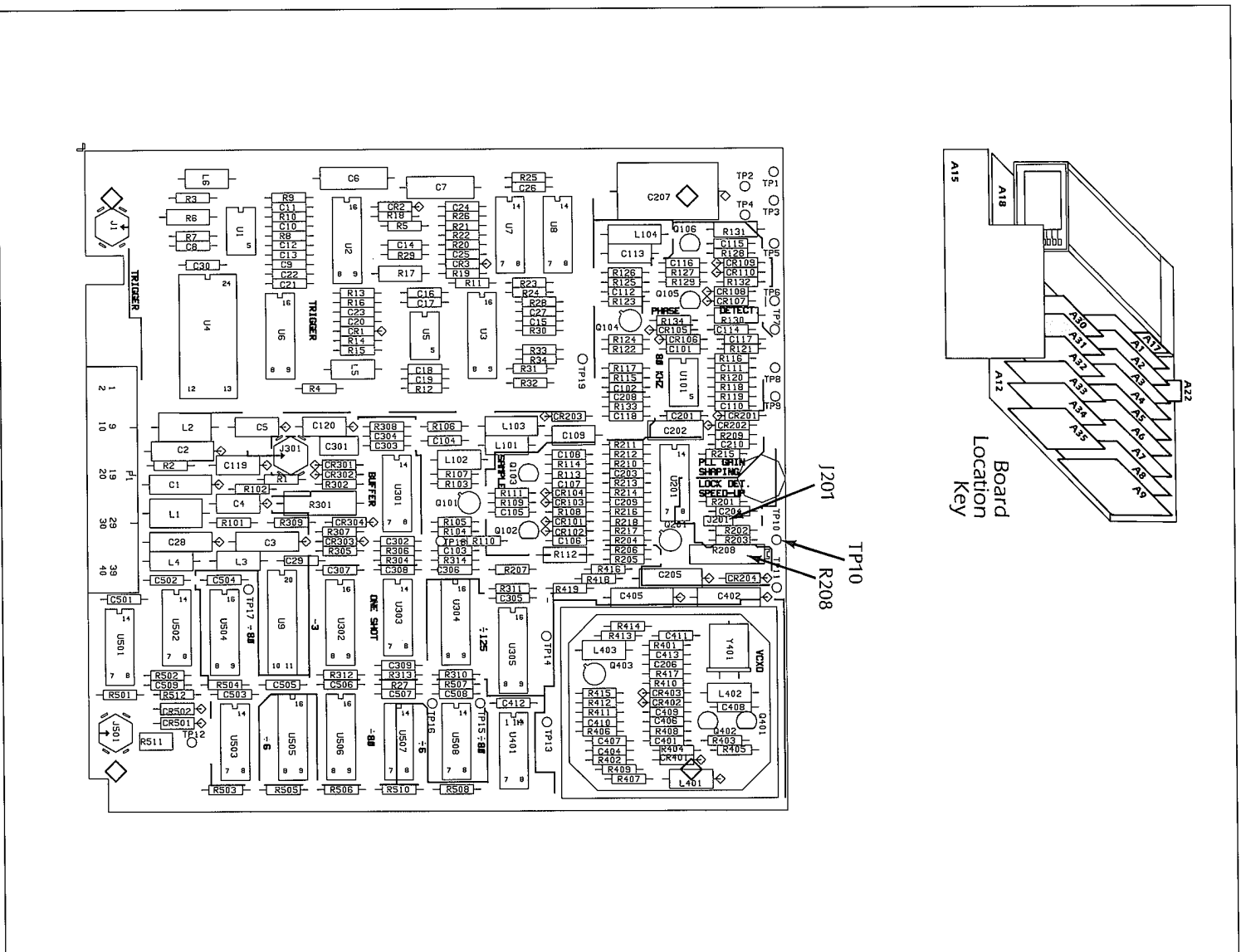


Figure 3-2 Trigger board component locator (A31)

Special note: A capacitive load may be used to reduce noise on the scope display in the following adjustment. This part is not required to perform this adjustment, but it does make it easier to evaluate the results the first few times through the procedure. It consists of a capacitor between the scope input and ground. It is made using a 3300 pf silver mica capacitor and two panel-mount BNC connectors; one female and one male. The HP part numbers for these parts and a drawing showing construction appear in figure 3-3.

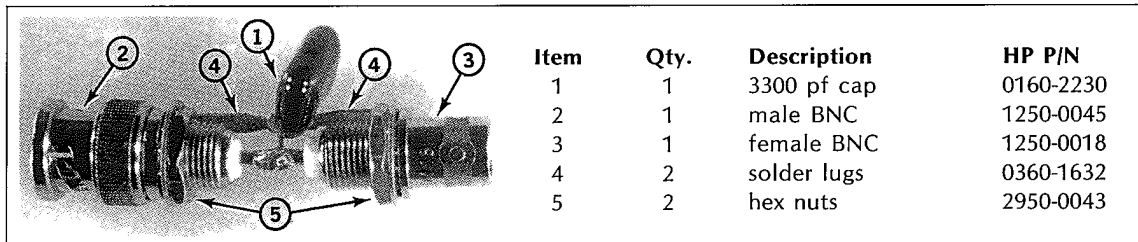


Figure 3-3 Capacitive load

CAUTION

Instrument power should always be turned off before any boards are removed or installed. Failing to do so causes circuit failure in most cases.

Procedure:

1. Disconnect the line power cord from the rear panel of the HP 3562A.
2. Remove the ADC board to be adjusted and place it on the extender board.
3. Reconnect the line power cord and turn the power switch ON.
4. Connect A32**TP400** to a ground test point with a shorting clip. This disables the offset DAC.
5. Remove the coaxial cable connected to A32**J200** and connect the synthesizer output to A32**J200** with the BNC-to-SMB adapter cable. Set the synthesizer for a 30 mVp-p triangle wave at 200 Hz.
6. Connect the scope to A32**TP401** with a 1:1 probe and a capacitive load. Connect the SYNC output of the synthesizer to the MAIN TRIG input of the scope. The scope should be set for 2 mV/div, 2 ms/div, ac coupling, BW limit on, and externally triggered.
7. Press the following keys in the order given:

```

PRESET      .... RESET

RANGE       .... 7 ..... dBVrms

SPCL FCTN   .... BEEPER ON/OFF   .. -66 .. ENTER (Dither off)
               .... BEEPER ON/OFF   .. -69 .. ENTER (2nd pass only)
    
```


NOTE

Pressing the beeper key toggles the beeper between on and off. It does not matter whether the beeper is turned on or off as long as the keys are pressed in the order specified. If beeper commands have been activated, the instrument must be reset before it can make measurements. This is required because the beeper commands configure internal circuits for special tests which do not allow accurate measurements to be made.

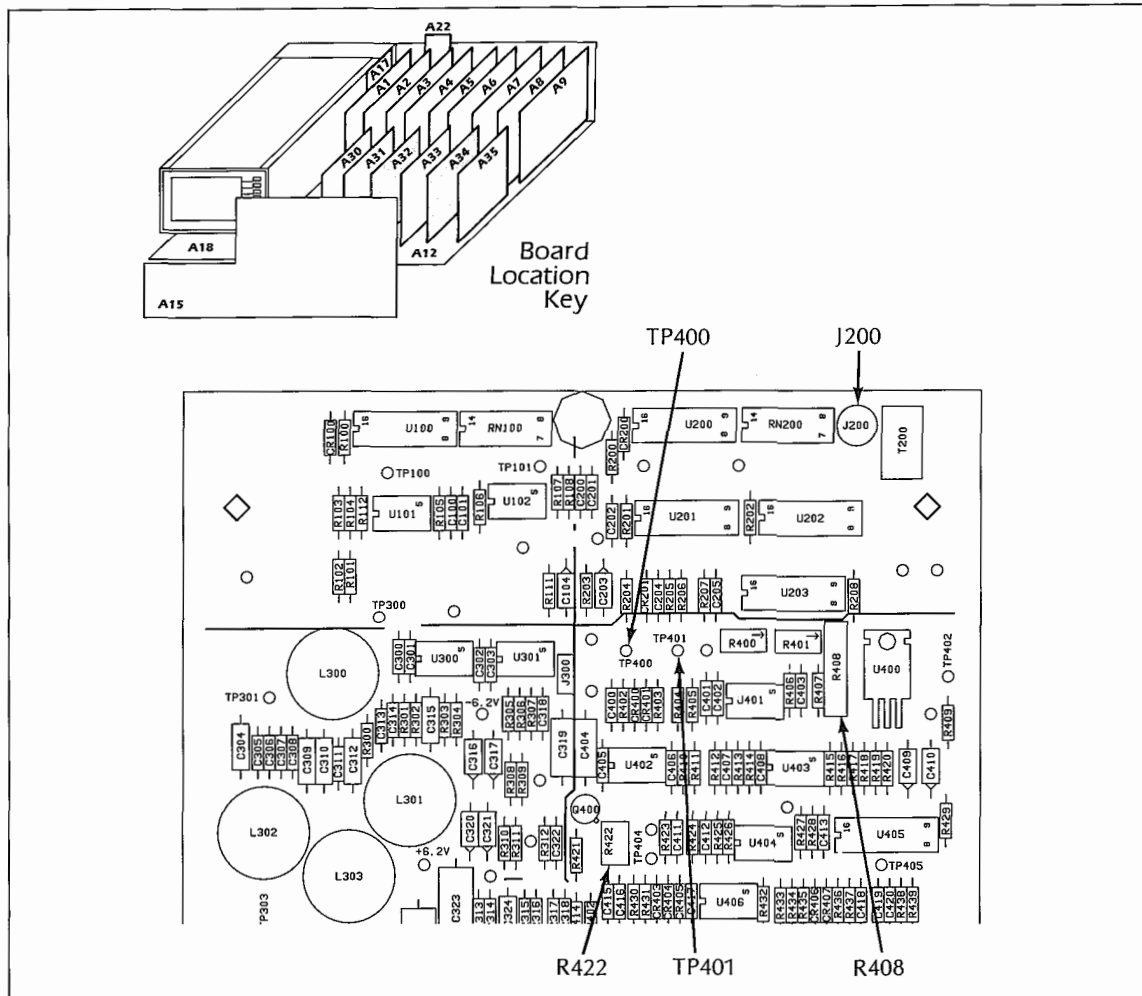


Figure 3-4 ADC board component locator (A32)

If the circuit is badly out of adjustment the signal may appear as a triangle waveform with either the upper or lower corners extending outward as spikes as shown in figure 3-5. The following adjustments should reduce the spikes to form a regular triangle waveshape and then flatten the triangle waveform into a "straight" line as shown in figure 3-8. The noise remaining after adjustment appears in varying amounts on most boards.

8. Adjust A32**R408** to remove sharp spikes in the scope waveform as shown in figure 3-6. These spikes may protrude up or down, depending on which way the adjustment is off.
9. Adjust A32**R422** to flatten the triangle signal at A32**TP401** (shown out of adjustment in figure 3-7).

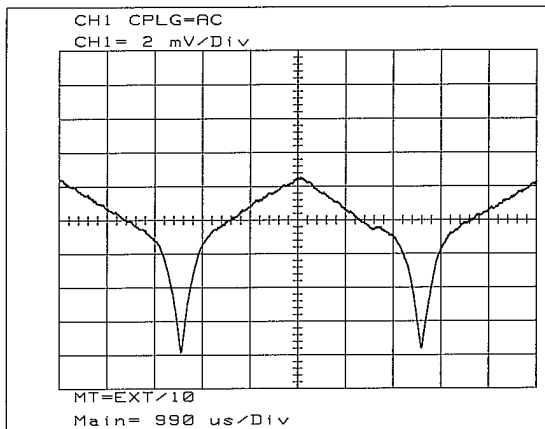


Figure 3-5 Both R408 & R422 out of adjustment

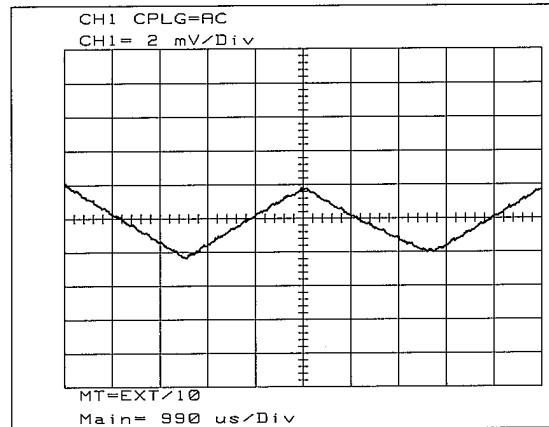


Figure 3-6 R408 needs adjustment

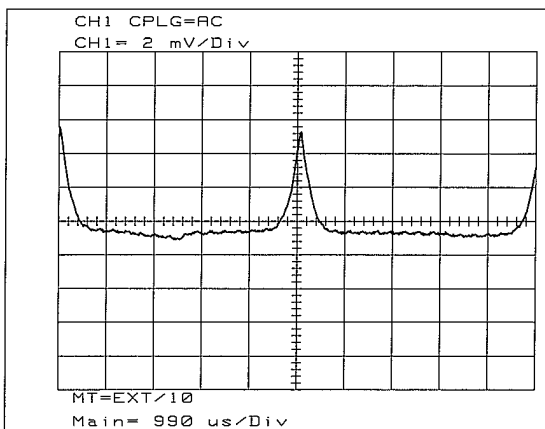


Figure 3-7 R422 needs adjustment (spikes may extend down)

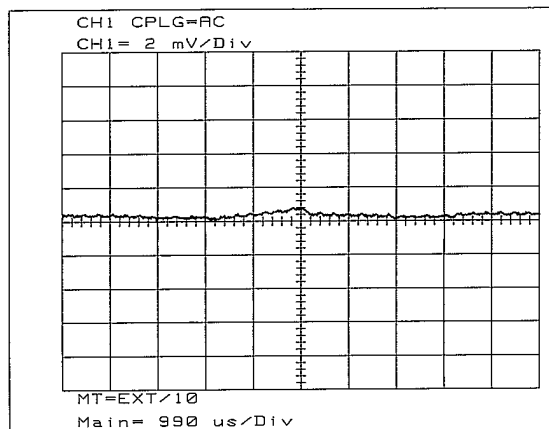


Figure 3-8 Second pass gain adjustments complete

This completes the adjustment. If no more adjustments are to be made to this board, remove the line power cord from the HP 3562A rear panel, remove the extender board and reinstall the ADC board in the card cage.

3-7 ADC OFFSET AND REFERENCE ADJUSTMENT

Description:

This procedure nulls the ADC's dc offset and optimizes its reference voltage.

NOTE

The second pass gain adjustment described in section 3-6 must be completed before making this adjustment.

Equipment Required:

- Frequency Synthesizer HP 3325A
- Oscilloscope HP 1980B
- 10:1 Oscilloscope Probe HP 10014A
- Extender board (part of kit 03562-84401) HP 03562-66542
- Adapter cable (part of kit 03562-84401) HP 03585-61616

CAUTION

Instrument power should always be turned off before any boards are removed or installed. Failing to do so causes circuit failure in most cases.

Procedure:

1. Disconnect the line power cord from the rear panel of the HP 3562A.
2. Remove the ADC board to be adjusted and place it on the extender board.
3. Reconnect the line power cord and turn the power switch ON.
4. Connect A32TP400 to a ground test point.
5. Set the frequency synthesizer for a 800 mVp-p triangle signal at 200 Hz. Connect the frequency synthesizer to A32J200 through the adapter cable.
6. Connect the scope to A32TP405 using the 10:1 probe. **Do not** use the capacitive load. Configure the scope for 15 mV/div, 1.5 ms/div, dc coupling, BW limiting on, and triggering HF rejection.
7. Press the following keys in the order given:

PRESET RESET
RANGE 7 dBVrms
SPCL FCTN BEEPER ON/OFF . . - 66 . . ENTER (Dither off)

(if still in "second pass only" from previous adjustment, beeper - 68 enter will return to normal two pass operation)

NOTE

Pressing the beeper key toggles the beeper between on and off. It does not matter whether the beeper is turned on or off as long as the keys are pressed in the order specified. If beeper commands have been activated, the instrument must be reset before it can make measurements. This is required because the beeper commands configure internal circuits for special tests which do not allow accurate measurements to be made.

8. Three traces should now appear on the scope display as shown in figure 3-10; 1) a straight, horizontal line in the upper half of the display, 2) a clean triangle wave in the lower half of the display, and 3) a "noisy" signal in the lower half of the display that may appear as either a straight or triangular line. The following adjustments flatten this last signal and center it in the clean triangular signal.

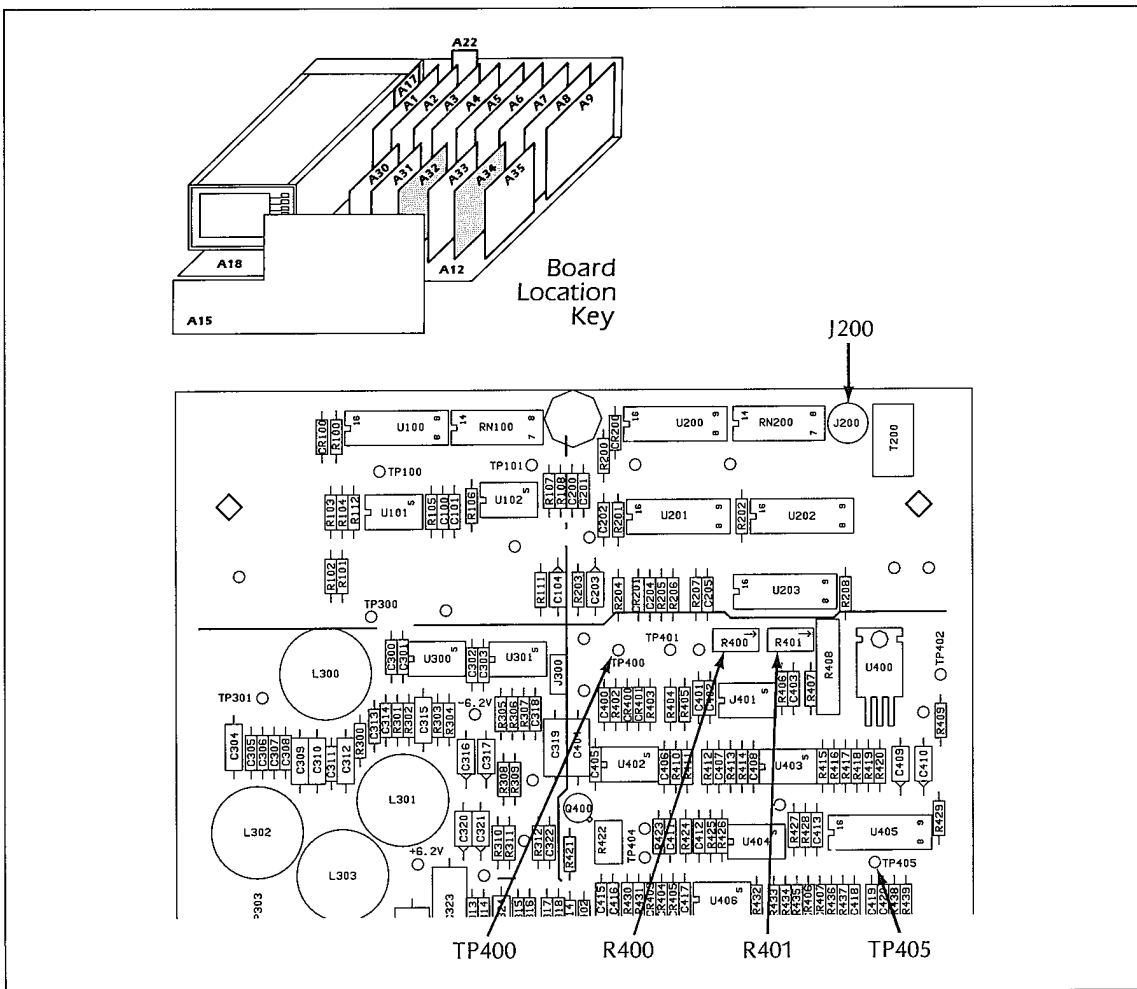


Figure 3-9 ADC board component locator (A32)

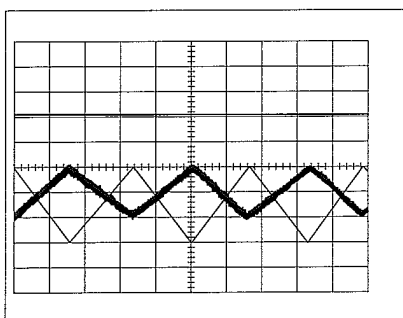


Figure 3-10 Both R401 & R400 out of adjustment

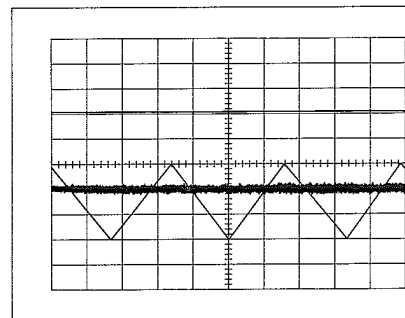


Figure 3-11 R401 adjusted to flatten "noisy" triangle signal

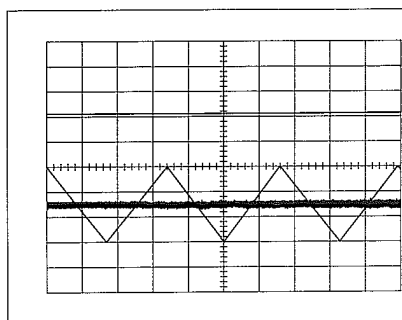


Figure 3-12 R400 adjusted to place "noisy" line in the center of the triangle signal

9. Adjust A32R401 for a flat "noisy" trace as shown in figure 3-11.
10. Adjust A32R400 to center the flat trace in the clean triangle trace as shown in figure 3-12.

This completes the adjustment. If no more adjustments are to be made to this board, remove the line power cord from the HP 3562A rear panel, remove the extender board and reinstall the ADC board in the card cage.

3-8 TRACK AND HOLD OFFSET ADJUSTMENT

Description:

This procedure minimizes the track and hold dc offset. This adjustment is required if the second pass gain adjustment (3-6) is performed, for optimal dc response.

Equipment Required:

Extender board (part of kit 03562-84401) HP 03562-66542

CAUTION

Instrument power should always be turned off before any boards are removed or installed. Failing to do so causes circuit failure in most cases.

Procedure:

1. Disconnect the line power cord from the rear panel of the HP 3562A.
2. Remove the ADC board to be adjusted and place it on the extender board.
3. Reconnect the line power cord and turn the power switch ON.
4. Connect A32TP400 to a test point ground.
5. Move A32J300 to the lower two pins.
6. Press the following keys in the order given:

| | | |
|------------------|--------------------|--------------------------------|
| PRESET | RESET | |
| RANGE | 7 | dBVrms |
| SPCL FCTN | BEEPER ON/OFF | .. -66 .. ENTER (Dither off) |
| | BEEPER ON/OFF | .. -67 .. ENTER (Autozero off) |
| | SERVIC TEST | |
| | LOOP ON | |
| | TEST INPUT | |
| | ADC | |
| | PASS THRU | |

NOTE

Pressing the beeper key toggles the beeper between on and off. It does not matter whether the beeper is turned on or off as long as the keys are pressed in the order specified. If beeper commands have been activated, the instrument must be reset before it can make measurements. This is required because the beeper commands configure internal circuits for special tests which do not allow accurate measurements to be made.

- Numbers appear on the screen under the headings "Channel 1" and Channel 2." Adjust A32R408 until the number corresponding to the channel under test is 0 ± 16 .

This completes the adjustment of the ADC board. Remove the line power cord from the HP 3562A rear panel, return jumper J300 to the upper two pins (normal position), remove the shorting clip between TP400 and ground, remove the extender board and reinstall the ADC board in the card cage.

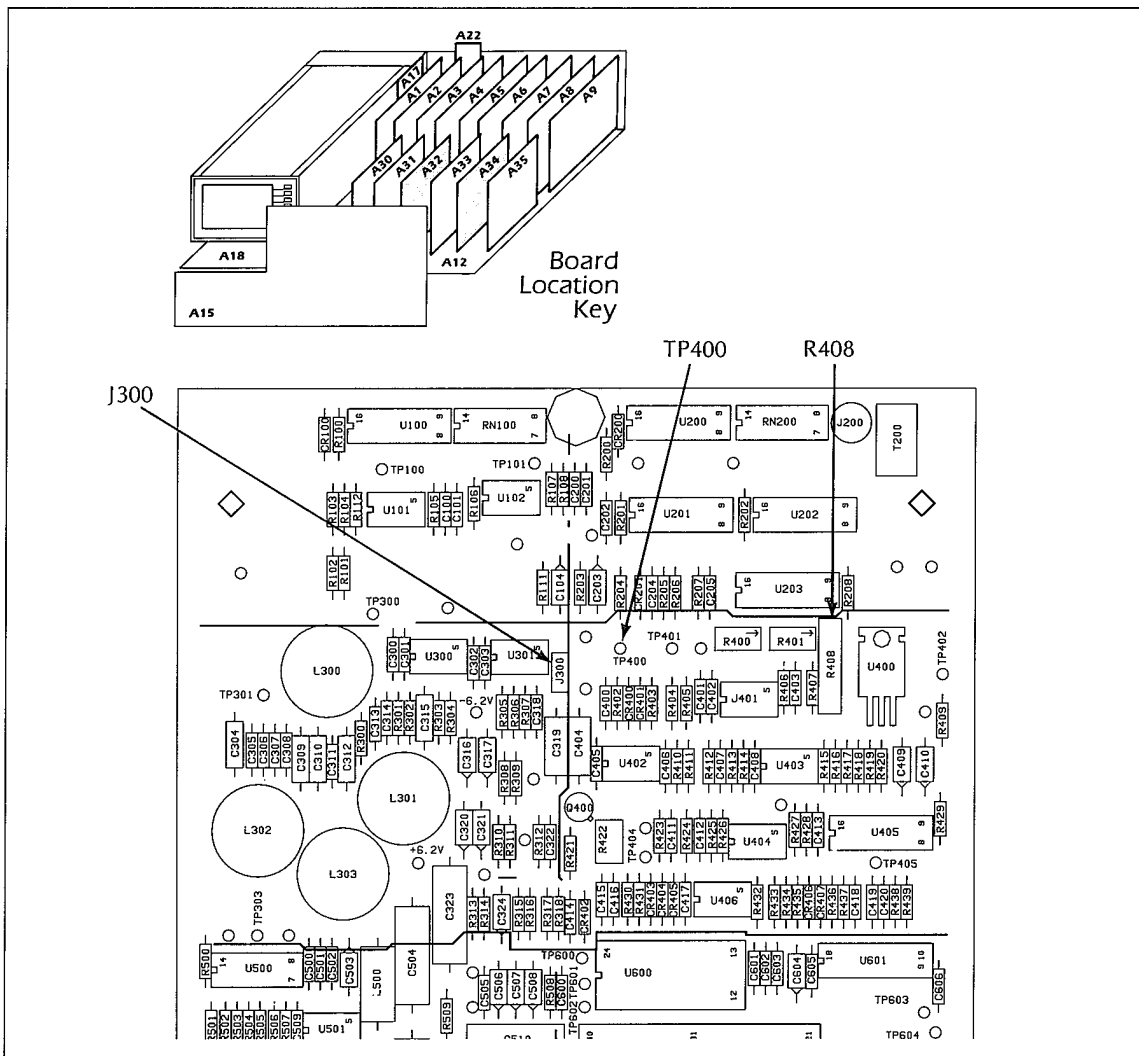


Figure 3-13 ADC board component locator (A32)

3-9 INPUT DC OFFSET ADJUSTMENT

Description:

This procedure centers the offset DAC on the ADC board to allow it maximum correction range in either the positive or negative direction.

Equipment Required:

Extender board (part of kit 03562-84401) HP 03562-66542

CAUTION

Instrument power should always be turned off before any boards are removed or installed. Failing to do so causes circuit failure in most cases.

Procedure:

1. Disconnect the line power cord from the rear panel of the HP 3562A.
2. Remove the Input board (A33) to be adjusted and place it on the extender board. Be sure to reconnect the coax between the input board and its accompanying ADC board.
3. Remove the ADC board of the same channel as the input board under adjustment and ground TP400. Replace the board in the instrument.
4. Short all three pins of the input connector A33**J300** and A33**TP501** together. Since the center pin of the input connector is ground, this grounds the input signals and TP501.
5. Reconnect the line power cord and turn the power switch ON.
6. Press the following keys in the order given:

RANGE **- 51** dBVrms

INPUT
COUPLE Select dc coupling

X (Turn on the X marker at frequency having the largest magnitude; in this case it should be 0 Hz)

To adjust channel two, also press:

MEAS DISP POWER SPEC2

7. Adjust A33**R212** for a marker amplitude reading of less than -85 dB on the HP 3562A display.
8. Remove the ground connection from A33**TP501**.

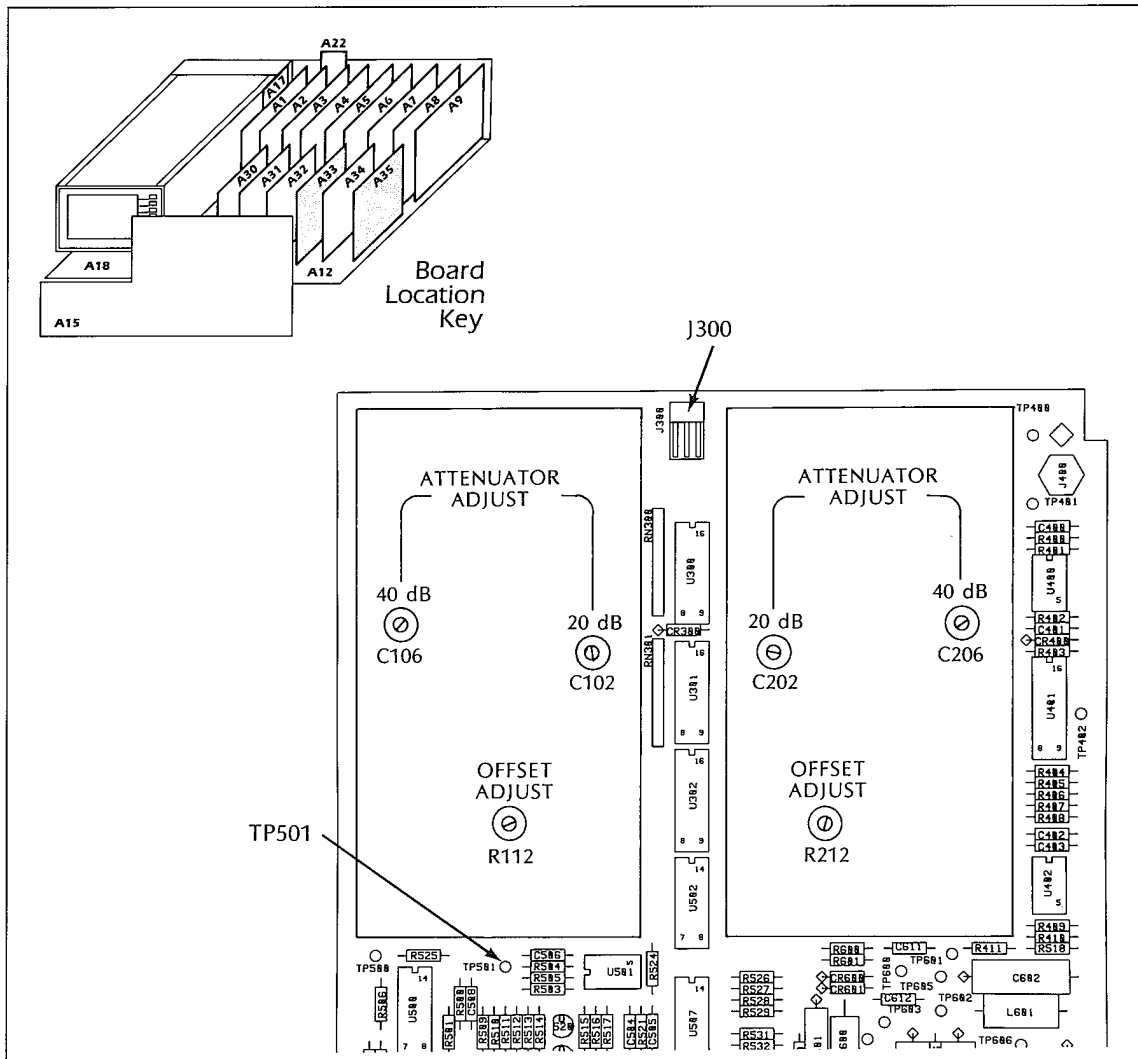


Figure 3-14 Input board component locator (A33)

9. Adjust A33R112 as described in step 7.

This completes the adjustment. If no more adjustments are to be made to this board, remove the line power cord from the HP 3562A rear panel, remove the ground wire from the ADC board, remove the extender board and reinstall the input board in the card cage.

3-10 INPUT ATTENUATORS

Description:

These adjustments set the input attenuation levels on either of the two input boards (A33 or A35). There are two pair of attenuators on each channel. In measurements made with reference to ground, two attenuators (one 20 dB and one 40 dB) are used for range setting on the input boards. When the inputs are floated there are 20 dB and 40 dB attenuators for each side of the input signal for each board (2 ranges on 2 signal lines on 2 boards = 8 total).

NOTE

The input board assemblies for the two channels are identical but it is recommended that they not be interchanged after adjustment.

Equipment Required:

Extender board (part of kit 03562-84401) HP 03562-66542

CAUTION

Instrument power should always be turned off before any boards are removed or installed. Failing to do so causes circuit failure in most cases.

Procedure:

1. Disconnect the line power cord from the rear panel of the HP 3562A.
2. Remove the Input board to be adjusted and place it on the extender board.
3. Reconnect the line power cord and turn the power switch ON.
4. Connect the front two pins of the input connector together. This grounds the low side of the differential input signal.
5. Press the following keys in the order given:

| | |
|-----------------------|--|
| PRESET | RESET |
| RANGE | 1 dBVrms (disables autoranging) |
| PAUSE/CONT | |
| SPCL FCTN | SERVIC TEST |
| | LOOP ON |
| | TEST INPUT |
| | FR END ADJUST |
| | SIDE A 40 dB |

Numbers should appear on the screen under the headings "Channel 1" and "Channel 2".

6. Adjust A33C206 for a zero reading on the HP 3562A display.
7. Press the **SIDE A 20 dB** softkey.
8. Adjust A33C202 for a zero reading on the HP 3562A display.
9. Move the shorting clip on the input connector to the rear two pins, shorting the high side of the differential input signal to ground.

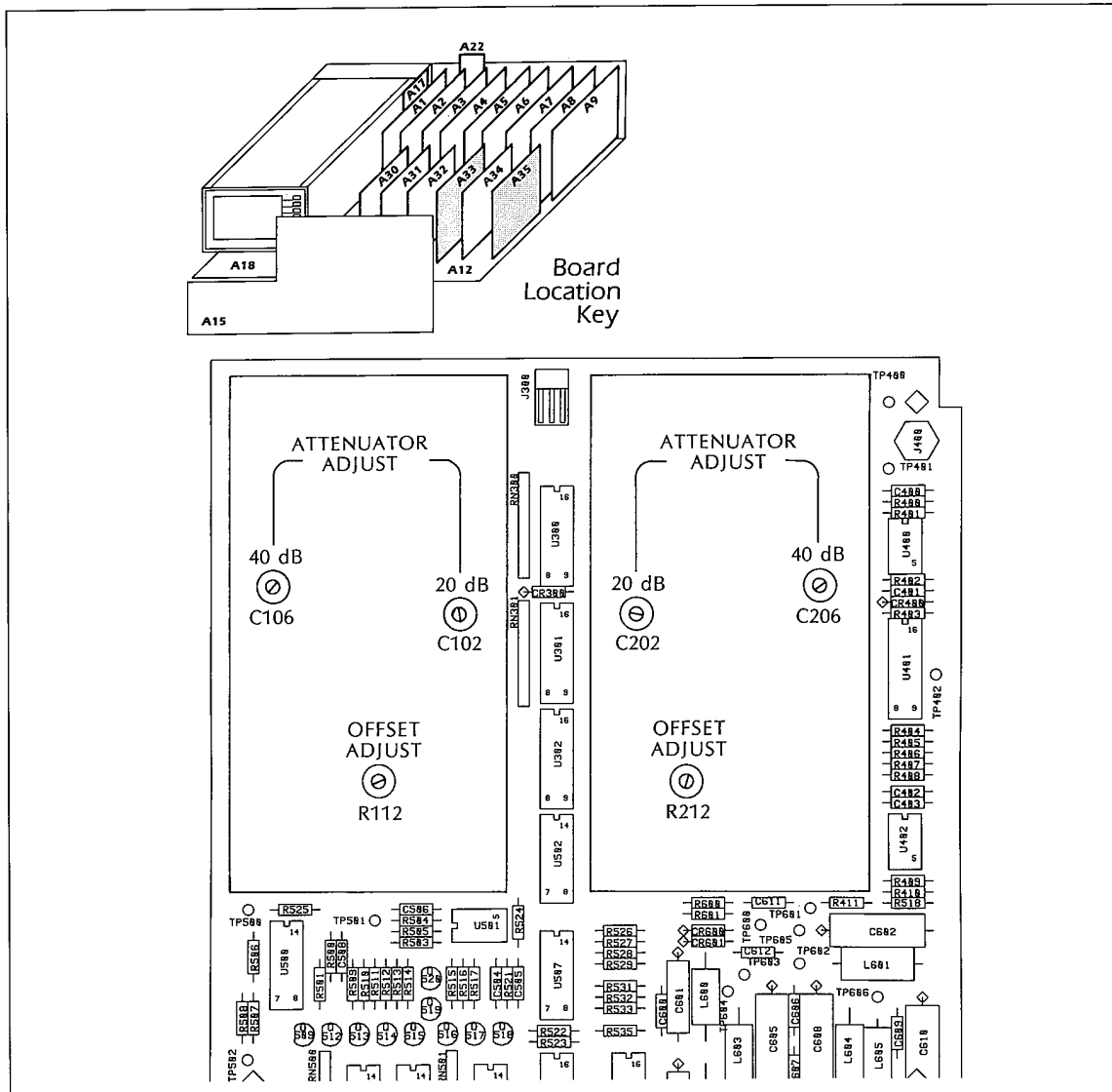


Figure 3-15 Input board component locator (A33)

10. Press the **SIDE B 40 dB** softkey.
11. Adjust A33C106 for a zero reading on the HP 3562A display.
12. Press the **SIDE B 20 dB** softkey.
13. Adjust A33C102 for a zero reading on the HP 3562A display.

This completes the adjustment. Disconnect the line power cord from the HP 3562A rear panel, remove the extender board and reinstall the input board in the card cage.

3-11 SOURCE DC OFFSET ADJUSTMENT

Description:

This procedure adjusts the dc offset control circuitry for proper amplitude. This adjustment sets the gain for the dc offset D/A converter.

Equipment Required:

Digital Voltmeter HP 3455A

Procedure:

1. Preset the HP 3562A by pressing the PRESET hardkey and the RESET softkey.
2. Press the following keys in the order given:

SOURCE SOURCE LEVEL **0** Vpk
 DC OFFSET **10** ... Vpk

3. Connect the digital voltmeter to the HP 3562A source front panel output using a BNC cable and a BNC-to-banana adapter.
4. Adjust A30R9 for a 10 V \pm 75 mV reading on the voltmeter.
5. Press the DC OFFSET softkey and enter a -10 Vpk offset.
6. Check for a -10 V voltmeter reading. Adjust A30R9 so both the the +10 V setting and the -10 V setting are within 75 mV of the programmed value.

This completes the adjustment. Remove the line power cord from the rear panel and disconnect all equipment.

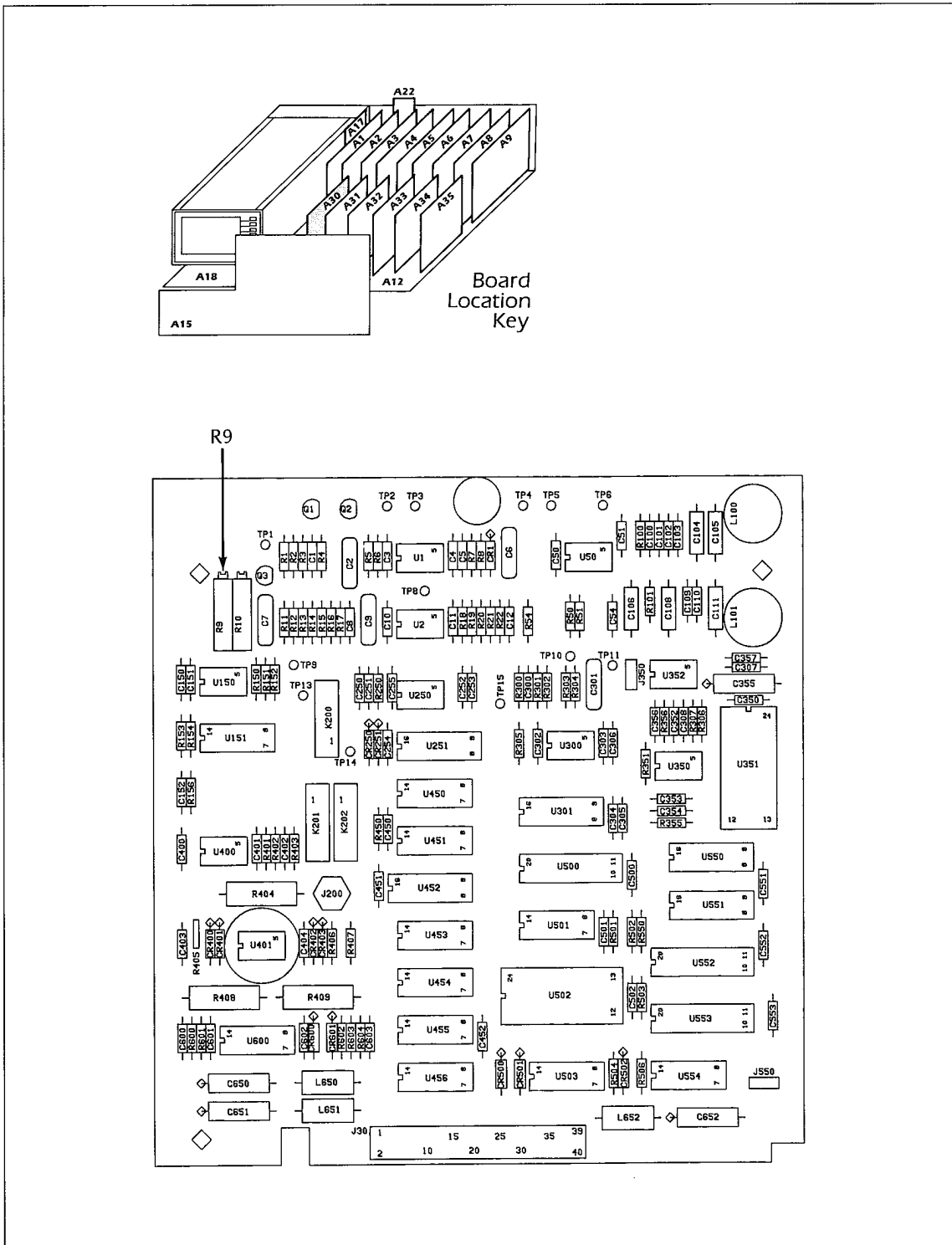


Figure 3-16 Analog source component locator; A30R9

3-12 CALIBRATOR GAIN ADJUSTMENT

Description:

This procedure adjusts the HP 3562A's internal calibrator on the analog source board for the optimum amplitude setting.

Equipment Required:

AC Calibrator Fluke 5200A
 Synthesized function generator HP 3325A

Procedure:

1. Phase lock the calibrator to the function generator and turn calibrator phase lock ON.
2. Preset the HP 3562A by pressing the PRESET hardkey and the RESET softkey.
3. Set the calibrator for 0.2 Vrms and 4 kHz.
4. Connect the calibrator output to the HP 3562A Input 1.
5. Press the following keys in the order given:

PAUSE/CONT

SPCL FCTN SERVIC TEST
 LOOP ON
 TEST INPUT
 FR END ADJUST
 CALIBR ADJUST

6. The HP 3562A display should now show a number that is constantly changing. Adjust **A30R10** until this number is positive as often as it is negative.

This completes the adjustment. Remove the line power cord and reinstall the instrument top cover.

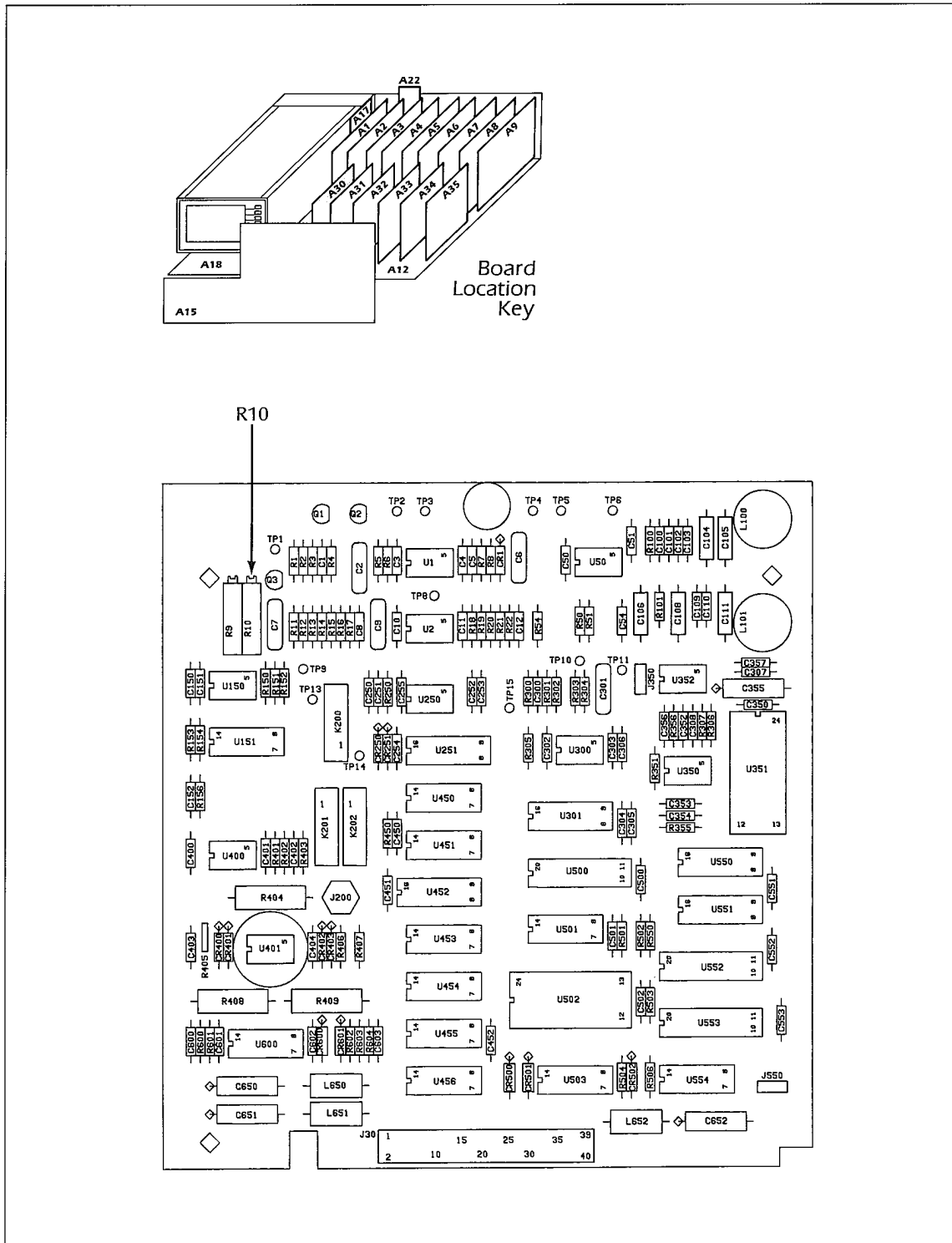
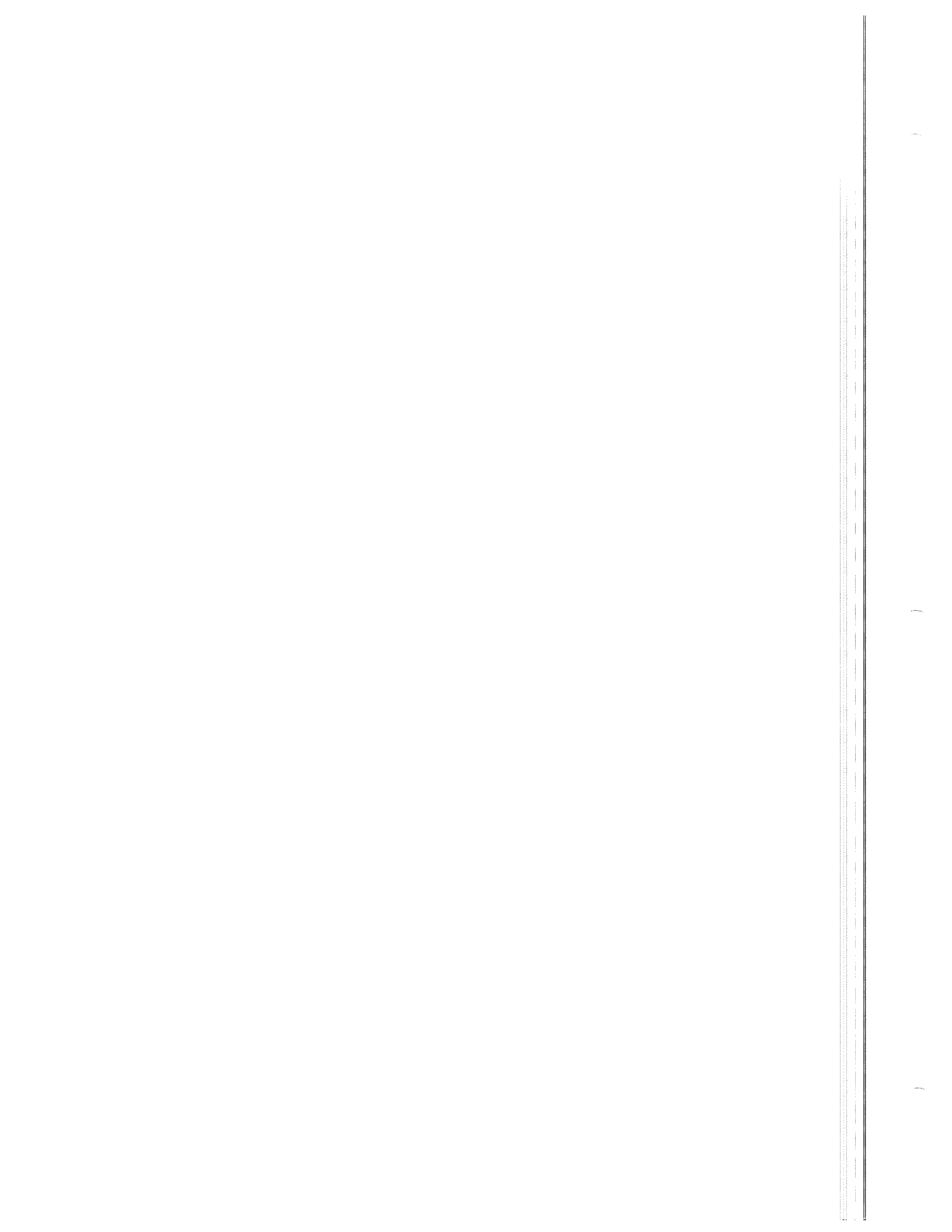


Figure 3-17 Analog source component locator; A30R10



SECTION IV REPLACEABLE PARTS

Contents

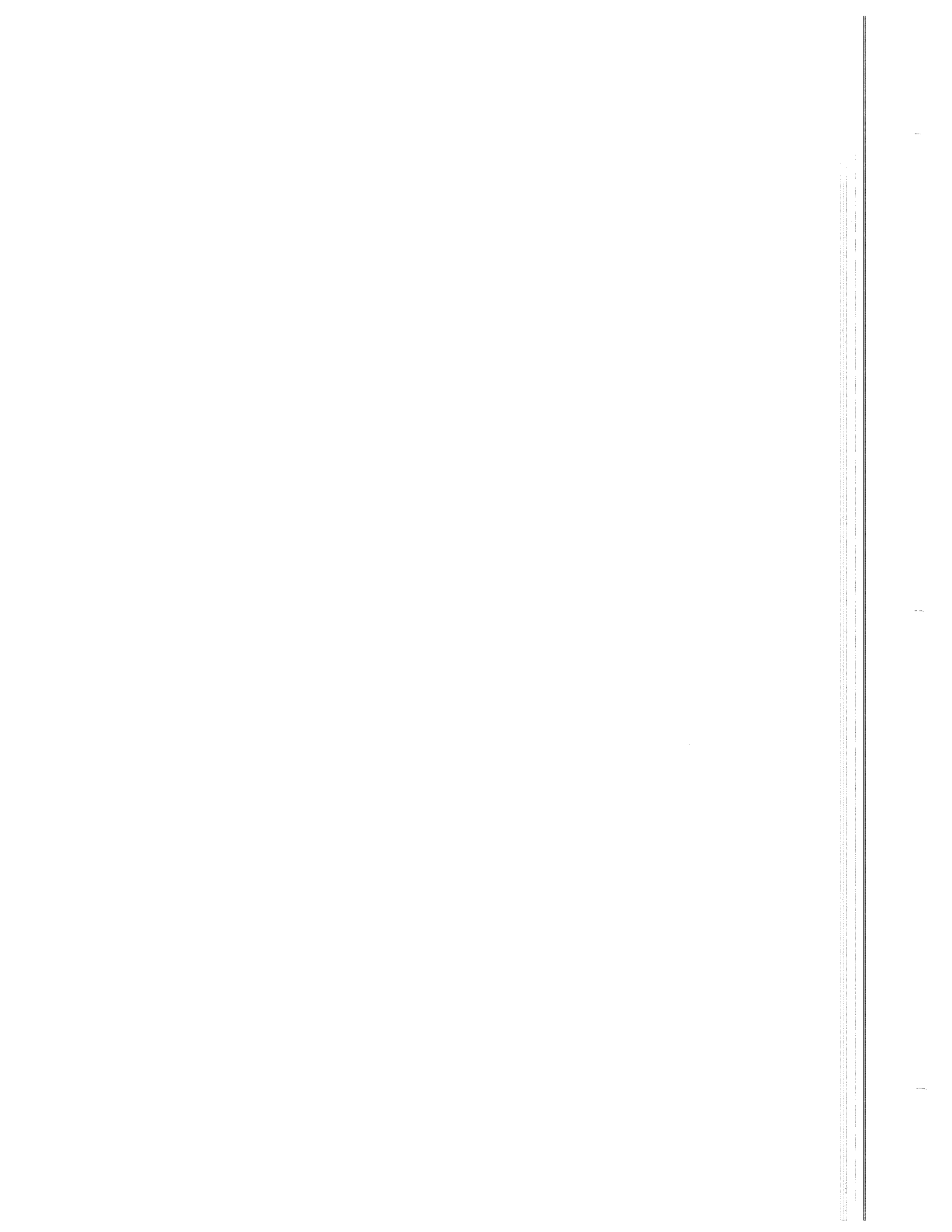
| Paragraph | Title | Page |
|-----------|------------------------------|------|
| 4-1 | Introduction | 4-1 |
| 4-2 | Replaceable Parts List | 4-1 |
| 4-3 | Ordering Information | 4-2 |

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| 4-2 | Manufacturers' Code List | 4-7/4-8 |
| 4-3 | Replaceable Parts | 4-9 |

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| 4-2 | Cabinet Parts, Exploded View | 4-5 |



NOTE

The total quantity of each part is given once for each board — at the first appearance of the part number on the board component listing.

4-3 ORDERING INFORMATION**Ordering Listed Parts**

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check (CD)), indicate the quantity required, and address the order to the nearest Hewlett-Packard office. The check digit will ensure accurate and timely processing of your order.

Ordering Non-listed Parts

To order a part that is NOT listed in the replaceable parts table, include the instrument model number, instrument serial number, description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

Direct Mail Order System

Within the U.S.A., Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

- Direct ordering and shipment from the HP Parts Center in Mountain View, California.
- No maximum or minimum on any mail order. There is a minimum order for parts ordered through a local HP sales and service office when the orders require billing and invoicing.
- Transportation charges are prepaid. A small handling charge is added to each order.
- No invoicing. A check or money order must accompany each order.

Mail order forms and specific ordering information are available through you local Hewlett-Packard sales and service office.

Special Handling

The HP 3562A contains many static sensitive components. Use the appropriate precautions when removing, handling and installing all parts to avoid unnecessary damage.

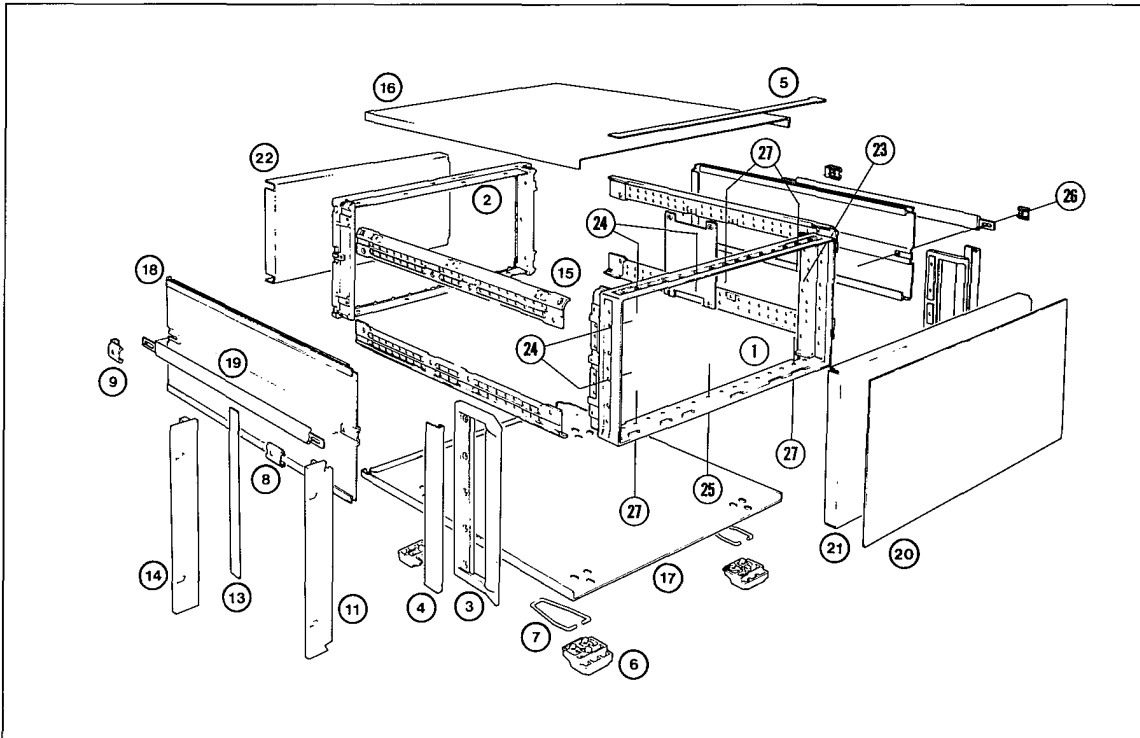


Figure 4-2 Cabinet Parts, Exploded View

| | MP#* | Description | Qty | Current Part Number (Metric)** | Previous Part Number (English)** |
|-----|------|--|-----|--------------------------------|----------------------------------|
| 1. | — | Front frame | 1 | 5021-5807 | 5020-8807 |
| 2. | — | Rear frame | 1 | 5021-5808 | 5020-8808 |
| 3. | — | Front handle kit (optional) | 2 | 5061-9691 | 5061-0091 |
| 4. | — | Trim, front handle | 2 | 5020-8898 | |
| 5. | 507 | Top trim, front frame | 1 | 5040-7202 | |
| 6. | 506 | Foot | 4 | 5040-7201 | |
| 7. | — | Tilt stand | 2 | 1460-1345 | |
| 8. | 508 | Front strap handle cap | 2 | 5041-6819 | 5040-7219 |
| 9. | 509 | Rear strap handle cap | 2 | 5041-6820 | 5040-7220 |
| 11. | — | Rack mount flange kit with front handle (optional) | 2 | 5061-9685 | 5061-0085 |
| 12. | — | Side gusset | 2 | 5001-8234 | |
| 13. | 505 | Side trim, front frame w/o front handle | 2 | 5001-0441 | |
| 14. | — | Rack mount flange kit w/o front handle (optional) | 2 | 5061-9679 | 5061-0079 |
| 15. | — | Corner strut with tapped holes | 4 | 5021-5838 | 5020-8838 |
| 16. | 510 | Top cover | 1 | 5061-9436 | 5060-9836 |
| 17. | 511 | Bottom cover | 1 | 5061-9448 | 5060-9848 |
| 18. | — | Side cover, perforated with handle recess | 2 | 5060-9948 | |
| 19. | 509 | Strap handle | 2 | 5060-9805 | |
| 20. | 100 | Front dress panel | 1 | 03562-00201 | |
| 21. | 101 | Front sub panel | 1 | 03562-00202 | |
| 22. | 200 | Rear panel | 1 | 03562-00203 | |
| 23. | — | Screw | 16 | 0515-1331 | 2510-0192 |
| 24. | — | Screw (attaches to CRT bezel) | 4 | 0515-0889 | 0515-0218 |
| 25. | — | Screw | 1 | 0515-0081 | |
| | — | Lock washer | 1 | 2190-0047 | |
| 26. | — | Screw | 4 | 0515-1132 | 2680-0172 |
| 27. | — | Screw | 5 | 0515-0657 | 0515-0218 |

* From replaceable parts list, table 4-3

** The current part numbers apply to instruments with serial numbers 2502A00566 and greater. The previous part numbers apply to serial numbers 2435A00565 and lower. If there is no previous part number listed, all serial numbers use the current part number.

Table 4-1 Reference Designations and Abbreviations

| Abbreviations | |
|------------------------|--|
| Ag | silver |
| Al | aluminum |
| A | ampere(s) |
| Au | gold |
| C | capacitor |
| cer | ceramic |
| coef | coefficient |
| com | common |
| comp | composition |
| conn | connection |
| dep | deposited |
| DPDT | double-pole double-throw |
| DPST | double-pole single-throw |
| elect | electrolytic |
| encap | encapsulated |
| F | farad(s) |
| FET | field effect transistor |
| fxd | fixed |
| GaAs | gallium arsenide |
| GHz | gigahertz = 10^{+9} hertz |
| gd | guard(ed) |
| Ge | germanium |
| gnd | ground(ed) |
| H | henry(ies) |
| Hg | mercury |
| Hz | hertz (cycle(s) per second) |
| ID | inside diameter |
| impg | impregnated |
| incd | incandescent |
| ins | insulation(ed) |
| k Ω | kilohm(s) = 10^{+3} ohms |
| kHz | kilohertz = 10^{+3} hertz |
| L | inductor |
| lin | linear taper |
| log | logarithmic taper |
| mA | milliamper(e)s = 10^{-3} amperes |
| MHz | megahertz = 10^{+6} hertz |
| M Ω | megohm(s) = 10^{+6} ohms |
| met flm | metal film |
| mfr | manufacturer |
| ms | millisecond |
| mtg | mounting |
| mV | millivolt(s) = 10^{-3} volts |
| μ F | microfarad(s) |
| μ s | microsecond(s) |
| μ V | microvolt(s) = 10^{-6} volts |
| my | Mylar [®] |
| nA | nanoampere(s) = 10^{-9} amperes |
| NC | normally closed |
| Ne | neon |
| NO | normally open |
| NPO | negative positive zero (zero temperature coefficient) |
| ns | nanosecond(s) = 10^{-9} seconds |
| nsr | not separately replaceable |
| Ω | ohm(s) |
| obd | order by description |
| OD | outside diameter |
| p | peak |
| pA | picoampere(s) |
| pc | printed circuit |
| pF | picofarad(s) 10^{-12} farads |
| piv | peak inverse voltage |
| p/o | part of |
| pos | position(s) |
| poly | polystyrene |
| pot | potentiometer |
| p-p | peak-to-peak |
| ppm | parts per million |
| prec | precision (temperature coefficient, long term stability and/or tolerance) |
| R | resistor |
| Rh | rhodium |
| rms | root-mean-square |
| rot | rotary |
| Se | selenium |
| sect | section(s) |
| Si | silicon |
| sl | slide |
| SPDT | single-pole double-throw |
| SPST | single-pole single-throw |
| Ta | tantalum |
| TC | temperature coefficient |
| TiO ₂ | titanium dioxide |
| tog | toggle |
| tol | tolerance |
| trim | trimmer |
| TSTR | transistor |
| V | volt(s) |
| vacw | alternating current working voltage |
| var | variable |
| vdcw | direct current working voltage |
| W | watt(s) |
| w/ | with |
| wiv | working inverse voltage |
| w/o | without |
| ww | wirewound |
| * | optimum value selected at factory average value shown (part may be omitted) |
| ** | no standard type number assigned selected or special type |
| | [®] Dupont de Nemours |
| Designators | |
| A | assembly |
| B | motor |
| BT | battery |
| C | capacitor |
| CR | diode or thyristor |
| DL | delay line |
| DS | lamp |
| E | misc electronic part |
| F | fuse |
| FL | filter |
| HR | heater |
| IC | integrated circuit |
| J | jack |
| K | relay |
| L | inductor |
| M | meter |
| MP | mechanical part |
| P | plug |
| Q | transistor |
| QCR | transistor-diode |
| R(p) | resistor(pack) |
| RT | thermistor |
| S | switch |
| T | transformer |
| TB | terminal board |
| TC | thermocouple |
| TP | test point |
| TS | terminal strip |
| U | microcircuit |
| V | vacuum tube, neon bulb, photocell, etc. |
| W | cable, jumper |
| X | socket |
| XDS | lampholder |
| XF | fuseholder |
| Y | crystal |
| Z | network |

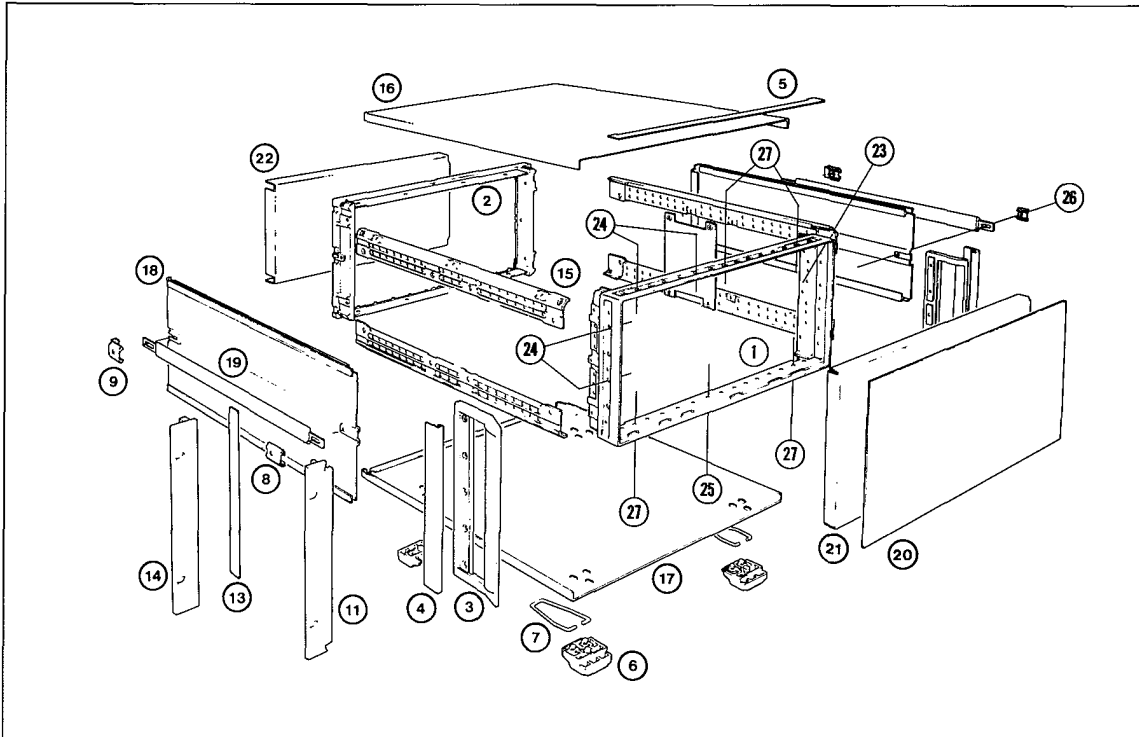


Figure 4-2 Cabinet Parts, Exploded View

| | MP#* | Description | Qty | Current Part Number (Metric)** | Previous Part Number (English)** |
|-----|------|--|-----|--------------------------------|----------------------------------|
| 1. | — | Front frame | 1 | 5021-5807 | 5020-8807 |
| 2. | — | Rear frame | 1 | 5021-5808 | 5020-8808 |
| 3. | — | Front handle kit (optional) | 2 | 5061-9691 | 5061-0091 |
| 4. | — | Trim, front handle | 2 | 5020-8898 | |
| 5. | 507 | Top trim, front frame | 1 | 5040-7202 | |
| 6. | 506 | Foot | 4 | 5040-7201 | |
| 7. | — | Tilt stand | 2 | 1460-1345 | |
| 8. | 508 | Front strap handle cap | 2 | 5041-6819 | 5040-7219 |
| 9. | 509 | Rear strap handle cap | 2 | 5041-6820 | 5040-7220 |
| 11. | — | Rack mount flange kit with front handle (optional) | 2 | 5061-9685 | 5061-0085 |
| 12. | — | Side gusset | 2 | 5001-8234 | |
| 13. | 505 | Side trim, front frame w/o front handle | 2 | 5001-0441 | |
| 14. | — | Rack mount flange kit w/o front handle (optional) | 2 | 5061-9679 | 5061-0079 |
| 15. | — | Corner strut with tapped holes | 4 | 5021-5838 | 5020-8838 |
| 16. | 510 | Top cover | 1 | 5061-9436 | 5060-9836 |
| 17. | 511 | Bottom cover | 1 | 5061-9448 | 5060-9848 |
| 18. | — | Side cover, perforated with handle recess | 2 | 5060-9948 | |
| 19. | 509 | Strap handle | 2 | 5060-9805 | |
| 20. | 100 | Front dress panel | 1 | 03562-00201 | |
| 21. | 101 | Front sub panel | 1 | 03562-00202 | |
| 22. | 200 | Rear panel | 1 | 03562-00203 | |
| 23. | — | Screw | 16 | 0515-1331 | 2510-0192 |
| 24. | — | Screw (attaches to CRT bezel) | 4 | 0515-0889 | 0515-0218 |
| 25. | — | Screw | 1 | 0515-0081 | |
| | | Lock washer | 1 | 2190-0047 | |
| 26. | — | Screw | 4 | 0515-1132 | 2680-0172 |
| 27. | — | Screw | 5 | 0515-0657 | 0515-0218 |

* From replaceable parts list, table 4-3

** The current part numbers apply to instruments with serial numbers 2502A00566 and greater. The previous part numbers apply to serial numbers 2435A00565 and lower. If there is no previous part number listed, all serial numbers use the current part number.

Table 4-1 Reference Designations and Abbreviations

| Abbreviations | |
|--|---|
| Ag silver | NPO negative positive zero (zero temperature coefficient) |
| Al aluminum | ns nanosecond(s) = 10 ⁻⁹ seconds |
| A ampere(s) | nsr not separately replaceable |
| Au gold | Ω ohm(s) |
| C capacitor | obd order by description |
| cer ceramic | OD outside diameter |
| coef coefficient | p peak |
| com common | pA picoampere(s) |
| comp composition | pc printed circuit |
| conn connection | pF picofarad(s) 10 ⁻¹² farads |
| dep deposited | piv peak inverse voltage |
| DPDT double-pole double-throw | p/o part of |
| DPST double-pole single-throw | pos position(s) |
| elect electrolytic | poly polystyrene |
| encap encapsulated | pot potentiometer |
| F farad(s) | p-p peak-to-peak |
| FET field effect transistor | ppm parts per million |
| fxd fixed | prec precision (temperature coefficient, long term stability and/or tolerance) |
| GaAs gallium arsenide | R resistor |
| GHz gigahertz = 10 ⁹ hertz | Rh rhodium |
| gd guard(ed) | rms root-mean-square |
| Ge germanium | rot rotary |
| gnd ground(ed) | Se selenium |
| H henry(ies) | sect section(s) |
| Hg mercury | Si silicon |
| Hz hertz (cycle(s) per second) | sl slide |
| ID inside diameter | SPDT single-pole double-throw |
| imp impregnated | SPST single-pole single-throw |
| incd incandescent | Ta tantalum |
| ins insulation(ed) | TC temperature coefficient |
| kΩ kilohm(s) = 10 ⁺³ ohms | TiO ₂ titanium dioxide |
| kHz kilohertz = 10 ⁺³ hertz | tog toggle |
| L inductor | tol tolerance |
| lin linear taper | trim trimmer |
| log logarithmic taper | TSTR transistor |
| mA milliampere(s) = 10 ⁻³ amperes | V volt(s) |
| MHz megahertz = 10 ⁺⁶ hertz | vacw alternating current working voltage |
| MΩ megohm(s) = 10 ⁺⁶ ohms | var variable |
| met flm metal film | vcw direct current working voltage |
| mfr manufacturer | W watt(s) |
| ms millisecond | w/ with |
| mtg mounting | wiv working inverse voltage |
| mV millivolt(s) = 10 ⁻³ volts | w/o without |
| μF microfarad(s) | ww wirewound |
| μs microsecond(s) | |
| μV microvolt(s) = 10 ⁻⁶ volts | |
| my Mylar® | * optimum value selected at factory average value shown (part may be omitted) |
| nA nanoampere(s) = 10 ⁻⁹ amperes | ** no standard type number assigned selected or special type |
| NC normally closed | ® Dupont de Nemours |
| Ne neon | |
| NO normally open | |

| Designators | |
|------------------------------|---|
| A assembly | Q transistor |
| B motor | QCR transistor-diode |
| BT battery | R(p) resistor(pack) |
| C capacitor | RT thermistor |
| CR diode or thyristor | S switch |
| DL delay line | T transformer |
| DS lamp | TB terminal board |
| E misc electronic part | TC thermocouple |
| F fuse | TP test point |
| FL filter | TS terminal strip |
| HR heater | U microcircuit |
| IC integrated circuit | V vacuum tube, neon bulb, photocell, etc. |
| J jack | W cable, jumper |
| K relay | X socket |
| L inductor | XDS lampholder |
| M meter | XF fuseholder |
| MP mechanical part | Y crystal |
| P plug | Z network |

Table 4-2 Manufacturers Code List

| MFR NO. | MANUFACTURER NAME | ADDRESS | ZIP CODE |
|---------|-------------------------------------|--------------------|----------|
| H9027 | Schurter A G H | Luzern SW | |
| 00779 | Amp Inc | Harrisburg PA | 17105 |
| 00853 | Sangamo Weston Inc | Pickens SC | 29671 |
| 01121 | Allen-Bradley Co | Milwaukee WI | 53204 |
| 01295 | Texas Instr Inc Semicon Cmpnt Div | Dallas TX | 75222 |
| 01536 | Textron Inc, Camcar Div | Rockford IL | 61108 |
| 02114 | Emperex Electronic Corp | Saugerties NY | 12477 |
| 03580 | French Creek Granite Co Inc | St Peters PA | |
| 04213 | Caddell-Burns Mfg Co Inc | Mimeola NY | 11501 |
| 04222 | AVX Ceramics Div | Myrtle Beach SC | 29577 |
| 04713 | Motorola Semiconductor Products | Phoenix AZ | 85008 |
| 05245 | Corcom Inc | Libertyville IL | 60048 |
| 06090 | Raychem Corp | Menlo Park CA | 94025 |
| 06560 | Airco Electronics Inc | Mogales AZ | |
| 06665 | Precision Monolithics Inc | Santa Clara CA | 95050 |
| 07263 | Fairchild Semiconductor Div | Mountain View CA | 94042 |
| 09023 | Cornell-Dubilier Electronics | Fuquay-Varina NC | 27526 |
| 09161 | The Brucon Co | San Francisco CA | |
| 09353 | C & K Components Inc | Newton MA | 02158 |
| 09922 | Burndy Corp | Norwalk CT | 06856 |
| 11236 | CTS of Berne Inc | Berne IN | 46711 |
| 11502 | TRW Resistive Products Div | Boone NC | 28607 |
| 13103 | Thermalloy Co | Dallas TX | 75234 |
| 13606 | Sprague Elect Co Semiconductor Div | Concord NH | 03301 |
| 15454 | Ametek/Rodan Div | Anaheim CA | 92806 |
| 16941 | Long-Loc Fasteners Corp | Cincinnati OH | 45215 |
| 17856 | Siliconix Inc | Santa Clara CA | 95054 |
| 18324 | Signetics Corp | Sunnyvale CA | 94086 |
| 18546 | Bean Rubber Mfg Co | San Jose CA | 95112 |
| 19378 | Diganostic/Retrieval Systems Inc | Oakland NJ | 07436 |
| 19701 | Mepco/Electra Corp | Mineral Wells TX | 76067 |
| 22526 | Du Pont E I de Remours & Co | New Cumberland PA | 17070 |
| 22670 | G M Nameplate Inc | Seattle WA | 98119 |
| 24226 | Gowanda Electronics Corp | Gowanda NY | 14070 |
| 24355 | Analog Devices Inc | Norwood MA | 02062 |
| 24444 | General Semiconductor Industries | Tempe AZ | 85281 |
| 24931 | Specialty Connector Co | Greenwood IN | 46142 |
| 25088 | Siemens Corp | Iselin NJ | 08830 |
| 25403 | N.V. Philips-Elcoma Department | Eindhoven HL | 02867 |
| 27014 | National Semiconductor Corp | Santa Clara CA | 95051 |
| 27167 | Corning Glass Works (Wilmington) | Wilmington NC | 28401 |
| 27264 | Molex Inc | Lisle IL | 60532 |
| 27463 | Tharco Precision Inc | San Lorenzo CA | 94580 |
| 28480 | Hewlett-Packard Co Corporate HQ | Palo Alto CA | 94304 |
| 31785 | Isotemp Research Inc | Charlottesville VA | 22901 |
| 32997 | Bourns Inc Trimpot Prod Div | Riverside CA | 92507 |
| 33096 | Colorado Crystal Corp | Loveland CO | 80537 |
| 34114 | OAD Industries Inc | Rancho Bernardo CA | 92127 |
| 34333 | Silicon General Inc | Garden Grove CA | 92641 |
| 34335 | Advanced Micro Devices Inc | Sunnyvale CA | 94086 |
| 34371 | Harris Semicon Div Harris-Intertype | Melbourne FL | 32901 |
| 34649 | Intel Corp | Santa Clara CA | 95051 |
| 35860 | Canadian Standards Assn | Rexdale ONT | |
| 46384 | Penn Engineering and Mfg Corp | Danboro PA | |
| 51633 | Fluorocarbon Co | Sunnyvale CA | 94088 |
| 54013 | Randolph and Baldwin Inc | Waltham MA | 02154 |
| 55285 | Bergquist Co | Minneapolis MN | 55099 |
| 55680 | Michicon/America Corp | Schaumburg IL | 60195 |
| 70318 | Allmetal Screw Products Inc | Garden City NY | 11530 |
| 71482 | Clare Div of General Instrument | Chicago IL | 60645 |
| 71707 | Coto Corp | Providence RI | 02905 |
| 71279 | Midland-Ross Corp | Cambridge MA | 02140 |
| 73138 | Beckman Instruments Inc Helipot Div | Fullerton CA | 92634 |
| 73734 | Federal Screw Products Inc | Chicago IL | 60618 |
| 75042 | TRW Electronic Components | Philadelphia PA | 19108 |
| 75263 | Keystone Carbon Co | St Marys PA | 15857 |
| 75915 | Littelfuse Inc | Des Plaines IL | 60016 |
| 76381 | Minnesota Mining and Manufacturing | St Paul MN | 55101 |
| 76854 | Oak Switch Systems Inc | Crystal Lake IL | 60014 |
| 77250 | Allied Products Corp | Chicago IL | 60650 |
| 77902 | Rohm and Maas Co | Philadelphia PA | 19105 |
| 82877 | Rotron Inc Custom Div | Woodstock NY | 12498 |
| 83486 | Elco Industries | Rockford IL | 61101 |
| 84411 | TRW Capacitor Div | Ogallala NE | 69153 |
| 84830 | Lee Spring Co | Brooklyn NY | 11219 |
| 86928 | Seastrom Mfg Co | Glendale CA | 91201 |
| 90949 | United States Steel Corp | San Francisco CA | 94101 |
| 91345 | Miller Dial Corp | El Monte CA | 91734 |
| 91637 | Dale Electronics Div | Columbus NE | 68601 |
| 98291 | Sealectro Corp | Trumbull CT | 06611 |
| 98978 | Intl Electronic Research Corp | Burbank CA | 91510 |
| 99484 | Flexsteel Industries Inc | Dubuque IA | 52001 |

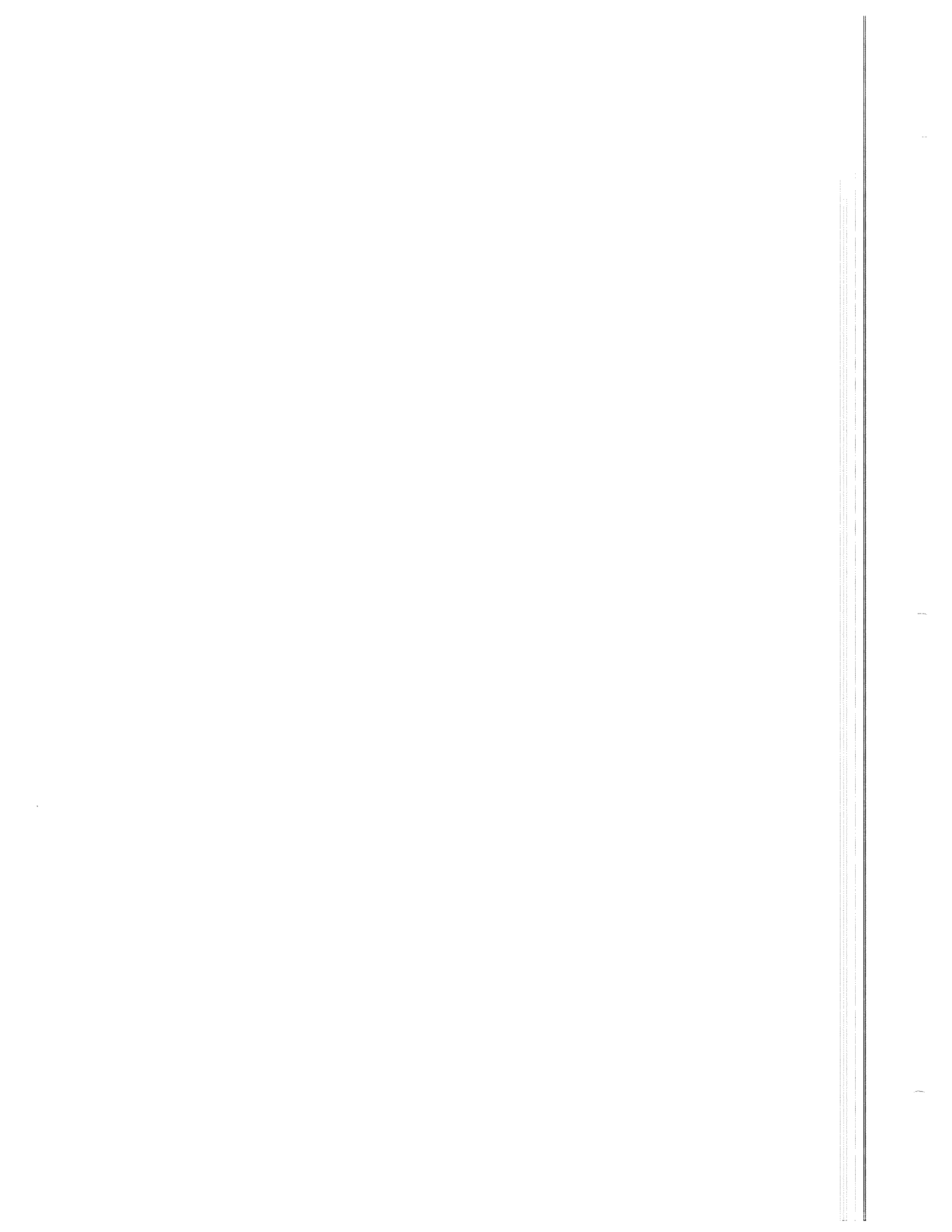


Table 4-3 Replaceable Parts

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|----------------------|
| A1 | 03562-66501 | | 5 | PC BOARD ASSY | 28480 | 03562-66501 |
| A1C1 | 0180-0094 | | 4 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2-DSM |
| A1C200-C240 | 0160-4571 | | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A1C405 | 0160-4571 | | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A1C414 | 0180-0116 | | 1 | CAPACITOR-FXD 6.8UF+-10% 35VDC TA | 13606 | 150D685X9035B2-DYS |
| A1C416-C417 | 0160-0127 | | 2 | CAPACITOR-FXD 1UF +-20% 25VDC CER | 13606 | 2C3725U105M025A |
| A1C418-C419 | 0160-4571 | | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A1C420 | 0160-4811 | | 4 | CAPACITOR-FXD 270PF +-5% 100VDC CER | 27167 | CAC02COG271J100A |
| A1C421-C424 | 0160-4571 | | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A1C425 | 0180-0116 | | 1 | CAPACITOR-FXD 6.8UF+-10% 35VDC TA | 13606 | 150D685X9035B2-DYS |
| A1C502 | 0160-4571 | | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A1CR501-CR502 | 1901-1080 | | 1 | DIODE-SCHOTTKY 1N5817 20V 1A | 04713 | SBR5120KBRL |
| A1CR503 | 1902-0025 | | 4 | DIODE-ZNR 10V 5% DO-35 PD=.4W TC=+.06% | 04713 | SZ30016-1182 |
| A1J2 | 1251-5202 | | 2 | CONN-POST TYPE .125-PIN-SPCG 5-CONT | 22526 | 65580-105 |
| A1J3 | 1251-4670 | | 2 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A1J10 | 1250-1255 | | 1 | CONNECTOR-RF SMB M PC 50-OHM | 98291 | 51-051-0000 |
| A1J701-J705 | 1251-4670 | | 2 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A1P1 | 1251-7506 | | 9 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A1Q1 | 1853-0036 | | 2 | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 04713 | SPS-3612 |
| A1R1 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R4-R6 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R103 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R302-R305 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R403 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R501 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R502 | 0837-0275 | | 6 | THERMISTOR DISC 50-OHM TC=+2.35%/C-DEG | 75263 | RL3006-50-110-25-PTO |
| A1R505-R506 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R507 | 0683-1055 | | 5 | RESISTOR 1M 5% .25W CF TC=0-800 | 77902 | R-25J |
| A1R508-R511 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R600 | 0683-1025 | | 9 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R601 | 0683-1035 | | 1 | RESISTOR 10K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R602-R603 | 0683-2025 | | 1 | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1R604 | 0683-4705 | | 8 | RESISTOR 47 5% .25W CF TC=0-400 | 77902 | R-25J |
| A1RP401 | 1810-0204 | | 6 | NETWORK-RES 8-SIP 1.0K OHM X 7 | 11236 | 750-81-R1K |
| A1TP1-TP15 | 1251-0600 | | 15 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A1U1-U2 | 1820-2779 | | 5 | IC CNTR TTL ALS BIN SYNCHRO | 01295 | SN71537N |
| A1U3 | 03562-60324 | | 8 | SW ASSY-BW | 28480 | 03562-60324 |
| A1U4 | 1820-2656 | | 7 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A1U5 | 03562-60325 | | 9 | PROGRAMMED PAL | 28480 | 03562-60325 |
| A1U6 | 1820-2635 | | 2 | IC GATE TTL ALS AND QUAD 2-INP | 01295 | SN71172N |
| A1U7 | 1820-3144 | | 3 | IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG | 01295 | SN71560N |
| A1U8-U9 | 1820-2488 | | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A1U10 | 1820-1433 | | 6 | IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT | 01295 | SN57194 |
| A1U11-U12 | 1820-2757 | | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A1U13 | 1820-1922 | | 8 | IC SHF-RGTR TTL LS PRL-IN SERIAL-OUT | 01295 | SN58781N |
| A1U14 | 1820-2488 | | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A1U101 | 1820-1244 | | 7 | IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL | 01295 | SN53619 |
| A1U102 | 03562-60326 | | 0 | PROGRAMMED PAL | 28480 | 03562-60326 |
| A1U103 | 1820-1195 | | 7 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN53526 |
| A1U104 | 1820-2096 | | 9 | IC CNTR TTL LS BIN DUAL 4-BIT | 01295 | SN59197N |
| A1U105 | 1820-1244 | | 7 | IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL | 01295 | SN53619 |
| A1U106 | 1820-2488 | | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A1U107-U108 | 1820-3144 | | 0 | IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG | 01295 | SN71560N |
| A1U109 | 1820-2657 | | 8 | IC GATE TTL ALS OR QUAD 2-INP | 01295 | SN71173N |
| A1U110 | 1820-1433 | | 6 | IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT | 01295 | SN57194 |
| A1U111-U112 | 1820-2757 | | 9 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A1U113 | 1820-2201 | | 8 | IC SHF-RGTR TTL LS COM CLEAR SERIAL-OUT | 01295 | SN59874N |
| A1U201 | 1820-1144 | | 6 | IC GATE TTL LS NOR QUAD 2-INP | 01295 | SN53243 |
| A1U202 | 1820-2634 | | 1 | IC INV TTL ALS HEX | 01295 | SN71332N |
| A1U203-U204 | 1820-1730 | | 6 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN58039 |
| A1U205 | 1820-1278 | | 7 | IC CNTR TTL LS BIN UP/DOWN SYNCHRO | 01295 | SN53646 |
| A1U206-U207 | 1820-1975 | | 1 | IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN | 01295 | SN58817N |
| A1U208 | 1820-1281 | | 2 | IC DCDR TTL LS 2-TO-4-LINE DUAL | 01295 | SN53657 |
| A1U209 | 1820-2120 | | 0 | IC MULTR TTL LS 8-BIT | 34335 | AN25LS14ADC |
| A1U210 | 1820-1730 | | 6 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN58039 |
| A1U212 | 1820-1441 | | 6 | IC ADDR TTL LS BIN FULL ADDR 4-BIT | 01295 | SN57202 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A1U301 | 1820-1074 | 1 | 1 | IC DRVR TTL NOR QUAD 2-INP | 01295 | SN43266 |
| A1U302 | 1820-2634 | 1 | 1 | IC INV TTL ALS HEX | 01295 | SN71332N |
| A1U303 | 03562-60328 | 2 | 1 | SW ASSY-BW | 28480 | 03562-60328 |
| A1U304 | 1820-1730 | 6 | 1 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN58039 |
| A1U305 | 1820-3093 | 8 | 1 | IC-8000-SERIES PROGRAMMABLE TIMER | 34649 | P8254 |
| A1U306-U307 | 1820-2757 | 9 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A1U308 | 1820-1470 | 1 | 1 | IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD | 01295 | SN53524 |
| A1U310 | 1820-1730 | 0 | 1 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN58039 |
| A1U311 | 1820-1297 | 6 | 1 | IC GATE TTL LS EXCL-NOR QUAD 2-INP | 01295 | SN53659 |
| A1U312 | 1820-1441 | 6 | 1 | IC ADDR TTL LS BIN FULL ADDR 4-BIT | 01295 | SN57202 |
| A1U313 | 03562-60327 | 1 | 1 | PROGRAMMED PROM | 28480 | 03562-60327 |
| A1U401 | 1820-1195 | 7 | 1 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN53526 |
| A1U402 | 1820-2775 | 1 | 1 | IC GATE TTL ALS NAND TPL 3-INP | 01295 | SN71546N |
| A1U403 | 1820-2710 | 4 | 1 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71708N |
| A1U404 | 1820-2740 | 0 | 1 | IC COMPTR TTL LS MAGTD 2-INP 8-BIT | 34335 | AM25LS2521PC |
| A1U405-U406 | 1820-3362 | 4 | 2 | IC TRANSCEIVER TTL ALS BUS OCTL | 01295 | SN71879N |
| A1U407 | 1820-1077 | 4 | 1 | IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD | 01295 | SN43268 |
| A1U409 | 1820-2757 | 9 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A1U410-U413 | 1820-3423 | 8 | 4 | IC SHF-RCTR TTL LS ASYNCHRO SERIAL-IN | 01295 | SN74LS959N |
| A1U414 | 1820-0493 | 6 | 1 | IC OP AMP GP 8-DIP-P PKG | 27014 | SL10084 |
| A1U415 | 1826-0065 | 0 | 1 | IC COMPARATOR PRCN 8-DIP-P PKG | 27014 | SL14334 |
| A1U601 | 1820-3349 | 7 | 1 | IC BFR TTL ALS NAND QUAD 2-INP | 01295 | SN71692N |
| | 1258-0141 | 8 | 6 | JMPR-REM .025P | 22526 | 65474-004 |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | 601016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| A2 | 03562-66502 | 6 | 1 | PC BOARD ASSY CPU/HPIB | 28480 | 03562-66502 |
| A2B1 | 1420-0301 | 7 | 1 | BATTERY 3.4V 1.8A-HR LITHIUM THIONYL | T01139 | 15-51-03-410-000 |
| A2C1 | 0180-0094 | 4 | 1 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2-DSM |
| A2C4 | 0180-0228 | 6 | 1 | CAPACITOR-FXD 22UF+10% 15VDC TA | 13606 | 150D226X9015B2-DYS |
| A2C100-C101 | 0160-4571 | 8 | 55 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C103-C105 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C107 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C109-C110 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C112-C113 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C204-C205 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C207 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C209-C212 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C303-C306 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C404 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C406-C410 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C412-C413 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C500 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C503-C512 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C600-C602 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C604-C611 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2C700-C703 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A2CR1 | 1902-0947 | 9 | 1 | DIODE-ZNR 3.6V 5% DO-35 PD=.4W TC=-.036% | 04713 | SZ30035-005 |
| A2CR2 | 1901-0539 | 3 | 1 | DIODE-SCHOTTKY SM SIG | 28480 | 1901-0539 |
| A2CR4 | 1901-0539 | 3 | 2 | DIODE-SCHOTTKY SM SIG | 28480 | 1901-0539 |
| A2DS1 | 1990-0486 | 6 | 1 | LED-LAMP LUM-INT=2MCD IF=25MA-MAX BVR=5V | 28480 | 1990-0486 |
| A2DS2 | 1990-0622 | 2 | 1 | LED-LAMP ARRAY LUM-INT=200UCD | 28480 | 1990-0622 |
| A2DS3-DS4 | 1990-0652 | 8 | 1 | LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX | 28480 | 1990-0652 |
| A2J1 | 1251-6515 | 8 | 2 | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A2J2 | 1251-5202 | 8 | 1 | CONN-POST TYPE .125-PIN-SPCG 5-CONT | 22526 | 65580-105 |
| A2J4-J7 | 1252-0169 | 8 | 1 | 3X8 CONN JUMPER POST | 22526 | 1252-0169 |
| A2J8-J10 | 1251-4670 | 2 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A2J11 | 1251-6515 | 8 | 1 | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A2J12-J13 | 1251-4670 | 2 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A2J14 | 1251-6515 | 8 | 1 | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A2J15-J18 | 1251-4670 | 2 | 10 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A2J20 | 1251-7229 | 3 | 1 | CONN-POST TYPE .100-PIN-SPCG 26-CONT | 28480 | 1251-7229 |
| A2J21 | 1251-4670 | 2 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A2P1 | 1251-7506 | 9 | 1 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A2Q1 | 1854-0215 | 1 | 1 | TRANSISTOR NPN SI PD=350MW FT=300MHZ | 04713 | SPS 3611 |
| A2Q2 | 1853-0393 | 4 | 1 | TRANSISTOR PNP SI TO-18 PD=500MW | 04713 | SPS 7011 |
| A2Q3-Q9 | 1854-0094 | 4 | 1 | TRANSISTOR NPN SI PD=200MW FT=350MHZ | 04713 | SPS 234 |

See introduction to this section for ordering information
*Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------------------|
| A2R1-R2 | 0757-0280 | 3 | 15 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R3 | 0757-0398 | 4 | 1 | RESISTOR 75 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R4 | 0757-0417 | 8 | 1 | RESISTOR 562 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R5 | 0757-0411 | 2 | 1 | RESISTOR 332 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R6 | 0757-0346 | 2 | 1 | RESISTOR 10 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A2R7-R8 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R9-R10 | 0757-0442 | 9 | 2 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R11 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R12-R16 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R17 | 0757-0451 | 0 | 1 | RESISTOR 24.3K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R18-R19 | 0698-4470 | 5 | 2 | RESISTOR 6.98K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A2R20 | 0698-3447 | 4 | 1 | RESISTOR 422 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R21 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R22 | 0698-3152 | 8 | 1 | RESISTOR 3.48K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R23 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R24 | 0757-0288 | 1 | 1 | RESISTOR 9.09K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R25 | 0698-3558 | 8 | 2 | RESISTOR 4.02K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R26-R27 | 0698-3450 | 9 | 4 | RESISTOR 42.2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R28 | 0757-0199 | 3 | 2 | RESISTOR 21.5K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R29-R30 | 0698-3450 | 9 | | RESISTOR 42.2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R31 | 0698-3158 | 4 | 1 | RESISTOR 23.7K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R32 | 0757-0199 | 3 | | RESISTOR 21.5K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R33-R34 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R35 | 0698-3558 | 8 | | RESISTOR 4.02K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R36 | 0757-0401 | 0 | 2 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R37 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R38 | 0757-0416 | 7 | 1 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2R50 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A2RP1-RP2 | 1810-0277 | 3 | | NETWORK-RES 10-SIP 2.2K OHM X 9 | 91637 | CSC10A01-222G/MSP10A01-222G |
| A2RP3 | 1810-0279 | 5 | 1 | NETWORK-RES 10-SIP 4.7K OHM X 9 | 91637 | CSC10A01-472G/MSP10A01-472G |
| A2RP4-RP5 | 1810-0277 | 3 | | NETWORK-RES 10-SIP 2.2K OHM X 9 | 91637 | CSC10A01-222G/MSP10A01-222G |
| A2S1 | 3101-2170 | 8 | 1 | SWITCH-PB SPDT MOM | 09353 | 8125-D8AE |
| A2TP1-TP6 | 1251-0600 | 0 | | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A2U100 | 1820-2505 | 5 | 1 | IC-MPU; CLK FREQ=8MHZ, INSTRUCTION | 04713 | SC88072L |
| A2U103 | 1820-2882 | 1 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| A2U104 | 1820-2861 | 6 | 1 | IC DCNR TTL F 3-TO-8-LINE | 07263 | 74F138PC |
| A2U105 | 03562-60333 | 9 | 1 | PROGRAMMED EPROM | 28480 | 03562-60333 |
| A2U105 | 1200-0567 | 1 | 2 | SOCKET-IC 28-CONT DIP DIP-SLDR | 09922 | DILB28P-308T |
| A2U107 | 1818-3183 | 2 | 8 | IC CMOS 65536 (64K) STAT RAM 150-NS 3-S | 54013 | HM6264LP-15 |
| A2U109-U110 | 1818-3183 | 2 | | IC CMOS 65536 (64K) STAT RAM 150-NS 3-S | 54013 | HM6264LP-15 |
| A2U112 | 1820-3431 | 8 | 1 | IC TRANSCEIVER TTL S INSTR-BUS IEEE-488 | 27014 | DS75160AN |
| A2U113 | 1820-3513 | 7 | 1 | IC TRANSCEIVER TTL S INSTR-BUS IEEE-488 | 27014 | DS75161AN |
| A2U204 | 1820-2656 | 7 | 3 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A2U205 | 03562-60334 | 0 | 1 | PROGRAMMED EPROM | 28480 | 03562-60334 |
| A2U205 | 1200-0567 | 1 | | SOCKET-IC 28-CONT DIP DIP-SLDR | 09922 | DILB28P-308T |
| A2U207 | 1818-3183 | 2 | | IC CMOS 65536 (64K) STAT RAM 150-NS 3-S | 54013 | HM6264LP-15 |
| A2U209-U212 | 1818-3183 | 2 | | IC CMOS 65536 (64K) STAT RAM 150-NS 3-S | 54013 | HM6264LP-15 |
| A2U303 | 1820-2656 | 7 | | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A2U304 | 1820-2657 | 8 | 2 | IC GATE TTL ALS OR QUAD 2-INP | 01295 | SN71173N |
| A2U305 | 03562-60332 | 8 | 1 | PROGRAMMED PAL | 28480 | 03562-60332 |
| A2U406 | 1820-2739 | 7 | 1 | IC GATE TTL ALS NOR QUAD 2-INP | 01295 | SN71336N |
| A2U404 | 1820-2947 | 9 | 1 | IC DIVR TTL LS BIN | 01295 | SN71558N |
| A2U406 | 1820-2656 | 7 | | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A2U407 | 1820-2488 | 3 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A2U408 | 1820-2923 | 1 | 1 | IC GATE CMOS/74HC NAND TPL 3-INP | 04713 | MC74HC10N |
| A2U409 | 1820-2657 | 8 | | IC GATE TTL ALS OR QUAD 2-INP | 01295 | SN71173N |
| A2U410 | 1820-1433 | 6 | 1 | IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT | 01295 | SN57194 |
| A2U412 | 1820-2548 | 6 | 1 | IC-GENERAL PURPOSE INTERFACE BUS ADAPTER | 01295 | MP9203NL |
| A2U413 | 1820-2469 | 0 | 1 | IC-PROGRAMMABLE TIMER, 3 TIME INTERVALS | 04713 | SC67515P |
| A2U500 | 1820-1851 | 2 | 1 | IC ENCDR TTL LS | 01295 | SN70488N |
| A2U503 | 1820-0684 | 7 | 1 | IC INV TTL S HEX 1-INP | 01295 | SN24652 |
| A2U504 | 03562-60329 | 3 | 1 | PROGRAMMED PAL | 28480 | 03562-60329 |
| A2U505 | 1820-3649 | 0 | 1 | IC-D 74F164 TTL F SHFRGT P14 | 07263 | 74F164PC |
| A2U506-U507 | 1820-3362 | 4 | | IC TRANSCEIVER TTL ALS BUS OCTL | 01295 | SN71879N |
| A2U508 | 1820-2795 | 5 | 2 | IC DRVR TTL F LINE DRVR OCTL | 07263 | SM83462 |
| A2U509 | 1820-2882 | 1 | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| A2U510 | 1820-2710 | 4 | | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71708N |
| A2U511 | 1820-2882 | 1 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-------------------|
| A2U512 | 1820-2710 | 4 | | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71708N |
| A2U600 | 1820-2684 | 1 | 1 | IC GATE TTL F NAND QUAD 2-INP | 07263 | SL82676 |
| A2U601 | 1820-2779 | 5 | 1 | IC CNTR TTL ALS BIN SYNCHRO | 01295 | SN71537N |
| A2U602 | 1820-3185 | 9 | 1 | IC SCHMITT-TRIG CMOS/74HC INV HEX | 27014 | MM74HC14N |
| A2U604 | 1820-2795 | 5 | | IC DRVR TTL F LINE DRVR OCTL | 07263 | SM83462 |
| A2U605 | 03562-60331 | 7 | 1 | PROGRAMMED PAL | 28480 | 03562-60331 |
| A2U606 | 03562-60330 | 6 | 1 | PROGRAMMED PAL | 28480 | 03562-60330 |
| A2U607-U609 | 1820-2698 | 7 | 3 | IC DRVR TTL F LINE DRVR OCTL | 07263 | SL82820 |
| A2U610-U611 | 1820-2710 | 4 | 4 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71708N |
| A2U700 | 1813-0130 | 3 | 1 | CRYSTAL CLKOSC 16MHZ MCAN | 04713 | RASCO-2-16MHZ |
| A2U701 | 1820-1450 | 7 | 1 | IC BFR TTL S NAND QUAD 2-INP | 01295 | SN85496 |
| A2U702-U703 | 1820-0697 | 2 | 2 | IC DRVR TTL S NAND LINE DUAL 4-INP | 01295 | SN24665 |
| A2W1 | 1258-0141 | 8 | 13 | JMPR-REM .025P | 22526 | 65474-004 |
| A2W3 | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A2W4-W7 | 1258-0218 | 0 | 4 | JUMPER, 16 CKT, CONN | 22526 | 76266-108 |
| A2W8-W18 | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | G01016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| A3 | 03562-66503 | 7 | 1 | ASSY, ROM | 28480 | 03562-66503 |
| A3C1-C3 | 0160-4571 | 8 | 54 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A3C5 | 0180-0094 | 4 | 1 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2-DSM |
| A3C10-C15 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A3C21-C23 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A3C100-C120 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A3C200-C220 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A3J1 | 1251-5202 | 2 | 1 | CONN-POST TYPE .125-PIN-SPCG 5-CONT | 22526 | 65580-105 |
| A3J2 | 1251-4670 | 2 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A3MP684 | 1200-0567 | 1 | 40 | SOCKET-IC 28-CONT DIP DIP-SLDR | 09922 | DIL828P-308T |
| A3P3 | 1251-7506 | 9 | 1 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A3R1-R21 | 0757-0384 | 8 | 41 | RESISTOR 20 1% .125W F TC=0+-100 | 19701 | 5033R |
| A3R29-R37 | 8150-3375 | 5 | 12 | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A3R40-R41 | 8150-3375 | 5 | | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A3R42 | 0757-0280 | 3 | 4 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A3R50 | 8150-3375 | 5 | | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A3R51-R53 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A3R101-R120 | 0757-0384 | 8 | | RESISTOR 20 1% .125W F TC=0+-100 | 19701 | 5033R |
| A3TP1-TP3 | 1251-0600 | 0 | 3 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A3U1-U3 | 1820-2698 | 7 | | IC DRVR TTL F LINE DRVR OCTL | 07263 | SL82820 |
| A3U10 | 1820-2685 | 2 | 1 | IC GATE TTL F NOR QUAD 2-INP | 07263 | SL82677 |
| A3U11 | 1820-2692 | 1 | 1 | IC GATE TTL F EXCL-OR QUAD 2-INP | 07263 | SL82686 |
| A3U12 | 1820-2689 | 6 | 1 | IC GATE TTL F NAND DUAL 4-INP | 07263 | SL82682 |
| A3U13-U14 | 1820-2691 | 0 | 2 | IC FF TTL F D-TYPE POS-EDGE-TRIG | 07263 | SL82685 |
| A3U15 | 1820-0687 | 0 | 1 | IC GATE TTL S AND TPL 3-INP | 01295 | SN24655 |
| A3U21-U23 | 1820-2861 | 6 | 3 | IC DCDR TTL F 3-TO-8-LINE | 07263 | 74F138PC |
| A3U100 | 1820-2698 | 7 | | IC DRVR TTL F LINE DRVR OCTL | 07263 | SL82820 |
| A3U101 | 03562-60343 | 1 | 1 | PROGRAMMED EPROM | 28480 | 03562-60343 |
| A3U102 | 03562-60344 | 2 | 1 | PROGRAMMED EPROM | 28480 | 03562-60344 |
| A3U103 | 03562-60345 | 3 | 1 | PROGRAMMED EPROM | 28480 | 03562-60345 |
| A3U104 | 03562-60346 | 4 | 1 | PROGRAMMED EPROM | 28480 | 03562-60346 |
| A3U105 | 03562-60347 | 5 | 1 | PROGRAMMED EPROM | 28480 | 03562-60347 |
| A3U106 | 03562-60348 | 6 | 1 | PROGRAMMED EPROM | 28480 | 03562-60348 |
| A3U107 | 03562-60349 | 7 | 1 | PROGRAMMED EPROM | 28480 | 03562-60349 |
| A3U108 | 03562-60350 | 0 | 1 | PROGRAMMED EPROM | 28480 | 03562-60350 |
| A3U109 | 03562-60351 | 1 | 1 | PROGRAMMED EPROM | 28480 | 03562-60351 |
| A3U110 | 03562-60352 | 2 | 1 | PROGRAMMED EPROM | 28480 | 03562-60352 |
| A3U111 | 03562-60353 | 3 | 1 | PROGRAMMED EPROM | 28480 | 03562-60353 |
| A3U112 | 03562-60354 | 4 | 1 | PROGRAMMED EPROM | 28480 | 03562-60354 |
| A3U113 | 03562-60355 | 5 | 1 | PROGRAMMED EPROM | 28480 | 03562-60355 |
| A3U114 | 03562-60356 | 6 | 1 | PROGRAMMED EPROM | 28480 | 03562-60356 |
| A3U115 | 03562-60357 | 7 | 1 | PROGRAMMED EPROM | 28480 | 03562-60357 |
| A3U116 | 03562-60358 | 8 | 1 | PROGRAMMED EPROM | 28480 | 03562-60358 |
| A3U117 | 03562-60359 | 9 | 1 | PROGRAMMED EPROM | 28480 | 03562-60359 |
| A3U118 | 03562-60360 | 2 | 1 | PROGRAMMED EPROM | 28480 | 03562-60360 |
| A3U119 | 03562-60361 | 3 | 1 | PROGRAMMED EPROM | 28480 | 03562-60361 |
| A3U120 | 03562-60362 | 4 | 1 | PROGRAMMED EPROM | 28480 | 03562-60362 |
| A3U200 | 1820-2698 | 7 | | IC DRVR TTL F LINE DRVR OCTL | 07263 | SL82820 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|---------------------------------------|----------|-------------------|
| A3U201 | 03562-60363 | 5 | 1 | PROGRAMMED EPROM | 28480 | 03562-60363 |
| A3U202 | 03562-60364 | 6 | 1 | PROGRAMMED EPROM | 28480 | 03562-60364 |
| A3U203 | 03562-60365 | 7 | 1 | PROGRAMMED EPROM | 28480 | 03562-60365 |
| A3U204 | 03562-60366 | 8 | 1 | PROGRAMMED EPROM | 28480 | 03562-60366 |
| A3U205 | 03562-60367 | 9 | 1 | PROGRAMMED EPROM | 28480 | 03562-60367 |
| A3U206 | 03562-60368 | 0 | 1 | PROGRAMMED EPROM | 28480 | 03562-60368 |
| A3U207 | 03562-60369 | 1 | 1 | PROGRAMMED EPROM | 28480 | 03562-60369 |
| A3U208 | 03562-60370 | 4 | 1 | PROGRAMMED EPROM | 28480 | 03562-60370 |
| A3U209 | 03562-60371 | 5 | 1 | PROGRAMMED EPROM | 28480 | 03562-60371 |
| A3U210 | 03562-60372 | 6 | 1 | PROGRAMMED EPROM | 28480 | 03562-60372 |
| A3U211 | 03562-60373 | 7 | 1 | PROGRAMMED EPROM | 28480 | 03562-60373 |
| A3U212 | 03562-60374 | 8 | 1 | PROGRAMMED EPROM | 28480 | 03562-60374 |
| A3U213 | 03562-60388 | 4 | 1 | PROGRAMMED EPROM | 28480 | 03562-60388 |
| A3U214 | 03562-60389 | 5 | 1 | PROGRAMMED EPROM | 28480 | 03562-60389 |
| A3U215 | 03562-60390 | 8 | 1 | PROGRAMMED EPROM | 28480 | 03562-60390 |
| A3U216 | 03562-60391 | 9 | 1 | PROGRAMMED EPROM | 28480 | 03562-60391 |
| A3U217 | 03562-60392 | 0 | 1 | PROGRAMMED EPROM | 28480 | 03562-60392 |
| A3U218 | 03562-60393 | 1 | 1 | PROGRAMMED EPROM | 28480 | 03562-60393 |
| A3U219 | 03562-60394 | 2 | 1 | PROGRAMMED EPROM | 28480 | 03562-60394 |
| A3U220 | 03562-60395 | 3 | 1 | PROGRAMMED EPROM | 28480 | 03562-60395 |
| | 1258-0141 | 8 | 4 | JMPR-REM .025P | 22526 | 65474-004 |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | G01016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| A4 | 03562-66504 | 8 | 1 | ASSY, L O | 28480 | 03562-66504 |
| A4C2 | 0160-4571 | 8 | 46 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C4-C5 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C7 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C9-C10 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C12 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C14-C15 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C17 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C19-C20 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C22 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C24 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C26 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C28-C29 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C31 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C33-C34 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C36-C38 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C40 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C42-C43 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C45 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C47-C48 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C50 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C52-C55 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C57 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C59 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C61-C62 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C64 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C66 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C68 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C70-C73 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C75 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A4C100 | 0180-0094 | 4 | 1 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2-DSM |
| A4J1 | 1251-5202 | 8 | 1 | CONN-POST TYPE .125-PIN-SPCG 5-CONT | 22526 | 65580-105 |
| A4P1 | 1251-7506 | 9 | 1 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A4R14 | 0757-0280 | 3 | 35 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A4R17 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A4R21 | 8150-3375 | 5 | 1 | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A4R23 | 8150-3375 | 5 | | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A4R25 | 8150-3375 | 5 | | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A4R31 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A4R34 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A4R36 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A4R37 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A4R39 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------|
| A4R41 | 0757-0280 | 3 | | RESISTOR 1K 1/4 .125W F TC=0+-100 | 19701 | 5033R |
| A4R46-R55 | 0757-0280 | 3 | | RESISTOR 1K 1/4 .125W F TC=0+-100 | 19701 | 5033R |
| A4R59 | 0757-0280 | 3 | | RESISTOR 1K 1/4 .125W F TC=0+-100 | 19701 | 5033R |
| A4R62 | 0757-0280 | 3 | | RESISTOR 1K 1/4 .125W F TC=0+-100 | 19701 | 5033R |
| A4R64-R67 | 0757-0280 | 3 | | RESISTOR 1K 1/4 .125W F TC=0+-100 | 19701 | 5033R |
| A4R69 | 0757-0280 | 3 | | RESISTOR 1K 1/4 .125W F TC=0+-100 | 19701 | 5033R |
| A4R70-R77 | 0757-0280 | 3 | | RESISTOR 1K 1/4 .125W F TC=0+-100 | 19701 | 5033R |
| A4TP1-TP24 | 1251-0600 | 0 | 29 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A4TP30-TP34 | 1251-0600 | 0 | | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A4U1 | 1820-3318 | 0 | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71690N |
| A4U2-U3 | 1816-0724 | 7 | | IC TTL S 64-BIT STAT RAM 35-NS 3-S | 01295 | SN86666N |
| A4U4 | 1820-1470 | 1 | | IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD | 01295 | SN53524 |
| A4U5-U6 | 1820-3318 | 0 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71690N |
| A4U7-U8 | 1816-0724 | 7 | | IC TTL S 64-BIT STAT RAM 35-NS 3-S | 01295 | SN86666N |
| A4U9 | 1820-1470 | 1 | | IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD | 01295 | SN53524 |
| A4U10 | 1816-0724 | 7 | | IC TTL S 64-BIT STAT RAM 35-NS 3-S | 01295 | SN86666N |
| A4U11 | 1820-1871 | 6 | 2 | IC ADDR TTL S BIN FULL ADDR 4-BIT | 01295 | SN44449N |
| A4U12 | 1820-1444 | 9 | 1 | IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD | 01295 | SN57205 |
| A4U13 | 03562-60340 | 8 | 1 | PROGRAMMED PROM | 28480 | 03562-60340 |
| A4U14 | 1820-2691 | 0 | 4 | IC FF TTL F D-TYPE POS-EDGE-TRIG | 07263 | SL82685 |
| A4U15 | 1816-0724 | 7 | | IC TTL S 64-BIT STAT RAM 35-NS 3-S | 01295 | SN86666N |
| A4U16 | 1820-1871 | 6 | | IC ADDR TTL S BIN FULL ADDR 4-BIT | 01295 | SN44449N |
| A4U17 | 1820-1195 | 7 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN53526 |
| A4U18-U19 | 1820-2757 | 9 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| Δ A4U20 | 03562-60342 | 0 | | PROGRAMMED EPROM | 28480 | 03562-60342 |
| A4U21-U23 | 1820-2757 | 9 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A4U24 | 1820-3362 | 4 | 1 | IC TRANSCEIVER TTL ALS BUS OCTL | 01295 | SN71879N |
| A4U25-U27 | 1820-2757 | 9 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| Δ A4U28 | 1820-2710 | 4 | 1 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71708N |
| A4U29 | 03562-60341 | 9 | | PROGRAMMED PROM | 28480 | 03562-60341 |
| A4U30 | 1820-1300 | 6 | | IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT | 01295 | SN53662 |
| A4U31 | 1820-1195 | 7 | 4 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN53526 |
| A4U32 | 03562-60339 | 5 | 1 | PROGRAMMED PAL | 28480 | 03562-60339 |
| A4U33 | 1820-2711 | 5 | 1 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71504N |
| A4U34-U35 | 1820-1300 | 6 | 4 | IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT | 01295 | SN53662 |
| A4U36 | 1820-2180 | 2 | 1 | IC-PERIPHERAL INTERFACE ADAPTER (PIA) | 04713 | SC67312L |
| A4U37 | 1820-2311 | 1 | 1 | IC COMPR TTL LS MAGTD 8-BIT | 34335 | AM25LS2521PC |
| A4U38 | 1820-1300 | 6 | | IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT | 01295 | SN53662 |
| A4U39 | 1820-1458 | 5 | 1 | IC ARITH-LGC-UN TTL S 4-BIT | 01295 | SN85504 |
| A4U40 | 1820-2656 | 7 | 2 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A4U41-U42 | 1820-3423 | 8 | | IC SHF-RGTR TTL LS ASYNCHRO SERIAL-IN | 01295 | SN74HS595N |
| A4U43-U44 | 1820-2757 | 9 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A4U45 | 1820-2506 | 6 | 2 | IC INV TTL F HEX | 07263 | SL82678 |
| A4U46 | 1820-2691 | 0 | | IC FF TTL F D-TYPE POS-EDGE-TRIG | 07263 | SL82685 |
| A4U47 | 1820-2488 | 3 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A4U48-U49 | 1820-2757 | 9 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A4U50 | 1820-2691 | 0 | | IC FF TTL F D-TYPE POS-EDGE-TRIG | 07263 | SL82685 |
| A4U51 | 1820-1195 | 7 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN53526 |
| A4U52 | 1820-0688 | 1 | 1 | IC GATE TTL S NAND DUAL 4-INP | 01295 | SN24656 |
| A4U53-U54 | 1820-3669 | 4 | | IC-D 74LS674 TTL LS SHFRGT P24 | 01295 | SN74LS674N |
| A4U55 | 03562-60338 | 4 | 1 | PROGRAMMED PAL | 28480 | 03562-60338 |
| A4U56 | 03562-60337 | 3 | 1 | PROGRAMMED PAL | 28480 | 03562-60337 |
| A4U57 | 1820-1470 | 1 | 3 | IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD | 01295 | SN53524 |
| A4U58 | 03562-60336 | 2 | 1 | PROGRAMMED PAL | 28480 | 03562-60336 |
| A4U59 | 1820-2692 | 1 | 1 | IC GATE TTL F EXCL-OR QUAD 2-INP | 07263 | SL82686 |
| A4U60 | 1820-2656 | 7 | | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A4U61 | 1820-2684 | 1 | 1 | IC GATE TTL F NAND QUAD 2-INP | 07263 | SL82676 |
| A4U62 | 1820-3669 | 4 | | IC-D 74LS674 TTL LS SHFRGT P24 | 01295 | SN74LS674N |
| A4U63 | 1820-1322 | 2 | 1 | IC GATE TTL S NOR QUAD 2-INP | 01295 | SN84050 |
| A4U64 | 1820-1195 | 7 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN53526 |
| A4U65 | 1820-2777 | 3 | 1 | IC CNTR TTL ALS BIN SYNCHRO | 01295 | SN71349N |
| A4U66 | 1820-2488 | 3 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A4U67 | 1820-2506 | 6 | | IC INV TTL F HEX | 07263 | SL82678 |
| A4U68 | 03562-60335 | 1 | 1 | PROGRAMMED PAL | 28480 | 03562-60335 |
| A4U69 | 1820-2739 | 7 | | IC GATE TTL ALS NOR QUAD 2-INP | 01295 | SN71336N |
| A4U70 | 1820-1210 | 7 | 1 | IC GATE TTL LS AND-OR-INV DUAL 2-INP | 01295 | SN53517 |
| A4U71 | 1820-2691 | 0 | | IC FF TTL F D-TYPE POS-EDGE-TRIG | 07263 | SL82685 |
| A4U72 | 1820-2690 | 9 | 1 | IC GATE TTL F OR QUAD 2-INP | 07263 | SL82683 |
| Δ See backdating. | | | | | | |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A4U73 | 1820-2488 | 3 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A4U74 | 1820-2698 | 7 | 1 | IC DRVR TTL F LINE DRVR OCTL | 07263 | SL82820 |
| A4U75 | 1820-2795 | 5 | 1 | IC DRVR TTL F LINE DRVR OCTL | 07263 | SM83462 |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | G01016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| | 1200-0638 | 7 | 1 | SOCKET-IC 14-CONT DIP DIP-SLDR | 09922 | DILB14P-308T |
| A5 | 03562-66505 | 9 | 1 | PC BOARD ASSY DGTL FLTR | 28480 | 03562-66505 |
| A5C1-C4 | 0160-4810 | 8 | 4 | CAPACITOR-FXD 330PF +-5% 100VDC CER | 27167 | CAC02COG331J100A |
| A5C5-C7 | 0180-0374 | 3 | 1 | CAPACITOR-FXD .1UF+-10% 20VDC TA | 13606 | 150D106X9020B2-DYS |
| A5C8 | 0180-0094 | 4 | 1 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2-DSM |
| A5C9-C10 | 0180-0374 | 3 | | CAPACITOR-FXD 10UF+-10% 20VDC TA | 13606 | 150D106X9020B2-DYS |
| A5C101-C104 | 0160-4571 | 8 | 54 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C105 | 0180-0309 | 4 | 6 | CAPACITOR-FXD 4.7UF+-20% 10VDC TA | 13606 | 150D475X0010A2-DYS |
| A5C106-C108 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C109 | 0180-0309 | 4 | | CAPACITOR-FXD 4.7UF+-20% 10VDC TA | 13606 | 150D475X0010A2-DYS |
| A5C110-C141 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C142 | 0180-0309 | 4 | | CAPACITOR-FXD 4.7UF+-20% 10VDC TA | 13606 | 150D475X0010A2-DYS |
| A5C143-C148 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C150 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C152 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C154 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C156-C157 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C159-C160 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C161 | 0180-0309 | 4 | | CAPACITOR-FXD 4.7UF+-20% 10VDC TA | 13606 | 150D475X0010A2-DYS |
| A5C162 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C163 | 0180-0309 | 4 | | CAPACITOR-FXD 4.7UF+-20% 10VDC TA | 13606 | 150D475X0010A2-DYS |
| A5C164 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A5C165 | 0180-0309 | 4 | | CAPACITOR-FXD 4.7UF+-20% 10VDC TA | 13606 | 150D475X0010A2-DYS |
| A5CR1 | 1902-3114 | 8 | 1 | DIODE-ZNR 6.19V 2% DO-35 PD=.4W | 04713 | SZ30016-123 |
| A5CR2 | 1901-0734 | 0 | 1 | DIODE-PWR RECT 1N5818 30V 1A | 04713 | SBR5303 |
| A5J2-J6 | 1251-4670 | 2 | 5 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A5J7 | 1251-6515 | 8 | 1 | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A5MP600 | 03561-41101 | 8 | 6 | HEAT SINK | 28480 | 03561-41101 |
| A5MP601 | 1460-1087 | 2 | 24 | SPRING-CPRSN .24-IN-OD .375-IN-OA-LG MUV | 84830 | LC-029C-1-MW |
| A5MP685 | 1200-1011 | 2 | 6 | SOCKET-ADAPTER 65-CONT SQUARE DIP-SLDR | A01102 | C5065-01TG |
| A5P1 | 1251-7506 | 9 | 1 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A5R100 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R101-R102 | 0683-3325 | 6 | 2 | RESISTOR 3.3K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R103-R104 | 0683-1005 | 5 | 8 | RESISTOR 10 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R105 | 0698-0082 | 7 | 4 | RESISTOR 464 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R106 | 0757-0280 | 3 | 4 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R107-R108 | 0683-1005 | 5 | | RESISTOR 10 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R109 | 0698-0082 | 7 | | RESISTOR 464 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R110 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R111-R112 | 0683-1005 | 5 | | RESISTOR 10 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R113 | 0698-0082 | 7 | | RESISTOR 464 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R114 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R115-R116 | 0683-1005 | 5 | | RESISTOR 10 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R117 | 0698-0082 | 7 | | RESISTOR 464 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R118 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R119-R120 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R121 | 0683-6815 | 5 | 2 | RESISTOR 680 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R122-R124 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R125 | 0683-2415 | 3 | | RESISTOR 240 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R126 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R127 | 0683-2415 | 3 | 4 | RESISTOR 240 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R128-R129 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R130 | 0683-2415 | 3 | | RESISTOR 240 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R131-R133 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R134 | 0683-2415 | 3 | | RESISTOR 240 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R135-R136 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R137 | 0683-6815 | 5 | | RESISTOR 680 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R138-R142 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R143 | 0698-4125 | 7 | 1 | RESISTOR 953 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R144 | 0683-5115 | 6 | 1 | RESISTOR 510 5% .25W CF TC=0-400 | 77902 | R-25J |
| A5R145 | 0757-0283 | 6 | 1 | RESISTOR 2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A5R146-R152 | 0683-2025 | 1 | | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------------------|
| A5RP1-RP7 | 1810-0279 | 5 | 7 | NETWORK-RES 10-SIP 4.7K OHM X 9 | 91637 | CSC10A01-472G/MSP10A01-472G |
| A5TP1-TP24 | 1251-0600 | 0 | 24 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A5U101 | 1820-2103 | 9 | 4 | IC DRVR TTL CLK DUAL | 27014 | DS0056CJ-8 |
| A5U102 | 1820-0681 | 4 | 2 | IC GATE TTL S NAND QUAD 2-INP | 01295 | SN24649 |
| A5U103 | 1820-2103 | 9 | 9 | IC DRVR TTL CLK DUAL | 27014 | DS00056CJ-8 |
| A5U106 | 1820-2635 | 2 | 2 | IC GATE TTL ALS AND QUAD 2-INP | 01295 | SN71172N |
| A5U107 | 1820-3466 | 9 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71746N |
| A5U108 | 1820-2488 | 3 | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A5U109 | 1820-2635 | 2 | 2 | IC GATE TTL ALS AND QUAD 2-INP | 01295 | SN71172N |
| A5U110 | 1820-3466 | 9 | 9 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71746N |
| A5U111 | 1820-2488 | 3 | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A5U114 | 1820-2103 | 9 | 9 | IC DRVR TTL CLK DUAL | 27014 | DS00056CJ-8 |
| A5U115 | 1820-0681 | 4 | 4 | IC GATE TTL S NAND QUAD 2-INP | 01295 | SN24649 |
| A5U116 | 1820-2103 | 9 | 9 | IC DRVR TTL CLK DUAL | 27014 | DS00056CJ-8 |
| A5U201 | 1SC3-0033 | 5 | 4 | DECIMATION FLTR | 28480 | 1SC3-0033 |
| A5U204 | 03562-60381 | 7 | 1 | PROGRAMMED PAL | 28480 | 03562-60381 |
| A5U205 | 03562-60378 | 2 | 1 | PROGRAMMED PAL | 28480 | 03562-60378 |
| A5U206 | 1820-2757 | 9 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A5U207 | 03562-60380 | 6 | 2 | PROGRAMMED PROM | 28480 | 03562-60380 |
| A5U208 | 03562-60379 | 3 | 1 | PROGRAMMED PAL | 28480 | 03562-60379 |
| A5U209 | 03562-60380 | 6 | 6 | PROGRAMMED PROM | 28480 | 03562-60380 |
| A5U210 | 1820-2889 | 8 | 1 | IC GATE TTL ALS AND TPL 3-INP | 01295 | SN71536N |
| A5U211 | 03562-60377 | 1 | 1 | PROGRAMMED PROM | 28480 | 03562-60377 |
| A5U212 | 03562-60376 | 0 | 1 | PROGRAMMED PROM | 28480 | 03562-60376 |
| A5U213 | 1820-0629 | 0 | 1 | IC FF TTL S J-K NEG-EDGE-TRIG | 01295 | SN23357 |
| A5U215 | 1SC3-0033 | 5 | 5 | DECIMATION FLTR | 28480 | 1SC3-0033 |
| A5U304 | 1820-3351 | 1 | 4 | IC TRANSCEIVER TTL LS BUS OCTL | 01295 | SN71932NT |
| A5U305 | 1820-3238 | 3 | 6 | IC TRANSCEIVER TTL ALS BUS OCTL | 01295 | SN71492N |
| A5U306 | 1820-3239 | 4 | 1 | IC DRVR TTL ALS BUS OCTL | 01295 | SN71491N |
| A5U307 | 1820-4019 | 0 | 2 | IC-D AM9517A-5PC | 28480 | 1820-4019 |
| A5U309 | 1820-4019 | 0 | 0 | IC-D AM9517A-5PC | 28480 | 1820-4019 |
| A5U311 | 1820-3237 | 2 | 1 | IC LCH TTL ALS TRANSPARENT NEG-EDGE-TRIG | 01295 | SN71490NT |
| A5U312 | 1820-3238 | 3 | 3 | IC TRANSCEIVER TTL ALS BUS OCTL | 01295 | SN71492N |
| A5U313 | 1820-3351 | 1 | 1 | IC TRANSCEIVER TTL LS BUS OCTL | 01295 | SN71932NT |
| A5U401 | 1SC4-0034 | 8 | 2 | FLTR CONTROLLER | 28480 | 1SC4-0034 |
| A5U404 | 1820-3351 | 1 | 1 | IC TRANSCEIVER TTL LS BUS OCTL | 01295 | SN71932NT |
| A5U404-U406 | 1820-3238 | 3 | 3 | IC TRANSCEIVER TTL ALS BUS OCTL | 01295 | SN71492N |
| A5U411-U412 | 1820-3238 | 3 | 3 | IC TRANSCEIVER TTL ALS BUS OCTL | 01295 | SN71492N |
| A5U413 | 1820-3351 | 1 | 1 | IC TRANSCEIVER TTL LS BUS OCTL | 01295 | SN71932NT |
| A5U415 | 1SC4-0034 | 8 | 8 | FLTR CONTROLLER | 28480 | 1SC4-0034 |
| A5U501 | 1SC3-0033 | 5 | 5 | DECIMATION FLTR | 28480 | 1SC3-0033 |
| A5U505 | 03562-60375 | 9 | 1 | PROGRAMMED PAL | 28480 | 03562-60375 |
| A5U506 | 1820-2657 | 8 | 1 | IC GATE TTL ALS OR QUAD 2-INP | 01295 | SN71173N |
| A5U507-U510 | 1820-3003 | 0 | 4 | IC LCH TTL ALS D-TYPE OCTL | 01295 | SN71330N |
| A5U511 | 1820-1568 | 8 | 1 | IC BFR TTL LS BUS QUAD | 01295 | SN57451N |
| A5U512 | 1820-2488 | 3 | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A5U513 | 1820-3402 | 3 | 1 | IC BFR TTL ALS NAND QUAD 2-INP | 01295 | SN71743N |
| A5U515 | 1SC3-0033 | 5 | 5 | DECIMATION FLTR | 28480 | 1SC3-0033 |
| | 0590-0526 | 6 | 24 | THREADED INSERT-NUT 4-40 .065-IN-LG SST | 46384 | KFS2-440 |
| | 0380-0411 | 3 | 24 | SPACER-RND .5-IN-LG .114-IN-ID | 34114 | 3-5162-111 |
| | 2200-0149 | 6 | 24 | SCREW-MACH 4-40 .625-IN-LG PAN-HD-POZI | 77250 | 4367 |
| | 1258-0141 | 8 | 7 | JMPR-REM .025P | 22526 | 65474-004 |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | G01016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| A6 | 03562-66506 | 0 | 1 | ASSY,DGTL FLTR | 28480 | 03562-66506 |
| A6C1 | 0180-0094 | 4 | 1 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2-DSM |
| A6C2-C3 | 0180-0197 | 8 | 2 | CAPACITOR-FXD 2.2UF+-10% 20VDC TA | 13606 | 150D225X9020A2-DYS |
| A6C100-C130 | 0160-4571 | 8 | 31 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A6C131-C132 | 0160-4788 | 9 | 8 | CAPACITOR-FXD 18PF +-5% 100VDC CER 0+-30 | 04222 | MA101A180JAA |
| A6J2 | 1251-4670 | 2 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A6P1 | 1251-7506 | 9 | 1 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A6R1 | 0683-2025 | 1 | 1 | RESISTOR 2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A6R2-R3 | 0683-6835 | 9 | 1 | RESISTOR 68K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A6RP1RP2 | 1810-0279 | 5 | 2 | NETWORK-RES 10-SIP 4.7K OHM X 9 | 91637 | CSC10A01-472G/MSP10A01-472G |
| A6TP1-TP7 | 1251-0600 | 0 | 7 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-------------------|
| A6U104 | 1820-2657 | 8 | 2 | IC GATE TTL ALS OR QUAD 2-INP | 01295 | SN71173N |
| A6U106 | 1820-2656 | 7 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A6U107 | 1820-3466 | 9 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71746N |
| A6U108 | 1820-2775 | 1 | 1 | IC GATE TTL ALS NAND TPL 3-INP | 01295 | SN71546N |
| A6U109 | 1820-2604 | 5 | 1 | IC-8-BIT/16-BIT SYSTEM TIMING CONTROLLER | 34335 | AM9513ADC |
| A6U201-U203 | 1820-2488 | 3 | 4 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A6U204 | 1820-2657 | 8 | | IC GATE TTL ALS OR QUAD 2-INP | 01295 | SN71173N |
| A6U206 | 1820-2635 | 2 | 1 | IC GATE TTL ALS AND QUAD 2-INP | 01295 | SN71172N |
| A6U207 | 1820-2758 | 0 | 1 | IC FF TTL ALS J-K BAR POS-EDGE-TRIG | 01295 | SN71174N |
| A6U208 | 1820-2951 | 5 | 1 | IC DRVR TTL ALS BUS OCTL | 01295 | SN71341N |
| A6U301 | 1820-3318 | 0 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71690N |
| A6U302 | 1820-2724 | 0 | 2 | IC LCH TTL ALS D-TYPE OCTL | 01295 | SN71340N |
| A6U303 | 1820-2772 | 8 | 1 | IC FF TTL ALS J-K NEG-EDGE-TRIG | 01295 | SN71543N |
| A6U304 | 03562-60383 | 9 | 1 | PROGRAMMED PAL | 28480 | 03562-60383 |
| A6U305 | 1820-2691 | 0 | 1 | IC FF TTL F D-TYPE POS-EDGE-TRIG | 07263 | SL82685 |
| A6U306 | 03562-60382 | 8 | 1 | PROGRAMMED PAL | 28480 | 03562-60382 |
| A6U307 | 1820-3318 | 0 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71690N |
| A6U308 | 1820-2724 | 0 | | IC LCH TTL ALS D-TYPE OCTL | 01295 | SN71340N |
| A6U309 | 03562-60396 | 4 | 1 | PROGRAMMED PAL | 28480 | 03562-60396 |
| A6U310 | 1820-1437 | 0 | 1 | IC MV TTL LS MONOSTBL DUAL | 01295 | SN57198 |
| A6U401-U402 | 1820-3349 | 7 | 2 | IC BFR TTL ALS NAND QUAD 2-INP | 01295 | SN71692N |
| A6U403 | 1820-3239 | 4 | 1 | IC DRVR TTL ALS BUS OCTL | 01295 | SN71491N |
| A6U404 | 1820-3106 | 4 | 1 | IC COMPTT TTL ALS MAGTD 8-BIT | 01295 | SN71693N |
| A6U405-U406 | 1820-3362 | 4 | 2 | IC TRANSCEIVER TTL ALS BUS OCTL | 01295 | SN71879N |
| A6U409 | 03562-60397 | 5 | 1 | PROGRAMMED PAL | 28480 | 03562-60397 |
| A6U410 | 1820-3391 | 9 | 1 | IC MUXR/DATA-SEL TTL ALS 8-TO-1-LINE | 01295 | SN71873N |
| A6U500 | 1820-2488 | 3 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A6W2 | 1258-0141 | 8 | 1 | JMPR-REM .025P | 22526 | 65474-004 |
| A6Y1 | 0410-1410 | 9 | 1 | CRYSTAL-QUARTZ 4.91520 MHZ HC-18/U-HLDR | S01163 | 0410-1410 |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | G01016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| A7 | 03562-66507 | 1 | 1 | ASSY, FPP | 28480 | 03562-66507 |
| A7C1-C50 | 0160-4571 | 8 | 50 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A7C51-C52 | 0180-0094 | 4 | 1 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2-DSM |
| A7J1 | 1251-4822 | 6 | 4 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 27264 | 22-03-2031 |
| A7J2 | 1251-6515 | 8 | 5 | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A7J3A | 1251-6515 | 8 | | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A7J3C | 1251-6515 | 8 | | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A7J4 | 1251-4822 | 6 | | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 27264 | 22-03-2031 |
| A7J5 | 1251-5202 | 8 | 1 | CONN-POST TYPE .125-PIN-SPCG 5-CONT | 22526 | 65580-105 |
| A7J6 | 1251-6515 | 8 | | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A7J7-J8 | 1251-4822 | 6 | | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 27264 | 22-03-2031 |
| A7J9 | 1251-6515 | 8 | | CONN-POST TYPE .100-PIN-SPCG 6-CONT | 22526 | 65610-106 |
| A7JP1 | 1258-0141 | 8 | 14 | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP2A | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP2B | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP3A | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP3B | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP3C | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP3D | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP4 | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP6A | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP6B | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP7 | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP8 | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP9A | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7JP9B | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A7LED1-LED2 | 1990-0652 | 8 | 1 | LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX | 28480 | 1990-0652 |
| A7P1 | 1251-7506 | 9 | 1 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A7R1-R8 | 0683-4725 | 2 | | RESISTOR 4.7K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A7R9-R10 | 0683-1025 | 9 | 3 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A7R11 | 0683-4725 | 2 | | RESISTOR 4.7K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A7R12 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A7R13 | 0683-4725 | 2 | | RESISTOR 4.7K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A7R14-R15 | 0699-0065 | 8 | 1 | RESISTOR 51.01 .25% .5W F TC=0+-50 | 19701 | 5053R |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------------------|
| A7R16-R17 | 0683-4725 | 2 | | RESISTOR 4.7K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A7TP1-TP11 | 1251-0600 | 0 | 11 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A7U103 | 1820-3657 | 0 | 1 | IC-12 BIT WIDE MICROPROGRAMMER | 34335 | AM2910ADC |
| A7U104 | 03562-60314 | 6 | 1 | PROGRAMMED PROM | 28480 | 03562-60314 |
| A7U105 | 03562-60315 | 7 | 1 | PROGRAMMED PROM | 28480 | 03562-60315 |
| A7U106 | 03562-60317 | 9 | 1 | PROGRAMMED PROM | 28480 | 03562-60317 |
| A7U110 | 03562-60316 | 8 | 1 | PROGRAMMED PROM | 28480 | 03562-60316 |
| A7U111 | 03562-60318 | 0 | 1 | PROGRAMMED PROM | 28480 | 03562-60318 |
| A7U112 | 03562-60319 | 1 | 1 | PROGRAMMED PROM | 28480 | 03562-60319 |
| A7U113 | 1820-1281 | 2 | 1 | IC DCDR TTL LS 2-TO-4-LINE DUAL | 01295 | SN53657 |
| A7U114 | 1820-2757 | 9 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A7U115 | 1820-2795 | 5 | 1 | IC DRVR TTL F LINE DRVR OCTL | 07263 | SM83462 |
| A7U201 | 1820-2613 | 6 | 1 | IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE | 01295 | SN70689N |
| A7U202 | 03562-60313 | 5 | 1 | PROGRAMMED PROM | 28480 | 03562-60313 |
| A7U204-U205 | 1820-2711 | 5 | 2 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71504N |
| A7U206-U207 | 1820-1858 | 9 | 2 | IC FF TTL LS D-TYPE OCTL | 01295 | SN58490N |
| A7U209 | 03562-60323 | 7 | 1 | PROGRAMMED PROM | 28480 | 03562-60323 |
| A7U211 | 1820-2389 | 3 | 2 | IC-LOOK-AHEAD CARRY GEN, 4 INPUT PAIRS | 34335 | AM2902APC |
| A7U212 | 03562-60320 | 4 | 1 | PROGRAMMED PAL | 28480 | 03562-60320 |
| A7U213 | 1820-1195 | 1 | 7 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN53526 |
| A7U215 | 1820-2488 | 3 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A7U301 | 1820-1298 | 1 | 1 | IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE | 01295 | SN53660 |
| A7U302 | 1820-2389 | 3 | 3 | IC-LOOK-AHEAD CARRY GEN, 4 INPUT PAIRS | 34335 | AM2902APC |
| A7U303-U308 | 1820-2377 | 9 | 6 | IC-BIT SLICE, 16 FUNCT ALU, EXPANDED | 34335 | AM2903DC |
| A7U310 | 1820-2377 | 9 | 1 | IC-BIT SLICE, 16 FUNCT ALU, EXPANDED | 34335 | AM2903DC |
| A7U312 | 1820-2690 | 9 | 2 | IC GATE TTL F OR QUAD 2-INP | 07263 | SL82683 |
| A7U313 | 03562-60321 | 5 | 1 | PROGRAMMED PAL | 28480 | 03562-60321 |
| A7U314 | 03562-60322 | 6 | 1 | PROGRAMMED PAL | 28480 | 03562-60322 |
| A7U315 | 1820-2690 | 9 | 1 | IC GATE TTL F OR QUAD 2-INP | 07263 | SL82683 |
| A7U401 | 03562-60312 | 4 | 1 | PROGRAMMED PAL | 28480 | 03562-60312 |
| A7U412-U415 | 1820-2882 | 1 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| A7U501 | 1820-2635 | 2 | 1 | IC GATE TTL ALS AND QUAD 2-INP | 01295 | SN71172N |
| A7U502 | 1820-2488 | 3 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A7U503 | 1820-3349 | 7 | 1 | IC BFR TTL ALS NAND QUAD 2-INP | 01295 | SN71692N |
| A7U504 | 1820-2951 | 5 | 1 | IC DRVR TTL ALS BUS OCTL | 01295 | SN71341N |
| A7U505-U506 | 1820-2882 | 1 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| A7U507 | 1820-2740 | 0 | 1 | IC COMPTR TTL LS MAGTD 2-INP 8-BIT | 34335 | AM25LS2521PC |
| A7U510-U515 | 1820-2882 | 1 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | G01016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| A8 | 03562-66508 | 2 | 1 | PC BD ASSY RAM/DSPL | 28480 | 03562-66508 |
| A8C1 | 0180-0094 | 4 | 1 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2-DSM |
| A8C2 | 0180-0097 | 7 | 1 | CAPACITOR-FXD 47UF+-10% 35VDC TA | 13606 | 150D476X9035S2-DYS |
| A8C101 | 0160-4571 | 8 | 67 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C103-C111 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C201-C211 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C301-C312 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C400-C401 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C404-C409 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C411 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C500-C509 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C511-C512 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8C600-C612 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A8CR1 | 1990-0486 | 6 | 1 | LED-LAMP LUM-INT=2MCD IF=25MA-MAX BVR=5V | 28480 | 1990-0486 |
| A8J1-J2 | 1251-5202 | 8 | 8 | CONN-POST TYPE .125-PIN-SPCG 5-CONT | 22526 | 65580-105 |
| A8J3-J4 | 1251-4670 | 2 | 7 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A8J5 | 1252-0169 | 8 | 1 | 3X8 CONN JUMPER POST | 22526 | 1252-0169 |
| A8J6-J9 | 1251-4670 | 2 | 2 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A8R1 | 0757-0411 | 2 | 3 | RESISTOR 332 1% .125W F TC=0+-100 | 19701 | 5033R |
| A8R2-R14 | 0757-0180 | 2 | 13 | RESISTOR 31.6 1% .125W F TC=0+-100 | 19701 | 5033R |
| A8R15-R16 | 0757-0411 | 2 | 2 | RESISTOR 332 1% .125W F TC=0+-100 | 19701 | 5033R |
| A8R17 | 0698-4123 | 5 | 1 | RESISTOR 499 1% .125W F TC=0+-100 | 19701 | 5033R |
| A8RP1-RP3 | 1810-0277 | 3 | 3 | NETWORK-RES 10-SIP 2.2K OHM X 9 | 91637 | CSC10A01-222G/MSP10A01-222G |
| A8RP4-RP5 | 1810-0280 | 8 | 2 | NETWORK-RES 10-SIP 10.0K OHM X 9 | 91637 | CSC10A01-103G/MSP10A01-103G |
| A8TP1-TP7 | 1251-0600 | 0 | 7 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A8U101 | 1820-2947 | 9 | 1 | IC DIRV TTL LS BIN | 01295 | SN71558N |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A8U103-U110 | 1818-3006 | 8 | | IC NMOS 65536 (64K) DYN RAM 200-NS 3-S | 54013 | HM4864P-3 |
| A8U111 | 1820-1450 | 7 | 3 | IC BFR TTL S NAND QUAD 2-INP | 01295 | SN85496 |
| A8U201 | 1820-2488 | 3 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A8U202 | 1820-2657 | 8 | 1 | IC GATE TTL ALS OR QUAD 2-INP | 01295 | SN71173N |
| A8U203-U210 | 1818-3006 | 8 | | IC NMOS 65536 (64K) DYN RAM 200-NS 3-S | 54013 | HM4864P-3 |
| A8U211 | 1820-1450 | 7 | | IC BFR TTL S NAND QUAD 2-INP | 01295 | SN85496 |
| A8U301 | 1820-0697 | 2 | 6 | IC DRVR TTL S NAND LINE DUAL 4-INP | 01295 | SN24665 |
| A8U302 | 1820-2701 | 3 | 2 | IC FF TTL F D-TYPE POS-EDGE-TRIG COM | 07263 | SL82694 |
| A8U303 | 03562-60384 | 0 | 1 | PROGRAMMED PROM | 28480 | 03562-60384 |
| A8U304 | 1820-2684 | 1 | 4 | IC GATE TTL F NAND QUAD 2-INP | 07263 | SL82676 |
| A8U305 | 1820-1450 | 7 | | IC BFR TTL S NAND QUAD 2-INP | 01295 | SN85496 |
| A8U306-U308 | 1820-0697 | 2 | | IC DRVR TTL S NAND LINE DUAL 4-INP | 01295 | SN24665 |
| A8U309 | 1820-2692 | 1 | 1 | IC GATE TTL F EXCL-OR QUAD 2-INP | 07263 | SL82686 |
| A8U310 | 1820-2684 | 1 | 1 | IC GATE TTL F NAND QUAD 2-INP | 07263 | SL82676 |
| A8U311-U312 | 1813-0424 | 8 | 3 | ACTIVE DELAY LINE 14 | E01049 | SXTTLDM-104 |
| A8U400-U401 | 1820-1435 | 8 | 7 | IC CNTR TTL LS BIN UP/DOWN SYNCHRO | 01295 | SN57196N |
| A8U404 | 1820-1278 | 7 | 1 | IC CNTR TTL LS BIN UP/DOWN SYNCHRO | 01295 | SN53646 |
| A8U405 | 1820-2488 | 3 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A8U406 | 1820-0697 | 2 | 3 | IC DRVR TTL S NAND LINE DUAL 4-INP | 01295 | SN24665 |
| A8U407-U408 | 1820-2656 | 7 | 2 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A8U409 | 1820-0697 | 2 | | IC DRVR TTL S NAND LINE DUAL 4-INP | 01295 | SN24665 |
| A8U411 | 1813-0424 | 8 | | ACTIVE DELAY LINE 14 | E01049 | SXTTLDM-104 |
| A8U500 | 1820-3349 | 7 | 1 | IC BFR TTL ALS NAND QUAD 2-INP | 01295 | SN71692N |
| A8U501 | 1820-1435 | 8 | | IC CNTR TTL LS BIN UP/DOWN SYNCHRO | 01295 | SN57196N |
| A8U502-U505 | 1820-3362 | 4 | 8 | IC TRANSCIEVER TTL ALS BUS OCTL | 01295 | SN71879N |
| A8U506 | 03562-60385 | 1 | 1 | PROGRAMMED PAL | 28480 | 03562-60385 |
| A8U507 | 1820-2701 | 3 | 3 | IC FF TTL F D-TYPE POS-EDGE-TRIG COM | 07263 | SL82694 |
| A8U508 | 1820-3362 | 4 | 4 | IC TRANSCIEVER TTL ALS BUS OCTL | 01295 | SN71879N |
| A8U509 | 1820-2795 | 5 | 1 | IC DRVR TTL F LINE DRVR OCTL | 07263 | SN83462 |
| A8U511-U512 | 1820-2270 | 1 | 2 | IC CNTR TTL LS BIN UP/DOWN SYNCHRO | 34335 | AM25LS2569DC |
| A8U600-U603 | 1820-1435 | 8 | | IC CNTR TTL LS BIN UP/DOWN SYNCHRO | 01295 | SN57196N |
| A8U604-U605 | 1820-3362 | 4 | | IC TRANSCIEVER TTL ALS BUS OCTL | 01295 | SN71879N |
| A8U606-U607 | 1820-2684 | 1 | 1 | IC GATE TTL F NAND QUAD 2-INP | 07263 | SL82676 |
| A8U608 | 1820-3362 | 4 | | IC TRANSCIEVER TTL ALS BUS OCTL | 01295 | SN71879N |
| A8U609-U610 | 1820-3654 | 7 | 4 | IC-BIDIRECTIONAL BUS TRANSCIEVER(8-WIDE) | 34335 | AM2946PC |
| A8U611-U612 | 1820-2763 | 7 | 2 | IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD | 07263 | SL83215 |
| | 1258-0141 | 8 | 7 | JMPR-REM .025P | 22526 | 65474-004 |
| | 1480-0116 | 8 | 8 | PIN-GRV .062-IN-DIA .25-IN-LG STL | G01016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| | 1258-0218 | 0 | 1 | JUMPER, 16 CKT, CONN | 22526 | 76266-108 |
| | 1251-7506 | 9 | 1 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A9 | 03562-66509 | 3 | 1 | PC BD ASSY FFT | 28480 | 03562-66509 |
| A9C101-C102 | 0160-4791 | 4 | 2 | CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG100J100A |
| A9C103 | 0160-4571 | 8 | 42 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C105-C107 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C109 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C117 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C206 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C208-C218 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C301 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C303 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C305 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C307 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C310-C311 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C313-C315 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C317 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C403 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C405-C406 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C408-C409 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C411-C412 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C501 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C502 | 0180-0094 | 4 | 1 | CAPACITOR-FXD 100UF+75-10% 25VDC AL | 13606 | 30D107G025DD2--DSM |
| A9C503 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C505-C506 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C507 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C515-C516 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A9C518 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A9CR101-CR102 | 1990-0652 | 8 | 1 | LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX | 28480 | 1990-0652 |
| A9J1-J2 | 1251-4670 | 2 | 2 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A9J3-J4 | 1252-0169 | 8 | 2 | 3X8 CONN JUMPER POST | 22526 | 1252-0169 |
| A9J5 | 1251-5202 | 8 | 1 | CONN-POST TYPE .125-PIN-SPCG 5-CONT | 22526 | 65580-105 |
| A9JP1-JP2 | 1258-0141 | 8 | 2 | JMPR-REM .025P | 22526 | 65474-004 |
| A9JP3-JP4 | 1258-0218 | 0 | 2 | JUMPER, 16 CKT, CONN | 22526 | 76266-108 |
| A9P1 | 1251-7506 | 9 | 1 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 1-532956-8 |
| A9R206 | 0683-1025 | 9 | 10 | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9R209 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9R211 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9R213 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9R216 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9R303 | 8150-3375 | 5 | 1 | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A9R305 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9R414 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9R501-R502 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9R511 | 0683-1025 | 9 | | RESISTOR 1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A9TP1-TP3 | 1251-0600 | 0 | | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A9U103 | 1820-3974 | 4 | 1 | IC-M TMS320 MMOS 16BMPU P40 | 01295 | TMS32010NL |
| A9U105-U108 | 1820-1987 | 5 | | IC SHF-RGTR TTL LS COM CLEAR STOR 8-BIT | 34335 | AM74LS299N |
| A9U109 | 1820-2634 | 1 | 2 | IC INV TTL ALS HEX | 01295 | SN71332N |
| A9U111-U112 | 1820-1440 | 5 | 2 | IC LCH TTL LS QUAD | 01295 | SN57201 |
| A9U115 | 03562-60311 | 3 | 1 | PROGRAMMED PAL | 28480 | 03562-60311 |
| A9U117 | 03562-60310 | 2 | 1 | PROGRAMMED PROM | 28480 | 03562-60310 |
| A9U202 | 1820-1729 | 3 | 1 | IC LCH TTL LS COM CLEAR 8-BIT | 07263 | 74LS259PC |
| A9U206 | 1820-1217 | 4 | 1 | IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE | 01295 | SN53523 |
| A9U207 | 03562-60307 | 7 | 1 | PROGRAMMED PAL | 28480 | 03562-60307 |
| A9U208 | 1820-1282 | 3 | 1 | IC FF TTL LS J-K BAR POS-EDGE-TRIG | 01295 | SN53656 |
| A9U209-U210 | 1820-3144 | 0 | 2 | IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG | 01295 | SN71560N |
| A9U211 | 1820-3349 | 7 | 1 | IC BFR TTL ALS NAND QUAD 2-INP | 01295 | SN71692N |
| A9U212 | 1820-2656 | 7 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A9U213 | 1820-2488 | 3 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A9U214 | 1820-2657 | 8 | 1 | IC GATE TTL ALS OR QUAD 2-INP | 01295 | SN71173N |
| A9U215 | 1820-2634 | 1 | 1 | IC INV TTL ALS HEX | 01295 | SN71332N |
| A9U216-U217 | 1820-2861 | 6 | 2 | IC DCDR TTL F 3-TO-8-LINE | 07263 | 74F138PC |
| A9U218 | 1820-2635 | 2 | 2 | IC GATE TTL ALS AND QUAD 2-INP | 01295 | SN71172N |
| A9U301 | 03562-60309 | 9 | 1 | PROGRAMMED PROM | 28480 | 03562-60309 |
| A9U303 | 03562-60308 | 8 | 1 | PROGRAMMED PROM | 28480 | 03562-60308 |
| A9U305 | 03562-60387 | 3 | 1 | PROGRAMMED PROM | 28480 | 03562-60387 |
| A9U307 | 1820-2635 | 2 | 1 | IC GATE TTL ALS AND QUAD 2-INP | 01295 | SN71172N |
| A9U309-U311 | 1820-1438 | 1 | | IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD | 01295 | SN57199N |
| A9U312 | 1820-1447 | 2 | 1 | IC TTL LS 16-BIT STAT RAM 45-NS 3-S | 01295 | SN57208 |
| A9U313 | 03562-60306 | 6 | 2 | PROGRAMMED PAL | 28480 | 03562-60306 |
| A9U314 | 03562-60306 | 6 | 1 | PROGRAMMED PAL | 28480 | 03562-60306 |
| A9U315 | 03562-60304 | 4 | 1 | PROGRAMMED PROM | 28480 | 03562-60304 |
| A9U317 | 03562-60303 | 3 | 1 | PROGRAMMED PROM | 28480 | 03562-60303 |
| A9U403 | 1820-3238 | 3 | 2 | IC TRANSCIEVER TTL ALS BUS OCTL | 01295 | SN71492N |
| A9U405-U406 | 1820-2757 | 9 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A9U408 | 1820-1211 | 8 | 1 | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN53518N |
| A9U409-U411 | 1820-1194 | 6 | 3 | IC CNTR TTL LS BIN UP/DOWN SYNCHRO | 01295 | SN53527 |
| A9U412-U413 | 1820-2724 | 0 | 2 | IC LCH TTL ALS D-TYPE OCTL | 01295 | SN71340N |
| A9U501 | 1820-2488 | 3 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A9U502 | 03562-60305 | 5 | 1 | PROGRAMMED PROM | 28480 | 03562-60305 |
| A9U503 | 1820-3238 | 3 | 1 | IC TRANSCIEVER TTL ALS BUS OCTL | 01295 | SN71492N |
| A9U505 | 1820-1640 | 7 | 1 | IC DRVR TTL LS BUS HEX 1-INP | 01295 | SN57699N |
| A9U506-U509 | 1820-2882 | 1 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| A9U510 | 1820-3106 | 4 | 1 | IC COMPTN TTL ALS MAGTD 8-BIT | 01295 | SN71693N |
| A9U511-U516 | 1820-2882 | 1 | | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| A9U517-U518 | 1820-2711 | 5 | 2 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71504N |
| A9Y1 | 0410-1501 | 9 | 1 | CRYSTAL-QUARTZ 20 MHZ HC-18/U-HLDR | 33096 | CCAT 101842 |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | G01016 | GP24-063 X 250-17 |
| | 4040-0753 | 0 | 2 | EXTR-PC BD GRN POLYC .062-IN-BD-THKNS | V01022 | 4040-0753 |
| A12 | 03562-66512 | 8 | 1 | PC BD ASSY MOTHERB'D | 28480 | 03562-66512 |
| A12C1 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A12C2 | 0180-2249 | 5 | 1 | CAPACITOR-FXD 47UF+-10% 20VDC TA | 13606 | 150D476X9020R2-DYS |
| A12J1-J10 | 1251-8097 | 5 | 10 | CONN-POST TYPE .100-PIN-SPCG 120-CONT | 00779 | 102692-9 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------------------|
| A12J15 | 1252-1187 | 2 | 1 | CONN-POST-TP-HDR 40 PIN .155" | 28480 | 1252-1187 |
| A12J16 | 1251-6173 | 4 | 1 | CONN-POST TYPE .156-PIN-SPCG 2-CONT | 27264 | 09-72-1021 |
| A12J17 | 1251-7627 | 5 | 4 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 00779 | 1-102567-2 |
| A12J30-J32 | 1251-7627 | 5 | 5 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 00779 | 1-102567-2 |
| A12J33 | 1251-7754 | 9 | 2 | CONN-POST TYPE .100-PIN-SPCG 30-CONT | 00779 | 1-102567-3 |
| A12J34 | 1251-7627 | 5 | 9 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 00779 | 1-102567-2 |
| A12J35 | 1251-7754 | 9 | 9 | CONN-POST TYPE .100-PIN-SPCG 30-CONT | 00779 | 1-102567-3 |
| A12MP686 | 03562-48305 | 9 | 2 | KEY,C.BD,FOOLPRF | 28480 | 03562-48305 |
| A12R1 | 0757-0795 | 5 | 1 | RESISTOR 75 1% .5W F TC=0+-100 | 19701 | 5033R |
| A12R2 | 0757-0178 | 8 | 1 | RESISTOR 100 1% .25W F TC=0+-100 | 19701 | 5043R |
| A12R4 | 0757-1040 | 5 | 1 | RESISTOR 50 1% .25W F TC=0+-100 | 19701 | 5043R |
| A12RP1-RP10 | 1810-0372 | 9 | 10 | NETWORK-RES 10-SIP 220.0 OHM X 9 | 11236 | 750-101-R220 |
| A12W13 | 03562-61613 | 0 | 1 | CBL PWR/MBD | 28480 | 03562-61613 |
| | 2190-0007 | 2 | 2 | WASHER-LK INTL T NO. 6 .141-IN-ID | T12345 | 1906-00-00-2580 |
| | 0380-0005 | 1 | 4 | SPCR-RD .31LG.18ID.25D BRNSI | LO1005 | 0380-0005 |
| | 0515-0211 | 8 | 4 | SCREW-MACH M3 X 0.5 6MM-LG PAN-HD | 16941 | 0515-0211 |
| | 0515-0900 | 2 | 4 | SCREW-MACH M3.5 X 0.6 14MM-LG PAN-HD | M01088 | 0515-0900 |
| | 0535-0007 | 2 | 4 | NUT-HEX DBL-CHAM M3.5 X 0.6 2.8MM-THK | H01043 | 0535-0007 |
| | 1251-7627 | 5 | 1 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 00779 | 1-102567-2 |
| A15 | 03562-66515 | 1 | 1 | PC BD ASSY KYBD | 28480 | 03562-66515 |
| A15C1 | 0180-2249 | 5 | 1 | CAPACITOR-FXD 47UF+-10% 20VDC TA | 13606 | 150D476X9020R2-DYS |
| A15C2-C3 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C4-C5 | 0160-4788 | 9 | 2 | CAPACITOR-FXD 18PF +-5% 100VDC CER 0+-30 | 04222 | MA101A180JAA |
| A15C105-C106 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C108 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C205-C206 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C208 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C210 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C300-C308 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C402 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C404 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15C406 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A15CR1-CR3 | 1990-0487 | 7 | 1 | LED-LAMP LUM-INT=2MCD BVR=5V | 28480 | 1990-0487 |
| A15CR4 | 1990-0485 | 5 | 4 | LED-LAMP LUM-INT=2MCD IF=30MA-MAX BVR=5V | 28480 | 1990-0485 |
| A15CR5-CR6 | 1990-0487 | 7 | 1 | LED-LAMP LUM-INT=2MCD BVR=5V | 28480 | 1990-0487 |
| A15CR7 | 1990-0486 | 6 | 3 | LED-LAMP LUM-INT=2MCD IF=25MA-MAX BVR=5V | 28480 | 1990-0486 |
| A15CR8-CR11 | 1990-0487 | 7 | 1 | LED-LAMP LUM-INT=2MCD BVR=5V | 28480 | 1990-0487 |
| A15CR12 | 1990-0485 | 5 | 1 | LED-LAMP LUM-INT=2MCD IF=30MA-MAX BVR=5V | 28480 | 1990-0485 |
| A15CR13-CR15 | 1990-0487 | 7 | 1 | LED-LAMP LUM-INT=2MCD BVR=5V | 28480 | 1990-0487 |
| A15CR16 | 1990-0486 | 6 | 1 | LED-LAMP LUM-INT=2MCD IF=25MA-MAX BVR=5V | 28480 | 1990-0486 |
| A15CR17 | 1990-0485 | 5 | 1 | LED-LAMP LUM-INT=2MCD IF=30MA-MAX BVR=5V | 28480 | 1990-0485 |
| A15CR18 | 1990-0486 | 6 | 1 | LED-LAMP LUM-INT=2MCD IF=25MA-MAX BVR=5V | 28480 | 1990-0486 |
| A15CR19 | 1990-0485 | 5 | 1 | LED-LAMP LUM-INT=2MCD IF=30MA-MAX BVR=5V | 28480 | 1990-0485 |
| A15CR20 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A15J1 | 1251-5202 | 8 | 1 | CONN-POST TYPE .125-PIN-SPCG 5-CONT | 22526 | 65580-105 |
| A15J2 | 1251-4670 | 2 | 5 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A15J3 | 1251-5041 | 3 | 2 | CONN-POST TYPE .100-PIN-SPCG 5-CONT | 22526 | 65500-105 |
| A15J4 | 1252-0169 | 8 | 1 | 3X8 CONN JUMPER POST | 22526 | 1252-0169 |
| A15J5 | 1251-4670 | 2 | 2 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A15J6 | 1251-5041 | 3 | 3 | CONN-POST TYPE .100-PIN-SPCG 5-CONT | 22526 | 65500-105 |
| A15J7-J9 | 1251-4670 | 2 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A15J10 | 1251-3782 | 5 | 1 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 76381 | 3432-1002 |
| A15Q1 | 1853-0036 | 2 | 1 | TRANSISTOR PNP SI PD=310MHZ FT=250MHZ | 04713 | SPS-3612 |
| A15R1 | 0683-2215 | 1 | 1 | RESISTOR 220 5% .25W CF TC=0-400 | 77902 | R-25J |
| A15R2 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A15R3 | 0757-0273 | 4 | 1 | RESISTOR 3.01K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A15R8 | 0757-0482 | 7 | 1 | RESISTOR 511K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A15RP1 | 1810-0280 | 8 | 3 | NETWORK-RES 10-SIP 10.0K OHM X 9 | 91637 | CSC10A01-103G/MSP10A01-103G |
| A15RP2 | 1810-0277 | 3 | 5 | NETWORK-RES 10-SIP 2.2K OHM X 9 | 91637 | CSC10A01-222G/MSP10A01-222G |
| A15RP3 | 1810-0280 | 8 | 3 | NETWORK-RES 10-SIP 10.0K OHM X 9 | 91637 | CSC10A01-103G/MSP10A01-103G |
| A15RP4-RP7 | 1810-0277 | 3 | 1 | NETWORK-RES 10-SIP 2.2K OHM X 9 | 91637 | CSC10A01-222G/MSP10A01-222G |
| A15RP8-RP9 | 1810-0372 | 9 | 2 | NETWORK-RES 10-SIP 220.0 OHM X 9 | 11236 | 750-101-R220 |
| A15RP10 | 1810-0280 | 8 | 1 | NETWORK-RES 10-SIP 10.0K OHM X 9 | 91637 | CSC10A01-103G/MSP10A01-103G |
| A15SPK1 | 0960-0483 | 9 | 1 | ALARM-AUDIBLE | P01152 | 0960-0483 |
| A15SW1-SW70 | 5060-9436 | 7 | 70 | PB-SWITCH | 28480 | 5060-9436 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|--------|-----|--|----------|--------------------|
| A15TP1-TP6 | 1251-0600 | 0 | 6 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A15U105 | 1820-2488 | 3 | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A15U106 | 1820-3665 | 0 | 1 | IC-D 74HCT245 CMOS TRNCVR P20 | 27014 | MM74HCT245N |
| A15U108 | 1820-2724 | 0 | 1 | IC LCH TTL ALS D-TYPE OCTL | 01295 | SN71340N |
| A15U205 | 1820-2488 | 3 | 3 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A15U206 | 1820-2762 | 6 | 1 | IC-8-BIT MICROPROCESSOR | 04713 | MC146805E2P |
| A15U208 | 03562-60386 | 2 | 1 | PROGRAMMED PROM | 28480 | 03562-60386 |
| A15U210 | 1820-1416 | 5 | 1 | IC SCHMITT-TRIG TTL LS INV HEX 1-INP | 01295 | SN57177 |
| A15U300 | 1820-2951 | 5 | 2 | IC DRVR TTL ALS BUS OCTL | 01295 | SN71341N |
| A15U301 | 1820-3668 | 3 | 1 | IC-D 74ALS642 TRNCVR P20 | 01295 | SN74ALS642AN |
| A15U302 | 1820-2882 | 1 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| A15U303 | 1820-2951 | 5 | 1 | IC DRVR TTL ALS BUS OCTL | 01295 | SN71341N |
| A15U304-U305 | 1820-2757 | 9 | 2 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG OCTL | 01295 | SN71342N |
| A15U306 | 1820-3176 | 8 | 1 | IC MUXR/DATA-SEL CMOS/74HC 8-TO-1-LINE | 27014 | MM74HC151N |
| A15U307 | 1820-3650 | 3 | 1 | IC-D 74LS445 TTL LS DECDRV P16 | 01295 | SN74LS445N |
| A15U308 | 1820-3100 | 7 | 1 | IC DCDR TTL ALS BIN 3-TO-8-LINE 3-INP | 01295 | SN71418N |
| A15U402 | 1820-2656 | 8 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A15U404 | 1820-3270 | 3 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71534N |
| A15U406 | 1820-2488 | 3 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A15W17 | 03562-61617 | 4 | 1 | CABLE ASSY DISP.ADJ. | 28480 | 03562-61617 |
| A15Y1 | 0410-1388 | 0 | 1 | CRYSTAL-QUARTZ 4.0000 MHZ HC-18/U-HLDR | N01090 | NDK-040 |
| | 05328-40003 | 8 | 19 | STAND-L.E.D | 28480 | 05328-40003 |
| | 1258-0141 | 8 | 5 | JMPR-REM .025P | 22526 | 65474-004 |
| | 1258-0218 | 0 | 1 | JUMPER,16 CKT,CONN | 22526 | 76266-108 |
| A17 | 03562-66517 | 3 | 1 | DISPLAY ASSY | 28480 | 03562-66517 |
| A17C1-C3 | 0160-4571 | 8 | 6 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A17C4 | 0180-1794 | 3 | 1 | CAPACITOR-FXD 22UF+-10% 35VDC TA | 13606 | 150D226X9035R2-DYS |
| A17C10-C12 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A17CR1-CR6 | 1901-0704 | 4 | 6 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A17CR7 | 1902-0940 | 2 | 1 | DIODE-ZNR 1N5339B 5.6V 5% PD=5W IR=1UA | 04713 | SZP40149 |
| A17J10-J12 | 1251-4836 | 2 | 2 | CONN-POST TYPE 2.5-PIN-SPCG 2-CONT | 27264 | 22-12-1022 |
| A17P17 | 1251-7629 | 7 | 1 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 00779 | 532955-7 |
| A17R1-R3 | 0837-0298 | 3 | 1 | PTC THERMISTER | 28480 | 0837-0298 |
| A17R4 | 0757-0280 | 3 | 2 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A17R5 | 0757-0401 | 0 | 3 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A17R7 | 0757-0401 | 0 | 0 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A17R9 | 0757-0280 | 3 | 3 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A17R10 | 0757-0401 | 0 | 0 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A17TP1-TP2 | 1251-0600 | 0 | 2 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A17U1-U2 | 1820-2882 | 1 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71333N |
| A17U3 | 1820-3145 | 1 | 1 | IC DRVR TTL ALS BUS OCTL | 01295 | SN71649N |
| A17W1 | 1251-4670 | 2 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A17W14 | 03562-61614 | 1 | 1 | CBLE ASSY DISP I/O | 28480 | 03562-61614 |
| A17W190-W192 | 03562-61619 | 6 | 1 | CABLE-DISPLAY XYZ | 28480 | 03562-61619 |
| | 1258-0141 | 8 | 1 | JMPR-REM .025P | 22526 | 65474-004 |
| A18 | 03562-66518 | 4 | 1 | PC BD-PWR SPLY | 28480 | 03562-66518 |
| A18C2 | 0180-0291 | 3 | 1 | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A18C4-C17 | 0160-3847 | 9 | 1 | CAPACITOR-FXD .01UF +100-0% 50VDC CER | 04222 | SA105C103KAA |
| A18C18-C19 | 0160-4571 | 8 | 26 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C20 | 0180-0197 | 8 | 1 | CAPACITOR-FXD 2.2UF+-10% 20VDC TA | 13606 | 150D225X9020A2-DYS |
| A18C100 | 0180-3115 | 6 | 1 | CAPACITOR-FXD 330UF+50-10% 63VDC AL | U01027 | SM63T330 |
| A18C101-C102 | 0160-4571 | 8 | 14 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C103 | 0180-2825 | 3 | 1 | CAPACITOR-FXD 22UF+50-10% 50VDC AL | 13606 | 510D057 |
| A18C104 | 0160-4822 | 2 | 1 | CAPACITOR-FXD 1000PF +-5% 100VDC CER | 27167 | CAC03COG102J100A |
| A18C105 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C106 | 0180-2825 | 3 | 1 | CAPACITOR-FXD 22UF+50-10% 50VDC AL | 13606 | 510D057 |
| A18C107 | 0180-2351 | 0 | 1 | CAPACITOR-FXD 2000UF+75-10% 50VDC AL | 13606 | 39D243-DSB |
| A18C108 | 0180-0374 | 3 | 1 | CAPACITOR-FXD 10UF+-10% 20VDC TA | 13606 | 150D106X9020B2-DYS |
| A18C109-C110 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C200 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C201-C202 | 0160-0302 | 5 | 1 | CAPACITOR-FXD .018UF +-10% 200VDC POLYE | 13606 | 192P18392 |
| A18C300 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |

△ See backdating.

See introduction to this section for ordering information
*Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A18C301 | 0160-4809 | 5 | 1 | CAPACITOR-FXD 390PF +-5% 100VDC CER | 27167 | CAC02COG391J100A |
| A18C302 | 0160-0159 | 0 | 1 | CAPACITOR-FXD 6800PF +-10% 200VDC POLYE | 13606 | 192P68292 |
| A18C303 | 0160-4835 | 7 | 1 | CAPACITOR-FXD .1UF +-10% 50VDC CER | 27167 | CAC04X7R104K050A |
| A18C304 | 0160-0128 | 3 | 1 | CAPACITOR-FXD 2.2UF +-20% 50VDC CER | 13606 | 3C37Z5U225M050A |
| A18C305-C306 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +-80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C307 | 0180-3525 | 2 | 1 | C-F 3300UF --% 12V ALUMEr | 13606 | 674D338H012HJ5A |
| A18C308 | 0180-0374 | 3 | 1 | CAPACITOR-FXD 10UF+-10% 20VDC TA | 13606 | 150D106X9020B2-DYS |
| A18C310 | 0160-2055 | 9 | 1 | CAPACITOR-FXD .01UF +80-20% 100VDC CER | T01067 | 805-504 Y5V 103Z |
| A18C400 | 0140-0200 | 0 | 2 | CAPACITOR-FXD 390PF +-5% 300VDC MICA | 09023 | 0140-0200 |
| A18C401 | 0180-2825 | 3 | 1 | CAPACITOR-FXD 22UF+50-10% 50VDC AL | 13606 | 510D057 |
| A18C402 | 0160-6087 | 5 | 1 | C-F 2UF 10% 400V POLYPa | 84411 | TRW-35 2UF 400V |
| A18C403-C404 | 0180-3500 | 3 | 2 | C-F 1400UF --% 250V ALSTMr | 13606 | 623D214 |
| A18C405 | 0160-4281 | 7 | 1 | CAPACITOR-FXD 2200PF +-20% 250VAC(RMS) | W01110 | W01110 |
| A18C406 | 0160-6087 | 5 | 1 | C-F 2UF 10% 400V POLYPa | 84411 | TRW-35 2UF 400V |
| A18C407 | 0140-0200 | 0 | 1 | CAPACITOR-FXD 390PF +-5% 300VDC MICA | 09023 | 0140-0200 |
| A18C408 | 0150-0012 | 3 | 1 | CAPACITOR-FXD .01UF +-20% 1KVDC CER | T01067 | 818-584 Z5U 103M |
| A18C500-C502 | 0180-2825 | 3 | 1 | CAPACITOR-FXD 22UF+50-10% 50VDC AL | 13606 | 510D057 |
| A18C503 | 0180-0550 | 7 | 4 | CAPACITOR-FXD 330UF+100-10% 25VDC AL | 55680 | R1-A25U-330 |
| A18C504-C505 | 0180-3524 | 1 | 2 | C-F 227UF --% 100V ALUMEr | 13606 | 674D227H100HJ5A |
| A18C506-C508 | 0180-3499 | 9 | 1 | C-F 470UF --% 50V ALUMEr | 13606 | 674D477H050JE5A |
| A18C509 | 0180-0550 | 7 | 1 | CAPACITOR-FXD 330UF+100-10% 25VDC AL | 55680 | R1-A25U-330 |
| A18C510-C511 | 0180-2825 | 3 | 1 | CAPACITOR-FXD 22UF+50-10% 50VDC AL | 13606 | 510D057 |
| A18C512-C516 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C517-C518 | 0180-0550 | 7 | 1 | CAPACITOR-FXD 330UF+100-10% 25VDC AL | 55680 | R1-A25U-330 |
| A18C519-C523 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C524-C525 | 0180-2825 | 3 | 1 | CAPACITOR-FXD 22UF+50-10% 50VDC AL | 13606 | 510D057 |
| A18C526 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C527-C530 | 0180-2825 | 3 | 1 | CAPACITOR-FXD 22UF+50-10% 50VDC AL | 13606 | 510D057 |
| A18C600 | 0160-3455 | 5 | 1 | CAPACITOR-FXD 470UF +-10% 1KVDC CER | T01067 | 838-546 X5E 471K |
| A18C700-C701 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18C800-C801 | 0160-3847 | 9 | 1 | CAPACITOR-FXD .01UF +100-0% 50VDC CER | 04222 | SA105C103KAA |
| A18C802-C803 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A18CR1-CR3 | 1901-0050 | 3 | 18 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A18CR4-CR6 | 1990-0652 | 3 | 3 | LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX | 28480 | 1990-0652 |
| A18CR7 | 1826-1138 | 0 | 1 | IC MISC 3-TO-46 PKG | 27014 | LM135AH |
| A18CR100-CR103 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A18CR200 | 0837-0299 | 4 | 1 | VOLTAGE SUPPRESSOR VR= 5.0V, BV= 5.3V | 24444 | GMP-5B |
| A18CR201 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A18CR300-CR302 | 1901-0960 | 4 | 2 | DIODE-PWR RECT 50V 75A DO-5 | 18546 | VSK71 |
| A18CR400 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A18CR401-CR402 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR403 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A18CR500 | 0837-0303 | 1 | 1 | VOLTAGE SUPPRESSOR VR=33.3V, BV=37.1 TO | 24444 | P6KE39A |
| A18CR501-CR502 | 1901-0704 | 4 | 24 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR503 | 0837-0303 | 1 | 1 | VOLTAGE SUPPRESSOR VR=33.3V, BV=37.1 TO | 24444 | P6KE39A |
| A18CR401-CR402 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR403 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A18CR500 | 0837-0303 | 1 | 1 | VOLTAGE SUPPRESSOR VR=33.3V, BV=37.1 TO | 24444 | P6KE39A |
| A18CR501-CR502 | 1901-0704 | 4 | 20 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR503 | 0837-0303 | 1 | 1 | VOLTAGE SUPPRESSOR VR=33.3V, BV=37.1 TO | 24444 | P6KE39A |
| A18CR504-CR507 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR508 | 0837-0300 | 8 | 1 | VOLTAGE SUPPRESSOR VR=8.55V, BV= 9.5 TO | 24444 | P6KE10A |
| A18CR509-CR510 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR511 | 0837-0300 | 8 | 1 | VOLTAGE SUPPRESSOR VR=8.55V, BV= 9.5 TO | 24444 | P6KE10A |
| A18CR512-CR513 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR514 | 0837-0302 | 0 | 1 | VOLTAGE SUPPRESSOR VR=16.2V, BV=18.0 TO | 24444 | P6KE20 |
| A18CR515-CR516 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR517 | 0837-0302 | 0 | 1 | VOLTAGE SUPPRESSOR VR=16.2V, BV=18.0 TO | 24444 | P6KE20 |
| A18CR518-CR519 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR520 | 0837-0302 | 0 | 1 | VOLTAGE SUPPRESSOR VR=16.2V, BV=18.0 TO | 24444 | P6KE20 |
| A18CR521-CR522 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR523 | 0837-0302 | 0 | 1 | VOLTAGE SUPPRESSOR VR=16.2V, BV=18.0 TO | 24444 | P6KE20 |
| A18CR524-CR525 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR526 | 0837-0301 | 9 | 1 | VOLTAGE SUPPRESSOR VR=12.8V, BV=14.3 TO | 24444 | P6KE15A |
| A18CR527 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR528 | 0837-0301 | 9 | 1 | VOLTAGE SUPPRESSOR VR=12.8V, BV=14.3 TO | 24444 | P6KE15A |
| A18CR529-CR533 | 1901-0704 | 4 | 1 | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR600-CR603 | 1901-1106 | 2 | 1 | DIODE-PWR RECT 400V 1A 50NS | 9N171 | UES-1106 |

See backdating.

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-------------------|
| A18CR700-CR707 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A18J3 | 1251-6310 | 1 | 1 | CONN-UTIL METMAT 6-CKT 6-CONT | 00779 | 207583-5 |
| A18CR528 | 0837-0301 | 9 | | VOLTAGE SUPPRESSOR VR=12.8V, BV=14.3 TO | 24444 | P6KE15A |
| A18CR529-CR533 | 1901-0704 | 4 | | DIODE-GEN PRP 1N4002 100V 1A DO-41 | 03580 | 1N4002 |
| A18CR600-CR603 | 1901-1106 | 2 | 1 | DIODE-PWR RECT 400V 1A 50NS | 9N171 | UES-1106 |
| A18CR700 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A18J10-J18 | 1251-4822 | 6 | | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 27264 | 22-03-2031 |
| A18J100 | 1251-4822 | 6 | | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 27264 | 22-03-2031 |
| A18J103 | 03562-61611 | 8 | 1 | CBL ASSY PWR/DISP | 28480 | 03562-61611 |
| A18J201 | 03562-61622 | 1 | 1 | CABLE ASSY +5V | 28480 | 03562-61612 |
| A18J202 | 03562-61623 | 2 | 1 | CABLE-GROUND | 28480 | 03562-61623 |
| A18J402-J407 | 1251-1636 | 4 | | CONNECTOR-SGL CONT SKT .04-IN-BSC-SZ RND | 71279 | 450-3388-01-03-00 |
| A18L100-L101 | 9140-0748 | 0 | 1 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A18L300 | 9140-0748 | 0 | 0 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A18L301 | 03562-60302 | 2 | 1 | IND 44UH 30A | 28480 | 03562-60302 |
| A18L400 | 9140-0748 | 0 | 0 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A18L500 | 9140-0893 | 6 | 2 | INDUCTOR 2MH | 09161 | PE 50502 |
| A18L503 | 9140-0893 | 6 | | INDUCTOR 2MH | 09161 | PE 50502 |
| A18MP4 | 1205-0586 | 4 | 1 | HEATSINK TO 220 | 98978 | 7-370-BA |
| A18MP5 | 1205-0587 | 5 | 1 | HEATSINK TWIN D05 | 13103 | 1676B-2XDO-5 |
| A18MP6-MP7 | 1205-0495 | 4 | 2 | HEAT SINK SGL TO-3-CS | 13103 | 16301B-4-SM4 |
| A18MP665 | 03562-01101 | 5 | 1 | HEATSINK POWER SUPPLY | 28480 | 03562-01101 |
| A18MP666 | 03562-01205 | 0 | 1 | BRKT-PWR SUPPLY | 28480 | 03562-01205 |
| A18Q2-Q4 | 1854-0215 | 1 | 6 | TRANSISTOR NPN SI PD=350MW FT=300MHZ | 04713 | SPS 3611 |
| A18Q100-Q101 | 1854-0215 | 1 | 2 | TRANSISTOR NPN SI PD=350MW FT=300MHZ | 04713 | SPS 3611 |
| A18Q102 | 1853-0036 | 2 | 7 | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 04713 | SPS-3612 |
| A18Q200-Q202 | 1853-0036 | 2 | | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 04713 | SPS-3612 |
| A18Q203 | 1854-0215 | 1 | | TRANSISTOR NPN SI PD=350MW FT=300MHZ | 04713 | SPS 3611 |
| A18Q204 | 1853-0036 | 2 | | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 04713 | SPS-3612 |
| A18Q300-Q301 | 1853-0036 | 2 | | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 04713 | SPS-3612 |
| A18Q400-Q401 | 1855-0473 | 5 | 2 | TRANSISTOR MOSFET N-CHAN TO-3 | I01060 | IR 94-0116 |
| A18R1 | 2100-3211 | 7 | 1 | RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN | 73138 | 72PR1K-105B |
| A18R2-R3 | 0757-0280 | 3 | 14 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R4 | 0757-0473 | 6 | 1 | RESISTOR 221K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R5 | 0757-0428 | 1 | 1 | RESISTOR 1.62K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R6 | 0757-0443 | 0 | 1 | RESISTOR 11K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R7 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R8 | 0757-0420 | 3 | 2 | RESISTOR 750 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R9 | 0757-0465 | 6 | 7 | RESISTOR 100K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R10 | 0757-0442 | 9 | 23 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R11 | 0757-0449 | 6 | 3 | RESISTOR 20K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R12 | 0698-3558 | 8 | 1 | RESISTOR 4.02K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R13 | 0757-0465 | 6 | | RESISTOR 100K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R14 | 0698-3484 | 9 | 1 | RESISTOR 6.65K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R15 | 0698-3279 | 0 | 5 | RESISTOR 4.99K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R16 | 0757-0472 | 5 | 1 | RESISTOR 200K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R17 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R18 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R19 | 0698-3499 | 6 | 1 | RESISTOR 40.2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R20-R21 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R22-R25 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R26 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R27 | 0757-0349 | 5 | 2 | RESISTOR 22.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R28 | 0757-0446 | 3 | 4 | RESISTOR 15K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R29 | 0698-3154 | 0 | 2 | RESISTOR 4.22K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R30 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R31 | 0698-3154 | 0 | | RESISTOR 4.22K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R32 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R33 | 0757-0349 | 5 | | RESISTOR 22.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R34 | 0757-0446 | 3 | | RESISTOR 15K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R35 | 0757-0465 | 6 | | RESISTOR 100K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R36 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R37 | 0757-0465 | 6 | | RESISTOR 100K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R38 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R39-R42 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R43-R44 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R45 | 0698-3519 | 1 | 2 | RESISTOR 12.4K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R46-R47 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| △ See backdating. | | | | | | |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------|
| A18R48 | 0698-3202 | 9 | 1 | RESISTOR 1.74K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R49 | 0757-0465 | 6 | | RESISTOR 100K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R50 | 0757-0446 | 3 | 1 | RESISTOR 15K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R51 | 0698-3268 | 7 | 1 | RESISTOR 11.5K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R52 | 0698-3519 | 1 | | RESISTOR 12.4K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R53-R54 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R60 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R61 | 0698-4486 | 3 | 1 | RESISTOR 24.9K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R62 | 0683-2055 | 7 | 1 | RESISTOR 2M 5% .25W CF TC=0-900 | 77902 | R-25J |
| A18R63 | 0757-0435 | 0 | 1 | RESISTOR 3.92K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R64 | 0757-0427 | 0 | 1 | RESISTOR 1.5K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R65 | 0757-0283 | 6 | 1 | RESISTOR 2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R66-R67 | 0698-3228 | 9 | 5 | RESISTOR 49.9K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R100 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R101 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R102 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R103 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R105 | 0698-3279 | 0 | | RESISTOR 4.99K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R106 | 0812-0047 | 8 | 1 | RESISTOR 5 5% 5W PW TC=0+-50 | 91637 | CW-5 |
| A18R107 | 0757-0420 | 3 | | RESISTOR 750 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R108-R109 | 0757-0384 | 8 | 2 | RESISTOR 20 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R110 | 0698-3225 | 6 | 1 | RESISTOR 1.43K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R111 | 0757-0283 | 6 | 3 | RESISTOR 2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R112 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R113 | 0698-3279 | 0 | | RESISTOR 4.99K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R116 | 0698-8827 | 4 | 3 | RESISTOR 1M 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R117 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R119-R120 | 0698-3228 | 9 | | RESISTOR 49.9K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R121 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R126 | 0698-8827 | 4 | | RESISTOR 1M 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R127 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R200 | 0698-3228 | 9 | | RESISTOR 49.9K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R201 | 0757-0449 | 6 | | RESISTOR 20K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R202 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R203 | 0698-3279 | 0 | | RESISTOR 4.99K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R204 | 0698-3162 | 0 | 2 | RESISTOR 46.4K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R205-R206 | 0698-0082 | 7 | 2 | RESISTOR 464 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R207 | 0698-3162 | 0 | | RESISTOR 46.4K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R209 | 0698-8827 | 4 | 1 | RESISTOR 1M 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R210 | 0757-0458 | 7 | 1 | RESISTOR 51.1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R212 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R300-R301 | 0698-3136 | 8 | 2 | RESISTOR 17.8K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R302 | 0698-3279 | 0 | | RESISTOR 4.99K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R303 | 0757-0283 | 6 | | RESISTOR 2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R304 | 0757-0465 | 6 | | RESISTOR 100K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R305 | 0757-0283 | 6 | | RESISTOR 2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R306 | 0698-3581 | 7 | 1 | RESISTOR 13.7K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R307 | 0698-4445 | 4 | 1 | RESISTOR 5.76K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R308 | 0757-0446 | 3 | | RESISTOR 15K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R309 | 0698-4461 | 4 | 1 | RESISTOR 698 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R310 | 63312-88002 | 1 | 1 | RES-SEN 1 OHM | 28480 | 63312-88002 |
| A18R311-R312 | 0698-3607 | 8 | 1 | RESISTOR 18 5% 2W MO TC=0+-200 | 11502 | GS-3 |
| A18R400 | 0698-3609 | 0 | 1 | RESISTOR 22 5% 2W MO TC=0+-200 | 11502 | GS-3 |
| A18R401 | 0686-4725 | 8 | 2 | RESISTOR 4.7K 5% .5W CC TC=0+647 | 01121 | EB4725 |
| A18R402 | 0764-0007 | 7 | | RESISTOR 27K 5% 2W MO TC=0+-200 | 11502 | GS-3 |
| A18R403 | 0699-1167 | 3 | 1 | RESISTOR-FUSE 18 OHM +-1%; .5W AT 70 DEG | 91637 | CMF60-64 |
| A18R404 | 0699-1168 | 4 | 1 | RESISTOR-FUSE 3.9K OHM +-2%; T.C. 0+-100 | 91637 | CMF60-64 |
| A18R405 | 0764-0007 | 7 | | RESISTOR 27K 5% 2W MO TC=0+-200 | 11502 | GS-3 |
| A18R406 | 0757-0442 | 9 | 1 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R407 | 0686-4725 | 8 | | RESISTOR 4.7K 5% .5W CC TC=0+647 | 01121 | EB4725 |
| A18R408 | 0698-3609 | 0 | | RESISTOR 22 5% 2W MO TC=0+-200 | 11502 | GS-3 |
| A18R409 | 0699-1167 | 3 | | RESISTOR-FUSE 18 OHM +-1%; .5W AT 70 DEG | 91637 | CMF60-64 |
| A18R410 | 0699-1168 | 4 | | RESISTOR-FUSE 3.9K OHM +-2%; T.C. 0+-100 | 91637 | CMF60-64 |
| A18R411 | 0837-0308 | 6 | 1 | THERMISTER 8 ADC | 15454 | SG-170 |
| A18R412-R413 | 0698-3609 | 0 | | RESISTOR 22 5% 2W MO TC=0+-200 | 11502 | GS-3 |
| A18R500 | 0698-3151 | 7 | 2 | RESISTOR 2.87K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R501 | 0698-4408 | 9 | 10 | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R502 | 0698-3151 | 7 | | RESISTOR 2.87K 1% .125W F TC=0+-100 | 19701 | 5033R |

See backdating.

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-------------------|
| A18R503 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R504 | 0698-3437 | 2 | 1 | RESISTOR 133 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R505 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R506 | 0757-0419 | 0 | 2 | RESISTOR 681 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R507 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R508 | 0757-0419 | 0 | | RESISTOR 681 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R509 | 0698-4408 | 9 | 1 | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R510 | 0698-4423 | 8 | 4 | RESISTOR 1.37K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R511 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R512 | 0698-4423 | 8 | | RESISTOR 1.37K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R513 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R514 | 0698-4423 | 8 | | RESISTOR 1.37K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R515 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R516 | 0698-4423 | 8 | | RESISTOR 1.37K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R517 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R518 | 0698-4196 | 2 | 2 | RESISTOR 1.07K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R519 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R520 | 0698-4196 | 2 | | RESISTOR 1.07K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R521 | 0698-4408 | 9 | | RESISTOR 124 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R600-R603 | 0698-3634 | 1 | 1 | RESISTOR 470 5% 2W MO TC=0+-200 | 11502 | GS-3 |
| A18R800 | 0698-4376 | 0 | 1 | RESISTOR 32.4 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A18R801 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R802 | 0757-0446 | 3 | | RESISTOR 15K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R803 | 0698-4123 | 5 | 1 | RESISTOR 499 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R804 | 0757-0449 | 6 | | RESISTOR 20K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18R805 | 0757-0465 | 6 | | RESISTOR 100K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A18SUP1-SUP2 | 1970-0094 | 0 | | TUBE-ELECTRON SURGE V PICTR | 71482 | CG2-250AL+-10% |
| A18T1 | 9100-4402 | 7 | 1 | PWR XFMR 128KHZ | 28480 | 9100-4402 |
| A18T2 | 9100-4348 | 0 | 1 | INDUCTOR-FIXED CURRENT SENSE INDUCTOR;L | 09161 | 51719 |
| A18T3 | 9100-4369 | 5 | 1 | BIAS XFMR | 28480 | 9100-4369 |
| A18T4 | 9140-0828 | 7 | 1 | GATE DRIVE TFMR | 28480 | 9140-0828 |
| A18TP1-TP15 | 1251-0600 | 0 | | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A18U1 | 1820-3670 | 7 | 1 | IC-D 74HC133 CMOS NANDGT P16 | 27014 | MM74HC133N |
| A18U2 | 1826-0138 | 8 | 4 | IC COMPARTOR GP QUAD 14-DIP-P PKG | 27014 | SL24958 |
| A18U3-U6 | 1820-2922 | 0 | 5 | IC GATE CMOS/74HC NAND QUAD 2-INP | 04713 | SC40291PK |
| A18U7-U8 | 1826-0138 | 8 | | IC COMPARTOR GP QUAD 14-DIP-P PKG | 27014 | SL24958 |
| A18U100 | 1820-2922 | 0 | | IC GATE CMOS/74HC NAND QUAD 2-INP | 04713 | SC40291PK |
| A18U101 | 1826-1040 | 3 | 1 | IC V RGLTR-SWG 4.85/5.15V 18-DIP-C PKG | 34333 | SG3526Z |
| A18U102 | 1820-1288 | 9 | 1 | IC DRVR TTL CLK TTL-TO-MOS 1-INP | 27014 | SD31013 |
| A18U103 | 1820-2656 | 7 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A18U104 | 1826-0138 | 8 | | IC COMPARTOR GP QUAD 14-DIP-P PKG | 27014 | SL24958 |
| A18U200 | 1826-1097 | 0 | 1 | IC OP AMP WB 8-DIP-C PKG | 06665 | OP-17 073Z |
| A18U300-U301 | 1826-0357 | 3 | | IC OP AMP WB TO-99 PKG | 27014 | SL32498 |
| A18U400 | 1906-0069 | 4 | 1 | DIODE-FW BRDG 400V 1A | 18546 | VM48 |
| A18U401 | 1906-0080 | 9 | 1 | DIODE-FW BRDG 600V 10A | 18546 | VJ647 |
| A18U500 | 1826-0393 | 7 | 7 | IC V RGLTR-ADJ-POS 1.2/37V TO-220 PKG | 27014 | SL33706 |
| A18U501 | 1826-0527 | 9 | 4 | IC V RGLTR-ADJ-NEG 1.2/37V TO-220 PKG | 27014 | SL35761 |
| A18U502-U506 | 1826-0393 | 7 | | IC V RGLTR-ADJ-POS 1.2/37V TO-220 PKG | 27014 | SL33706 |
| A18U507-U509 | 1826-0527 | 9 | | IC V RGLTR-ADJ-NEG 1.2/37V TO-220 PKG | 27014 | SL35761 |
| A18U510 | 1826-0393 | 7 | | IC V RGLTR-ADJ-POS 1.2/37V TO-220 PKG | 27014 | SL33706 |
| A18U511-U512 | 1906-0301 | 7 | 2 | DUAL RECT 200V 20A | 18546 | VHE2404 |
| A18U513-U514 | 1901-1157 | 3 | 2 | DIODE-GENERAL PURPOSE | 18546 | VHE1404 |
| A18U800 | 1826-0175 | 3 | 1 | IC COMPARTOR GP DUAL 14-DIP-P PKG | 27014 | SL26763 |
| A18W1-W10 | 1258-0141 | 8 | | JMPR-REM .025P | 22526 | 65474-004 |
| A18W400-W401 | 1258-0224 | 8 | | JUMPER, PROGRAMMING | M01051 | 461-2872-02-03-10 |
| | 2190-0004 | 9 | 15 | WASHER-LK INTL T NO. 4 .115-IN-ID | T12345 | SF 1904-00 |
| | 3050-0440 | 2 | 15 | WASHER-SHLDR NO. 4 .115-IN-ID .2-IN-OD | 86928 | 5607-45 |
| | 2200-0139 | 4 | 15 | SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI | 83486 | 2200-0139 |
| | 2260-0001 | 5 | 15 | NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK | T1234 | 2260-0001 |
| | 0340-0564 | 3 | 15 | INSULATOR-XSTR THRM-CNDCT | 55285 | 7403-09FR-51 |
| | 0515-0212 | 9 | 4 | SCREW-MACH M3.5 X 0.6 6MM-LG PAN-HD | 16941 | 0515-0212 |
| | 0535-0031 | 2 | 4 | NUT-HEX W/LKWR M3 X 0.5 2.4MM-THK | H01043 | 0535-0031 |
| | 0515-0413 | 2 | 3 | SCREW-MACH M4 X 0.7 6MM-LG PAN-HD | 16941 | 0515-0413 |
| | 1400-0249 | 0 | 3 | CABLE TIE .062-.625-DIA .091-WD NYL | 59730 | TY-23M-8 |
| | 1400-0507 | 3 | 3 | CABLE TIE .062-2-DIA .095-WD NYL | 59730 | TY-232M |
| | 2190-0027 | 6 | 2 | WASHER-LK INTL T 1/4 IN .256-IN-ID | T12345 | 1914-00 |
| | 2190-0060 | 7 | 2 | WASHER-LK INTL T 1/4 IN .256-IN-ID | T12345 | 1214-10 |
| | 2950-0134 | 8 | 2 | NUT-HEX-DBL-CHAM 1/4-28-THD .125-IN-THK | 70318 | 2950-0134 |

Δ See backdating.

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-------------------------|
| | 2360-0121 | 2 | 1 | SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI | 01536 | 2360-0121 |
| | 2420-0001 | 5 | 1 | NUT-HEX-W/LKWR 6-32-THD .109-IN-THK | T12345 | 511-061800-00-0280-2580 |
| | 1252-0139 | 2 | 1 | HEADER,RND-W,PLZ,15 CONT | 27264 | 10-19-1151 |
| | 1251-5383 | 6 | 1 | CONN-POST TYPE .100-PIN-SPCG 2-CONT | 27264 | 22-29-2021 |
| A22 | 03562-66522 | 0 | 1 | HPIB INTERFACE | 28480 | 03562-66522 |
| A22J1 | 1251-8517 | 4 | 1 | CONN-RECT MICRORBN 24-CKT 24-CONT | 00779 | 554194-2 |
| A22MP687 | 03577-24701 | 6 | 2 | SPACER | 76854 | 03577-24701 |
| A22W14 | 03562-61614 | 1 | 1 | CBLE ASSY DISP I/O | 28480 | 03562-61614 |
| | 2190-0918 | 4 | 2 | WASHER-LK HLCL NO. 6 .141-IN-ID | 73734 | 2190-0918 |
| | 0380-1214 | 6 | 2 | STANDOFF-HEX 4.7-MM-LG M3.5 X 0.6-THD | L01005 | 0380-1214 |
| | 0535-0007 | 2 | 2 | NUT-HEX DBL-CHAM M3.5 X 0.6 2.8MM-THK | H01043 | 0535-0007 |
| A30 | 03562-66530 | 0 | 1 | ASSY,SCE/ANLG | 28480 | 03562-66530 |
| A30C1 | 0160-4571 | 8 | 45 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C2 | 0160-0128 | 3 | 1 | CAPACITOR-FXD 2.2UF +-20% 50VDC CER | 13606 | 3C37Z5U225M050A |
| A30C3-C5 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C6-C7 | 0160-0127 | 2 | 1 | CAPACITOR-FXD 1UF +-20% 25VDC CER | 13606 | 2C37Z5U105M025A |
| A30C8 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C9 | 0160-0127 | 2 | 1 | CAPACITOR-FXD 1UF +-20% 25VDC CER | 13606 | 2C37Z5U105M025A |
| A30C10-C12 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C50-C51 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C54 | 0160-5439 | 9 | 1 | CAPACITOR-FXD 510PF +-5% 100VDC CER | 27167 | CAC03COG511J100A |
| A30C100 | 0160-4790 | 3 | 2 | CAPACITOR-FXD 12PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG120J100A |
| A30C101 | 0160-5404 | 8 | 1 | CAPACITOR-FXD 360PF +-5% 100VDC CER | 27167 | CAC02COG361J100A |
| A30C102 | 0160-4792 | 5 | 1 | CAPACITOR-FXD 8.2PF +-5PF 100VDC CER | 27167 | CAC02COG8R2D100A |
| A30C103 | 0160-4811 | 9 | 1 | CAPACITOR-FXD 270PF +-5% 100VDC CER | 27167 | CAC02COG271J100A |
| A30C104 | 0160-5889 | 3 | 1 | CAPACITOR-FXD 5600PF +-1% 50VDC CER | 27167 | CAC05COG562F050A |
| A30C105 | 0160-5877 | 9 | 1 | CAPACITOR-FXD 2400PF +-1% 50VDC CER | 27167 | CAC04COG242F050A |
| A30C106 | 0160-5890 | 6 | 1 | CAPACITOR-FXD 9100PF +-1% 50VDC CER | 27167 | CAC05COG912F050A |
| A30C108 | 0160-5878 | 0 | 1 | CAPACITOR-FXD 3600PF +-1% 50VDC CER | 27167 | CAC04COG362F050A |
| A30C109 | 0160-4794 | 7 | 1 | CAPACITOR-FXD 5.6PF +-5PF 100VDC CER | 27167 | CAC02COG5R6D100A |
| A30C110 | 0160-5405 | 9 | 1 | CAPACITOR-FXD 130PF +-5% 100VDC CER | 27167 | CAC02COG131J100A |
| A30C111 | 0160-5876 | 8 | 1 | CAPACITOR-FXD 1300PF +-1% 50VDC CER | 27167 | CAC03COG132F050A |
| A30C150-C151 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C152 | 0160-3046 | 0 | 1 | CAPACITOR-FXD 250PF +-1% 100VDC MICA | 09023 | 0160-3046 |
| A30C250-C254 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C255 | 0160-4790 | 3 | 1 | CAPACITOR-FXD 12PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG120J100A |
| A30C300 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C301 | 0160-0127 | 2 | 1 | CAPACITOR-FXD 1UF +-20% 25VDC CER | 13606 | 2C37Z5U105M025A |
| A30C302-C308 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C350 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C352 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C353 | 0160-4803 | 9 | 1 | CAPACITOR-FXD 68PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG680J100A |
| A30C354 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C355 | 0180-0100 | 3 | 1 | CAPACITOR-FXD 4.7UF+-10% 35VDC TA | 13606 | 150D475X9035B2-DYS |
| A30C356-C357 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C400-C401 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C402 | 0160-2530 | 5 | 1 | CAPACITOR-FXD 180PF +-2% 300VDC MICA | 00853 | 0160-2530 |
| A30C403-C404 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C450-C452 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C500-C502 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C551-C553 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C600-C603 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A30C650-C651 | 0180-3113 | 4 | 1 | CAPACITOR-FXD 330UF+50-10% 25VDC AL | P01016 | ECEB1EV331S |
| A30C652 | 0180-0228 | 6 | 1 | CAPACITOR-FXD 22UF+-10% 15VDC TA | 13606 | 150D226X9015B2-DYS |
| A30CR1 | 1902-0686 | 3 | 1 | DIODE-ZNR 6.2V 2% DO-7 PD=.4W TC=+.002% | 04713 | SZ 12170 |
| A30CR250-CR251 | 1901-0050 | 3 | 6 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A30CR402-CR403 | 1901-0050 | 3 | 3 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A30CR500-CR502 | 1901-1080 | 1 | 3 | DIODE-SCHOTTKY 1N5817 20V 1A | 04713 | SBR5120KBRL |
| A30CR600-CR601 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A30J200 | 1250-1255 | 1 | 1 | CONNECTOR-RF SMB M PC 50-OHM | 98291 | 51-051-0000 |
| A30J350 | 1251-4670 | 2 | 2 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A30J550 | 1251-4670 | 2 | 2 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|----------------------|
| A30K200-K202 | 0490-1403 | 8 | 3 | RELAY-REED 1A 500MA 200VDC 5VDC-COIL | 71707 | 2900-0022 |
| A30L100 | 03562-60301 | 1 | 1 | IND 393.8 | 28480 | 03562-60301 |
| A30L101 | 03562-60300 | 0 | 1 | IND 335 | 28480 | 03562-60300 |
| A30L151 | 9100-1665 | 8 | 1 | INDUCTOR RF-CH-MLD 3.3MH 5% .23DX.57LG | 24226 | 22M334J |
| A30L650-L651 | 9140-0748 | 0 | 1 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A30L652 | 9100-1788 | 6 | 1 | CORE-FERRITE CHOKE-WIDEBAND;IMP:>680 | 02114 | VK200 20/4B |
| A30P30 | 1251-7629 | 7 | 1 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 00779 | 532955-7 |
| A30Q1-Q3 | 1854-0215 | 1 | 1 | TRANSISTOR NPN SI PD=350MW FT=300MHZ | 04713 | SPS 3611 |
| A30R1 | 0683-4705 | 8 | 2 | RESISTOR 47 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R2 | 0683-5125 | 8 | 2 | RESISTOR 5.1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R3 | 0757-0449 | 6 | 1 | RESISTOR 20K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R4 | 0698-4438 | 5 | 1 | RESISTOR 3.09K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A30R5 | 0698-6625 | 6 | 2 | RESISTOR 6K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A30R6 | 0698-6377 | 5 | 2 | RESISTOR 200 .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A30R7 | 0757-0401 | 0 | 6 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R8 | 0698-6625 | 6 | 1 | RESISTOR 6K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A30R9 | 2100-3095 | 5 | 1 | RESISTOR-TRMR 200 10% C SIDE-ADJ 17-TRN | 73138 | 89PR200 |
| A30R10 | 2100-3164 | 9 | 1 | RESISTOR-TRMR 10 20% C SIDE-ADJ 17-TRN | 73138 | 89PR10 |
| A30R11 | 0757-0462 | 3 | 3 | RESISTOR 75K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R12 | 0757-0462 | 3 | 3 | RESISTOR 75K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R13 | 0683-5125 | 8 | 1 | RESISTOR 5.1K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R14 | 0698-3484 | 9 | 1 | RESISTOR 6.65K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R15 | 0757-0442 | 5 | 3 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R16 | 0698-6806 | 5 | 1 | RESISTOR 119.3 .25% .125W F TC=0+-25 | 19701 | 5033R |
| A30R17 | 0683-4705 | 8 | 1 | RESISTOR 47 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R18 | 0698-6624 | 5 | 2 | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A30R19 | 0698-6362 | 8 | 3 | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A30R20 | 0698-4376 | 0 | 1 | RESISTOR 32.4 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A30R21 | 0698-4492 | 1 | 1 | RESISTOR 32.4K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A30R22 | 0757-0280 | 3 | 2 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R50 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R51 | 0698-3518 | 0 | 1 | RESISTOR 7.32K 1% .125W R TC=0+-100 | 19701 | 5033R |
| A30R54 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R100 | 0698-6624 | 5 | 1 | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A30R101 | 0698-6377 | 5 | 1 | RESISTOR 200 .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A30R150-R151 | 0698-6362 | 8 | 1 | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A30R152 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R153 | 0698-4123 | 5 | 4 | RESISTOR 499 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R154 | 0698-8827 | 4 | 1 | RESISTOR 1M 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R156 | 0698-6322 | 0 | 1 | RESISTOR 4K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A30R250 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R300-R301 | 0698-8607 | 8 | 2 | RESISTOR 4.5K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A30R302 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R303 | 0683-1855 | 3 | 1 | RESISTOR 1.8M 5% .25W CF TC=0-900 | 77902 | R-25J |
| A30R304-R305 | 0699-0533 | 5 | 2 | RESISTOR 4.64K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A30R306-R307 | 0757-0277 | 8 | 2 | RESISTOR 49.9 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R351 | 0757-0283 | 6 | 1 | RESISTOR 2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R355 | 0698-4123 | 5 | 1 | RESISTOR 499 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R356 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R401 | 0698-3279 | 0 | 1 | RESISTOR 4.99K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R402 | 0698-6320 | 8 | 2 | RESISTOR 5K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A30R403 | 0698-6320 | 8 | 1 | RESISTOR 5K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A30R404 | 0757-0072 | 1 | 1 | RESISTOR 49.9 1% .5W F TC=0+-100 | 19701 | 5053R |
| A30R405 | 0837-0275 | 6 | 1 | THERMISTOR DISC 50-OHM TC=+2.35%/C-DEG | 75263 | RL3006-50-110-25-PTO |
| A30R406 | 0757-0462 | 3 | 1 | RESISTOR 75K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R407 | 0683-2225 | 3 | 8 | RESISTOR 2.2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R408-R409 | 0757-0991 | 3 | 1 | RESISTOR 20 1% .5W F TC=0+-100 | 19701 | 5053R |
| A30R450 | 0683-2225 | 3 | 1 | RESISTOR 2.2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R501-R504 | 0683-2225 | 3 | 1 | RESISTOR 2.2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R506 | 0683-2225 | 3 | 1 | RESISTOR 2.2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R550 | 0683-2225 | 3 | 1 | RESISTOR 2.2K 5% .25W CF TC=0-400 | 77902 | R-25J |
| A30R600 | 0698-4123 | 5 | 1 | RESISTOR 499 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R601 | 0757-0442 | 9 | 1 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R602 | 0698-4123 | 5 | 1 | RESISTOR 499 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R603 | 0698-3155 | 1 | 1 | RESISTOR 4.64K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30R604 | 0757-0442 | 9 | 1 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A30TP1-TP11 | 1251-0600 | 0 | 1 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A30TP13-TP15 | 1251-0600 | 0 | 1 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A30U1 | 1820-0493 | 6 | 2 | IC OP AMP GP 8-DIP-P PKG | 27014 | SL10084 |
| A30U2 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A30U50 | 1826-0601 | 0 | 1 | IC OP AMP PRCN TO-99 PKG | 06665 | OP-16 008J |
| A30U150 | 1826-0601 | 0 | 0 | IC OP AMP PRCN TO-99 PKG | 06665 | OP-16 008J |
| A30U151 | 1826-0778 | 2 | 1 | ANALOG SWITCH 2 SPST 14 -DIP-P | 17856 | DG300CJ |
| A30U250 | 1826-0601 | 0 | 0 | IC OP AMP PRCN TO-99 PKG | 06665 | OP-16 008J |
| A30U251 | 1826-0838 | 5 | 1 | D/A 10-BIT 16-PLASTIC CMOS | 24355 | AD11/435 |
| A30U300 | 1820-0493 | 6 | 1 | IC OP AMP GP 8-DIP-P PKG | 27014 | SL10084 |
| A30U301 | 1820-1934 | 2 | 1 | D/A 8-BIT 16-CERDIP BPLR | 06665 | DAC-08 096Q |
| A30U350 | 1826-1097 | 0 | 1 | IC OP AMP WB 8-DIP-C PKG | 06665 | OP-17 073Z |
| A30U351 | 1826-0726 | 0 | 1 | D/A 12-BIT 24-DIP-C BPLR | 24355 | AD40997 |
| A30U352 | 1820-0224 | 1 | 1 | IC OP AMP SPCL TO-99 PKG | 27014 | SH08495 |
| A30U400 | 1826-0601 | 0 | 1 | IC OP AMP PRCN TO-99 PKG | 06665 | OP-16 008J |
| A30U401 | 1820-0224 | 1 | 1 | IC OP AMP SPCL TO-99 PKG | 27014 | SH08495 |
| A30U401 | 1205-0011 | 0 | 1 | HEAT SINK TO-5/TO-39-CS | 98978 | TXBF-032-025B |
| A30U450 | 1820-2096 | 9 | 1 | IC CNTR TTL LS BIN DUAL 4-BIT | 01295 | SN59197N |
| A30U451 | 1820-2488 | 3 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A30U452 | 1820-1244 | 7 | 1 | IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL | 01295 | SN53619 |
| A30U453 | 1820-1211 | 8 | 1 | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN53518N |
| A30U454 | 1820-2773 | 9 | 1 | IC GATE TTL ALS NAND 8-INP | 01295 | SN71544N |
| A30U455 | 1820-1433 | 6 | 2 | IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT | 01295 | SN57194 |
| A30U456 | 1820-2656 | 7 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A30U500 | 1820-3318 | 0 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG COM | 01295 | SN71690N |
| A30U501 | 1820-1433 | 6 | 1 | IC SHF-RGTR TTL LS R-S SERIAL-IN PRL-OUT | 01295 | SN57194 |
| A30U502 | 1820-2313 | 3 | 1 | IC SHF-RGTR TTL LS SERIAL-IN SERIAL-OUT | 01295 | SN70509N |
| A30U503 | 1820-1209 | 4 | 1 | IC BFR TTL LS NAND QUAD 2-INP | 01295 | SN53516 |
| A30U550-U551 | 1820-1196 | 8 | 2 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN53525 |
| A30U552-U553 | 1820-1987 | 5 | 2 | IC SHF-RGTR TTL LS COM CLEAR STOR 8-BIT | 34335 | AM74LS299N |
| A30U554 | 1820-2634 | 1 | 1 | IC INV TTL ALS HEX | 01295 | SN71332N |
| A30U600 | 1826-0175 | 3 | 1 | IC COMPARATOR GP DUAL 14-DIP-P PKG | 27014 | SL26763 |
| A30W350 | 1258-0141 | 8 | 2 | JMPR-REM .025P | 22526 | 65474-004 |
| A30W550 | 1258-0141 | 8 | 8 | JMPR-REM .025P | 22526 | 65474-004 |
| | 0360-1917 | 4 | 1 | TERMINAL-STUD SPCL-FDTHRU PRESS-MTG | 98291 | 011-6812-00-0-206 |
| | 5000-9043 | 6 | 1 | PIN EXTR | 28480 | 5000-9043 |
| A31 | 03562-66531 | 1 | 1 | PC BD-TRIGGER | 28480 | 03562-66531 |
| A31C1-C2 | 0180-0116 | 1 | 1 | CAPACITOR-FXD 6.8UF+-10% 35VDC TA | 13606 | 150D685X9035B2-DYS |
| A31C3 | 0180-0228 | 6 | 1 | CAPACITOR-FXD 22UF+-10% 15VDC TA | 13606 | 150D226X9015B2-DYS |
| A31C4-C5 | 0180-0291 | 3 | 1 | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A31C6-C7 | 0160-2414 | 4 | 2 | CAPACITOR-FXD .022UF +-5% 200VDC POLYE | 13606 | 192P22352 |
| A31C8-C10 | 0160-4571 | 8 | 45 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C11-C12 | 0160-4791 | 4 | 8 | CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG100J100A |
| A31C13-C15 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C16 | 0160-4801 | 7 | 3 | CAPACITOR-FXD 100PF +-5% 100VDC CER | 27167 | CAC02COG101J100A |
| A31C17-C18 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C19 | 0160-4791 | 4 | 5 | CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG100J100A |
| A31C20-C21 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C22 | 0160-4832 | 4 | 8 | CAPACITOR-FXD .01UF +-10% 100VDC CER | 27167 | CAC02X7R103K100A |
| A31C23-C27 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C28 | 0180-0228 | 6 | 6 | CAPACITOR-FXD 22UF+-10% 15VDC TA | 13606 | 150D226X9015B2-DYS |
| A31C29-30 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C45 | 0180-0116 | 1 | 1 | CAPACITOR-FXD 6.8UF+-10% 35VDC TA | 13606 | 150D685X9035B2-DYS |
| A31C101C103 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C104 | 0160-5880 | 4 | 1 | CAPACITOR-FXD 2200PF +-1% 50VDC CER | 27167 | CAC03COG222F050A |
| A31C105 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C106-C107 | 0160-4801 | 7 | 7 | CAPACITOR-FXD 100PF +-5% 100VDC CER | 27167 | CAC02COG101J100A |
| A31C108 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C109 | 0160-5099 | 7 | 2 | CAPACITOR-FXD 3300PF +-5% 100VDC CER | 27167 | CAC05COG332J100A |
| A31C110-C111 | 0160-4812 | 0 | 2 | CAPACITOR-FXD 220PF +-5% 100VDC CER | 27167 | CAC02COG221J100A |
| A31C112 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C113 | 0160-5099 | 7 | 7 | CAPACITOR-FXD 3300PF +-5% 100VDC CER | 27167 | CAC05COG332J100A |
| A31C108 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C109 | 0160-5099 | 7 | 2 | CAPACITOR-FXD 3300PF +-5% 100VDC CER | 27167 | CAC05COG332J100A |
| A31C110-C111 | 0160-4812 | 0 | 2 | CAPACITOR-FXD 220PF +-5% 100VDC CER | 27167 | CAC02COG221J100A |
| A31C112 | 0160-4571 | 8 | 8 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C113 | 0160-5099 | 7 | 7 | CAPACITOR-FXD 3300PF +-5% 100VDC CER | 27167 | CAC05COG332J100A |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A31C114-C115 | 0160-4832 | 4 | | CAPACITOR-FXD .01UF +-10% 100VDC CER | 27167 | CAC02X7R103K100A |
| A31C116-C117 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C118 | 0160-4832 | 4 | | CAPACITOR-FXD .01UF +-10% 100VDC CER | 27167 | CAC02X7R103K100A |
| A31C119-C120 | 0180-0291 | 3 | | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A31C201 | 0160-4835 | 7 | 1 | CAPACITOR-FXD .1UF +-10% 50VDC CER | 27167 | CAC04X7R104K050A |
| A31C202 | 0160-0127 | 2 | 1 | CAPACITOR-FXD 1UF +-20% 25VDC CER | 13606 | 2637Z5U105M025A |
| A31C203-C203 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C205 | 0180-0228 | 6 | | CAPACITOR-FXD 22UF+-10% 15VDC TA | 13606 | 150D226X9015B2-DYS |
| A31C206 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C208 | 0160-4832 | 4 | | CAPACITOR-FXD .01UF +-10% 100VDC CER | 27167 | CAC02X7R103K100A |
| A31C209-C210 | 0160-4791 | 4 | | CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG100J100A |
| A31C301 | 0160-4005 | 3 | 1 | CAPACITOR-FXD 1UF +-20% 100VDC CER | 04222 | SR401E105MAA |
| A31C302-C308 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C309 | 0160-4787 | 8 | 1 | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A31C402 | 0180-0228 | 6 | | CAPACITOR-FXD 22UF+-10% 15VDC TA | 13606 | 150D226X9015B2-DYS |
| A31C404 | 0160-4832 | 4 | | CAPACITOR-FXD .01UF +-10% 100VDC CER | 27167 | CAC02X7R103K100A |
| A31C406 | 0160-4811 | 9 | 1 | CAPACITOR-FXD 270PF +-5% 100VDC CER | 27167 | CAC02COG271J100A |
| A31C407 | 0160-4823 | 3 | 1 | CAPACITOR-FXD 820PF +-5% 100VDC CER | 27167 | CAC03COG821J100A |
| A31C408-C409 | 0160-4822 | 2 | 2 | CAPACITOR-FXD 1000PF +-5% 100VDC CER | 27167 | CAC03COG102J100A |
| A31C410 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C411 | 0160-4832 | 4 | | CAPACITOR-FXD .01UF +-10% 100VDC CER | 27167 | CAC02X7R103K100A |
| A31C412 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31C413 | 0160-4832 | 4 | | CAPACITOR-FXD .01UF +-10% 100VDC CER | 27167 | CAC02X7R103K100A |
| A31C501-C509 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A31CR1 | 1902-3097 | 6 | 1 | DIODE-ZNR 5.23V 2% DO-35 PD=.4W | 04713 | SZ30016-102 |
| A31CR2-CR3 | 1902-0958 | 2 | | DIODE-ZNR 10V 5% DO-35 PD=.4W TC=+.075% | 04713 | SZ30035-016 |
| A31CR101-CR104 | 1901-0040 | 1 | 8 | DIODE-SWITCHING 30V 50MA 2NS DO-35 | 07263 | FDH1088 |
| A31CR105-CR106 | 1901-0050 | 3 | 6 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A31CR107-CR110 | 1901-0040 | 1 | | DIODE-SWITCHING 30V 50MA 2NS DO-35 | 07263 | FDH1088 |
| A31CR201-CR202 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A31CR203 | 1902-0950 | 4 | 1 | DIODE-ZNR 4.7V 5% DO-35 PD=.4W TC=+.025% | 04713 | SZ30035-008 |
| A31CR204 | 0757-0274 | 5 | 1 | RESISTOR 1.21K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31CR301-CR302 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A31CR303-CR304 | 1902-0958 | 2 | | DIODE-ZNR 10V 5% DO-35 PD=.4W TC=+.075% | 04713 | SZ30035-016 |
| A31CR401 | 1901-0040 | 1 | 1 | DIODE-SWITCHING 30V 50MA 2NS DO-35 | 07263 | FDH1088 |
| A31CR402-CR403 | 0122-0162 | 5 | 2 | DIODE-VVC 29PF 10% BVR=30V | 25403 | BB809 |
| A31CR501-CR502 | 1901-1080 | 1 | 2 | DIODE-SCHOTTKY 1N5817 20V 1A | 04713 | SBR5120KBRL |
| A31J1 | 1250-1255 | 1 | 3 | CONNECTOR-RF SMB M PC 50-OHM | 98291 | 51-051-0000 |
| A31J201 | 1251-4670 | 2 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 22526 | 65500-103 |
| A31J301 | 1250-1255 | 1 | | CONNECTOR-RF SMB M PC 50-OHM | 98291 | 51-051-0000 |
| A31J501 | 1250-1255 | 1 | | CONNECTOR-RF SMB M PC 50-OHM | 98291 | 51-051-0000 |
| A31L1-L2 | 9140-0748 | 0 | 1 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A31L3-L4 | 9100-1788 | 6 | 1 | CORE-FERRITE CHOKE-WIDEBAND;IMP:>680 | 02114 | VK200 20/4B |
| A31L5-L6 | 9100-1622 | 7 | 1 | INDUCTOR RF-CH-MLD 24UH 5% .166DX.385LG | 06560 | 15-4455-1J |
| A31L101 | 9100-3912 | 2 | 1 | INDUCTOR RF-CH-MLD 15UH 5% .166DX.385LG | 24226 | 15M152J |
| A31L102 | 9100-3341 | 1 | 1 | INDUCTOR RF-CH-MLD 1UH 2% .166DX.385LG | 06560 | 4425-6G |
| A31L103-L104 | 9100-2574 | 0 | 2 | INDUCTOR RF-CH-MLD 1.2MH 10% | 24226 | 9100-2574 |
| A31L401 | 9140-0253 | 2 | 1 | INDUCTOR RF-CH-MLD 300NH 1% .166DX.385LG | 24226 | 15M300F-1 |
| A31L402 | 9140-0454 | 5 | 1 | INDUCTOR RF-CH-MLD 18UH 5% .166DX.385LG | 24226 | 15M-182J |
| A31L403 | 9140-0399 | 7 | 1 | INDUCTOR RF-CH-MLD 2.2UH 5% .166DX.385LG | 24226 | 15M221J |
| A31P1 | 1251-7629 | 7 | 1 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 00779 | 532955-7 |
| A31Q101 | 1853-0010 | 2 | 1 | TRANSISTOR PNP SI TO-18 PD=360MW | 04713 | SM4713 |
| A31Q102-Q103 | 1853-0089 | 5 | 1 | TRANSISTOR PNP 2N4917 SI PD=200MW | 07263 | S33022 |
| A31Q104 | 1853-0010 | 2 | | TRANSISTOR PNP SI TO-18 PD=360MW | 04713 | SM4713 |
| A31Q105-Q106 | 1853-0089 | 5 | | TRANSISTOR PNP 2N4917 SI PD=200MW | 07263 | S33022 |
| A31Q201 | 1855-0410 | 0 | 1 | TRANSISTOR J-FET N-CHAN D-MODE TO-18 SI | 27014 | SF51006 |
| A31Q401-Q402 | 1854-0215 | 1 | | TRANSISTOR NPN SI PD=350MW FT=300MHZ | 04713 | SPS 3611 |
| A31Q403 | 1854-0019 | 3 | 1 | TRANSISTOR NPN SI TO-18 PD=360MW | 07263 | S-6516 |
| A31R1-R2 | 0757-0346 | 2 | 5 | RESISTOR 10 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A31R3-R5 | 0757-0394 | 0 | 12 | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R6 | 0698-4740 | 2 | 1 | RESISTOR 42.2K 1% .25W F TC=0+-100 | 91637 | CMF-60-1, T-1 |
| A31R7 | 0698-7579 | 1 | 1 | RESISTOR 7.853K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A31R8 | 0698-3259 | 6 | 3 | RESISTOR 7.87K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R9 | 0757-0438 | 3 | 1 | RESISTOR 5.11K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R10 | 0757-0394 | 0 | | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R11 | 0757-0280 | 3 | 28 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R12-R13 | 0698-6366 | 2 | 2 | RESISTOR 800 .1% .125W F TC=0+-25 | 19701 | 5033R |
| A31R14 | 0698-3157 | 3 | 7 | RESISTOR 19.6K 1% .125W F TC=0+-100 | 19701 | 5033R |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|---|----------|-----------------|
| A31R15 | 0698-6348 | 0 | 1 | RESISTOR 3K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A31R16 | 0698-0085 | 0 | 3 | RESISTOR 2.61K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R17 | 0757-0726 | 2 | 1 | RESISTOR 511 1% .25W F TC=0+-100 | 19701 | 5043R |
| A31R18 | 0757-0416 | 7 | 3 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R19 | 0698-3132 | 4 | 4 | RESISTOR 261 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R20 | 0757-0411 | 2 | 2 | RESISTOR 332 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R21 | 0757-0394 | 0 | 0 | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R22 | 0698-0085 | 0 | 0 | RESISTOR 2.61K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R23 | 0698-4496 | 5 | 2 | RESISTOR 45.3K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A31R24 | 0698-0085 | 0 | 0 | RESISTOR 2.61K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R25 | 0757-0280 | 3 | 3 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R26 | 0698-4496 | 5 | 5 | RESISTOR 45.3K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A31R27-R28 | 0757-0280 | 3 | 3 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R29 | 8150-3375 | 5 | 1 | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A31R30-R34 | 0757-0280 | 3 | 3 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R101-R102 | 0757-0346 | 2 | 2 | RESISTOR 10 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A31R103 | 0698-0083 | 8 | 2 | RESISTOR 1.96K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R104 | 0757-0273 | 4 | 3 | RESISTOR 3.01K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R105 | 0757-0394 | 0 | 0 | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R106 | 0698-3488 | 3 | 1 | RESISTOR 442 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R107 | 0698-3447 | 4 | 1 | RESISTOR 422 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R108 | 0698-3157 | 3 | 3 | RESISTOR 19.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R109 | 0757-0410 | 1 | 2 | RESISTOR 301 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R110-R111 | 0757-0394 | 0 | 0 | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R112 | 0757-0338 | 2 | 2 | RESISTOR 1K 1% .25W F TC=0+-100 | 19701 | 5043R |
| A31R113 | 0757-0280 | 3 | 3 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R114 | 0757-0273 | 4 | 4 | RESISTOR 3.01K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R115 | 0757-0442 | 9 | 4 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R116 | 0698-3259 | 6 | 6 | RESISTOR 7.87K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R117 | 0757-0442 | 9 | 9 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R118 | 0698-3160 | 8 | 4 | RESISTOR 31.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R119 | 0698-3259 | 6 | 6 | RESISTOR 7.87K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R120 | 0698-3160 | 8 | 8 | RESISTOR 31.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R121 | 0757-0280 | 3 | 3 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R122 | 0698-3160 | 8 | 8 | RESISTOR 31.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R123 | 0698-3157 | 3 | 3 | RESISTOR 19.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R124 | 0757-0394 | 0 | 0 | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R125 | 0757-0419 | 0 | 1 | RESISTOR 681 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R126 | 0698-0084 | 9 | 1 | RESISTOR 2.15K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R127 | 0757-0410 | 1 | 1 | RESISTOR 301 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R128 | 0757-0394 | 0 | 0 | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R129 | 0757-0280 | 3 | 3 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R130-R131 | 0757-0338 | 2 | 2 | RESISTOR 1K 1% .25W F TC=0+-100 | 19701 | 5043R |
| A31R132-R133 | 0698-8958 | 2 | 3 | RESISTOR 511K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R134 | 0698-3132 | 4 | 4 | RESISTOR 261 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R201 | 0698-8827 | 4 | 2 | RESISTOR 1M 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R202 | 0757-0442 | 9 | 9 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R203-R204 | 0698-3451 | 0 | 2 | RESISTOR 133K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R205 | 0698-3157 | 3 | 3 | RESISTOR 19.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R206 | 0698-8827 | 4 | 3 | RESISTOR 1M 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R207 | 1902-0777 | 3 | 1 | DIODE-ZNR 1N825 6.2V 5% DO-7 PD-.4W | 04713 | SZ14376RL |
| A31R208 | 2100-3103 | 6 | 1 | RESISTOR-TRMR 10K 10% C SIDE-ADJ 17-TRN | 73138 | 89PR10K |
| A31R209 | 0757-0442 | 9 | 9 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R210 | 0757-0463 | 4 | 1 | RESISTOR 82.5K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R211 | 0757-0440 | 7 | 1 | RESISTOR 7.5K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R212 | 0698-3160 | 8 | 8 | RESISTOR 31.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R213 | 0699-0121 | 7 | 1 | RESISTOR 2.05M 1% .125W F TC=0+-100 | D8439 | MK2 |
| A31R214 | 0698-3515 | 7 | 2 | RESISTOR 5.9K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R215 | 0698-8958 | 2 | 2 | RESISTOR 511K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R216 | 0698-3449 | 6 | 1 | RESISTOR 28.7K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R217 | 0757-0280 | 3 | 3 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R218 | 0757-0442 | 9 | 1 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R301 | 0757-0072 | 1 | 1 | RESISTOR 49.9 1% .5W F TC=0+-100 | 19701 | 5053R |
| A31R302 | 0698-0082 | 7 | 1 | RESISTOR 464 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R304 | 0757-0416 | 7 | 1 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R305 | 0757-0411 | 2 | 2 | RESISTOR 332 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R306 | 0698-3157 | 3 | 3 | RESISTOR 19.6K 1% .125W F TC=0+-100 | 19701 | 5033R |

See introduction to this section for ordering information
*Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|----------------------|
| A31R307 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R308 | 0698-3157 | 3 | | RESISTOR 19.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R309 | 0757-0416 | 7 | | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R310-R313 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R314 | 0698-3515 | 7 | | RESISTOR 5.9K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R401 | 0757-0273 | 4 | | RESISTOR 3.01K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R402 | 0698-0083 | 8 | | RESISTOR 1.96K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R403 | 0757-0394 | 0 | | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R404 | 0757-0416 | 7 | 1 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R405 | 0698-0082 | 7 | 1 | RESISTOR 464 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R406 | 0757-0394 | 0 | | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R407 | 0698-0082 | 7 | | RESISTOR 464 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R408 | 0757-0394 | 0 | 1 | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R409 | 0698-0083 | 8 | 1 | RESISTOR 1.96K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R410-R412 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R413-R414 | 0698-3132 | 4 | | RESISTOR 261 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R415 | 0757-0394 | 0 | | RESISTOR 51.1 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R416 | 0757-0346 | 2 | | RESISTOR 10 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A31R417-R419 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R501-R508 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R510 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31R511 | 0837-0275 | 6 | 1 | THERMISTOR DISC 50-OHM TC=+2.35%/C-DEG | 75263 | RL3006-50-110-25-PTO |
| A31R512 | 0698-3157 | 3 | | RESISTOR 19.6K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A31TP1-TP19 | 1251-0600 | 0 | 19 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| A31U1 | 1826-0488 | 1 | | IC OP AMP WB TO-99 PKG | 27014 | SL34907 |
| A31U2 | 1826-0846 | 5 | 1 | ANALOG SWITCH 4 SPST 16 -CBRZ/SDR | 27014 | LF13332D |
| A31U3 | 1820-1281 | 2 | 1 | IC DCDR TTL LS 2-TO-4-LINE DUAL | 01295 | SN53657 |
| A31U4 | 1820-2313 | 3 | 1 | IC SHF-RGTR TTL LS SERIAL-IN SERIAL-OUT | 01295 | SN70509N |
| A31U5 | 1826-0035 | 4 | 1 | IC OP AMP LOW-DRIFT TO-99 PKG | 27014 | SL12451 |
| A31U6 | 1820-1934 | 2 | 1 | D/A 8-BIT 16-CERDIP BPLR | 06665 | DAC-08 096Q |
| A31U7 | 1826-0210 | 7 | 2 | IC COMPARATOR HS 14-DIP-P PKG | 27014 | SL27610 |
| A31U8 | 1820-1211 | 8 | 1 | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN53518N |
| A31U9 | 1820-3145 | 1 | 1 | IC DRVR TTL ALS BUS OCTL | 01295 | SN71649N |
| A31U101 | 1826-0521 | 3 | 1 | IC OP AMP LOW-BIAS-H-IMPD DUAL 8-DIP-P | 01295 | SN99855P |
| A31U201 | 1826-0522 | 4 | 1 | IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-P | 01295 | SN99856N |
| A31U301 | 1826-0210 | 7 | | IC COMPARATOR HS 14-DIP-P PKG | 27014 | SL27610 |
| A31U302 | 1820-2772 | 8 | 2 | IC FF TTL ALS J-K NEG-EDGE-TRIG | 01295 | SN71543N |
| A31U303 | 1820-1422 | 3 | 1 | IC MV TTL LS MONOSTBL RETRIG | 01295 | SN57183 |
| A31U304-U305 | 1820-2779 | 5 | | IC CNTR TTL ALS BIN SYNCHRO | 01295 | SN71537N |
| A31U401 | 1820-2656 | 7 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A31U501 | 1820-1415 | 4 | 1 | IC SCHMITT-TRIG TTL LS NAND DUAL 4-INP | 01295 | SN57176 |
| A31U502-U503 | 1820-0697 | 2 | 2 | IC DRVR TTL S NAND LINE DUAL 4-INP | 01295 | SN24665 |
| A31U504 | 1820-2776 | 2 | 2 | IC CNTR TTL ALS DECD SYNCHRO | 01295 | SN71744N |
| A31U505 | 1820-2772 | 8 | | IC FF TTL ALS J-K NEG-EDGE-TRIG | 01295 | SN71543N |
| A31U506 | 1820-2776 | 2 | | IC CNTR TTL ALS DECD SYNCHRO | 01295 | SN71744N |
| A31U507-U508 | 1820-2691 | 0 | 2 | IC FF TTL F D-TYPE POS-EDGE-TRIG | 07263 | SL82685 |
| A31W201 | 1258-0141 | 8 | 1 | JMPR-REM .025F | 22526 | 65474-004 |
| A31Y401 | 0410-1503 | 1 | 1 | CRYSTAL-QUARTZ 20.48 MHZ HC-18/U-HLDR | 33096 | 0410-1503 |
| | 5000-9043 | 6 | 1 | PIN EXTR | 28480 | 5000-9043 |
| A32, A34 | 03562-66532 | 2 | 2 | PC BOARD ASSY ADC | 28480 | 03562-66532 |
| A32C100-C101 | 0160-4571 | 8 | 36 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C104 | 0180-0291 | 3 | | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A32C200-C201 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C202 | 0160-3847 | 9 | 1 | CAPACITOR-FXD .01UF +100-0% 50VDC CER | 04222 | SA105C103KAA |
| A32C203 | 0180-0291 | 3 | | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A32C204-C205 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C300 | 0160-5865 | 5 | 1 | CAPACITOR-FXD 36PF +-5% 200VDC CER 0+-30 | U01025 | C114G360J2G5CA |
| A32C301 | 0160-5862 | 2 | 1 | CAPACITOR-FXD 240PF +-1% 100VDC CER | U01025 | C114G241F1G5CA |
| A32C302-C303 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C304 | 0160-5872 | 4 | 1 | CAPACITOR-FXD 750PF +-1% 100VDC CER | 27167 | CAC03COG751F100A |
| A32C305-C306 | 0160-5861 | 1 | | CAPACITOR-FXD 100PF +-1% 100VDC CER | 27167 | CAC02COG101F100A |
| A32C307 | 0160-5870 | 2 | 1 | CAPACITOR-FXD 430PF +-1% 100VDC CER | 27167 | CAC03COG431F100A |
| A32C308 | 0160-4788 | 9 | 1 | CAPACITOR-FXD 18PF +-5% 100VDC CER 0+-30 | 04222 | MA101A180JAA |
| A32C309-C310 | 0160-5874 | 6 | 2 | CAPACITOR-FXD 2000PF +-1% 50VDC CER | 27167 | CAC03COG202F050A |
| A32C311 | 0160-5861 | 1 | | CAPACITOR-FXD 100PF +-1% 100VDC CER | 27167 | CAC02COG101F100A |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A32C312 | 0160-5880 | 4 | 1 | CAPACITOR-FXD 2200PF +-1% 50VDC CER | 27167 | CAC03COG222F050A |
| A32C313 | 0160-5871 | 3 | 1 | CAPACITOR-FXD 510PF +-1% 100VDC CER | 27167 | CAC03COG511F100A |
| A32C314 | 0160-4807 | 3 | 1 | CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG330J100A |
| A32C315 | 0160-5873 | 5 | 1 | CAPACITOR-FXD 1500PF +-1% 50VDC CER | 27167 | CAC03COG152F050A |
| A32C316-C317 | 0180-0291 | 3 | 1 | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A32C318 | 0160-5863 | 3 | 1 | CAPACITOR-FXD 330PF +-1% 100VDC CER | U01025 | C124G331F1G5CA |
| A32C319 | 0160-4812 | 0 | 1 | CAPACITOR-FXD 220PF +-5% 100VDC CER | 27167 | CAC02COG221J100A |
| A32C320-C321 | 0180-0291 | 3 | 1 | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A32C322 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C323 | 0180-1794 | 3 | 1 | CAPACITOR-FXD 22UF+-10% 35VDC TA | 13606 | 150D226X9035R2-DYS |
| A32C324 | 0180-0291 | 3 | 1 | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A32C400 | 0160-4793 | 6 | 3 | CAPACITOR-FXD 6.8PF +-5% 100VDC CER | 27167 | CAC02COG68BD100A |
| A32C401 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C402 | 0160-4789 | 0 | 2 | CAPACITOR-FXD 15PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG150J100A |
| A32C403 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C404 | 0160-4447 | 7 | 1 | CAPACITOR-FXD 220PF +-10% 50VDC POLYP | 25088 | B33063-A1221-K |
| A32C405-C406 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C407 | 0160-4787 | 8 | 1 | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A32C408 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C409 | 0180-0309 | 4 | 1 | CAPACITOR-FXD 4.7UF+-20% 10VDC TA | 13606 | 150D475X0010A2-DYS |
| A32C410 | 0180-0291 | 3 | 1 | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A32C411 | 0160-4793 | 6 | 1 | CAPACITOR-FXD 6.8PF +-5% 100VDC CER | 27167 | CAC02COG68BD100A |
| A32C412-C416 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C417 | 0160-4793 | 6 | 1 | CAPACITOR-FXD 6.8PF +-5% 100VDC CER | 27167 | CAC02COG68BD100A |
| A32C418 | 0160-4825 | 5 | 1 | CAPACITOR-FXD 560PF +-5% 100VDC CER | 27167 | CAC03COG561J100A |
| A32C419-C420 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C500-C502 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C503 | 0180-0291 | 3 | 1 | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A32C504 | 0180-1794 | 3 | 1 | CAPACITOR-FXD 22UF+-10% 35VDC TA | 13606 | 150D226X9035R2-DYS |
| A32C505 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C506-C507 | 0180-0291 | 3 | 1 | CAPACITOR-FXD 1UF+-10% 35VDC TA | 13606 | 150D105X9035A2-DYS |
| A32C508 | 0180-0309 | 4 | 1 | CAPACITOR-FXD 4.7UF+-20% 10VDC TA | 13606 | 150D475X0010A2-DYS |
| A32C509 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C510 | 0180-1794 | 3 | 1 | CAPACITOR-FXD 22UF+-10% 35VDC TA | 13606 | 150D226X9035R2-DYS |
| A32C511 | 0160-4789 | 0 | 1 | CAPACITOR-FXD 15PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG150J100A |
| A32C512-C514 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C600-C602 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C603 | 0160-4808 | 4 | 1 | CAPACITOR-FXD 470PF +-5% 100VDC CER | 27167 | CAC02COG471J100A |
| A32C604 | 0180-0197 | 8 | 1 | CAPACITOR-FXD 2.2UF+-10% 20VDC TA | 13606 | 150D225X9020A2-DYS |
| A32C605-C608 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A32C609 | 0160-4822 | 2 | 1 | CAPACITOR-FXD 1000PF +-5% 100VDC CER | 27167 | CAC03COG102J100A |
| A32CR100 | 1901-0050 | 3 | 4 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A32CR200 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A32CR201 | 1902-0686 | 3 | 1 | DIODE-ZNR 6.2V 2% DO-7 PD=.4W TC=+.002% | 04713 | SZ 12170 |
| A32CR400-CR401 | 1901-0050 | 3 | 1 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A32CR402 | 1902-0952 | 6 | 1 | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A32CR403-CR404 | 1901-0518 | 8 | 1 | DIODE-SCHOTTKY SM SIG | 28480 | 1901-0518 |
| A32CR405-CR407 | 1901-0040 | 1 | 5 | DIODE-SWITCHING 30V 50MA 2NS DO-35 | 07263 | FDH1088 |
| A32CR500-CR501 | 1901-0040 | 1 | 1 | DIODE-SWITCHING 30V 50MA 2NS DO-35 | 07263 | FDH1088 |
| A32J300 | 1251-4822 | 6 | 1 | CONN-POST TYPE .100-PIN-SPCG 3-CONT | 27264 | 22-03-2031 |
| A32L400 | 1251-7629 | 7 | 1 | CONN-POST TYPE .100-PIN-SPCG 40-CONT | 00779 | 532955-7 |
| A32L300 | 03561-60302 | 1 | 1 | L-2304UH 1% | 28480 | 03561-60302 |
| A32L301 | 03561-60301 | 0 | 1 | L-2035UH 1% | 28480 | 03561-60301 |
| A32L302 | 03561-60303 | 2 | 1 | L-1834UH 1% | 28480 | 03561-60303 |
| A32L303 | 03561-60301 | 0 | 2 | L-2035UH 1% | 28480 | 03561-60301 |
| A32L500-L501 | 9140-0029 | 0 | 1 | INDUCTOR RF-CH-MLD 100UH 10% .25DX.313LG | 99484 | 3100-12-101 |
| A32L502 | 9140-0748 | 0 | 1 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A32MP688 | 0340-0564 | 3 | 1 | INSULATOR-XSTR THRM-CNDCT | 55285 | 7403-09FR-51 |
| A32Q400 | 1855-0269 | 7 | 1 | TRANSISTOR MOSFET N-CHAN E-MODE TO-72 SI | S01041 | SD214 |
| A32R100 | 0757-0280 | 3 | 17 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R101 | 0698-6360 | 6 | 1 | RESISTOR 10K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R102 | 0698-7847 | 6 | 1 | RESISTOR 1.111K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R103 | 0757-0401 | 0 | 3 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R104 | 0698-6624 | 5 | 7 | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R105 | 0698-6362 | 8 | 5 | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R106 | 0698-6624 | 5 | 1 | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R107 | 0698-6362 | 8 | 1 | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R108 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|--------|-----|---|----------|-----------------|
| A32R111 | 0757-0346 | 2 | 10 | RESISTOR 10 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R112 | 0757-0460 | 1 | 1 | RESISTOR 61.9K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R200 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R201 | 0698-3279 | 0 | 2 | RESISTOR 4.99K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R202 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R203 | 0757-0346 | 2 | | RESISTOR 10 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R204 | 0698-4205 | 4 | 1 | RESISTOR 21K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R205 | 0757-0274 | 5 | 3 | RESISTOR 1.21K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R206 | 0757-0442 | 9 | 2 | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R207 | 0698-3279 | 0 | | RESISTOR 4.99K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R208 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R300 | 8150-3375 | 5 | 2 | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A32R301 | 0698-4500 | 2 | 1 | RESISTOR 57.6K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R302 | 0698-8629 | 4 | 1 | RESISTOR 1.69K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R303 | 0698-6362 | 8 | | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R304 | 0698-6624 | 5 | | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R305 | 0698-6362 | 8 | | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R306 | 0698-6624 | 5 | | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R307 | 0698-6362 | 8 | | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R308-R311 | 0757-0346 | 2 | | RESISTOR 10 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R312 | 0757-0403 | 2 | 1 | RESISTOR 121 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R313-R316 | 0757-0346 | 2 | | RESISTOR 10 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R317 | 0757-1094 | 9 | 2 | RESISTOR 1.47K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R318 | 0698-3161 | 9 | 2 | RESISTOR 38.3K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R400 | 2100-3354 | 9 | 1 | RESISTOR-TRMR 50K 10% C SIDE-ADJ 1-TRN | 73138 | 72XR50K-149B |
| A32R401 | 2100-3207 | 1 | 1 | RESISTOR-TRMR 5K 10% C SIDE-ADJ 1-TRN | 32997 | 3386X-Y46-502 |
| A32R402 | 0757-0274 | 5 | | RESISTOR 1.21K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R403 | 8150-3375 | 5 | | RESISTOR-ZERO OHMS 22 AWG LEAD DIA | 75042 | ZEROHM |
| A32R404 | 0698-6320 | 8 | 1 | RESISTOR 5K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A32R405 | 0698-6627 | 8 | 1 | RESISTOR 25K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R406 | 0698-6624 | 5 | | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R407 | 0698-3162 | 0 | 1 | RESISTOR 46.4K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R408 | 2100-3054 | 6 | 1 | RESISTOR-TRMR 50K 10% C SIDE-ADJ 17-TRN | 73138 | 89PR50K |
| A32R409 | 0698-6377 | 5 | 1 | RESISTOR 200 .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A32R410 | 0698-4412 | 5 | 1 | RESISTOR 143 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R411 | 0698-3161 | 9 | | RESISTOR 38.3K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R412 | 0757-1094 | 9 | | RESISTOR 1.47K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R413 | 0698-6624 | 5 | | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R414 | 0757-0467 | 8 | 1 | RESISTOR 121K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R415 | 0757-0442 | 9 | | RESISTOR 10K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R416 | 0698-3445 | 2 | 1 | RESISTOR 348 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R417-R418 | 0698-6361 | 7 | 3 | RESISTOR 8K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R419 | 0698-4503 | 5 | 1 | RESISTOR 66.5K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R420 | 0699-0690 | 5 | 1 | RESISTOR 302 .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R421 | 0757-0459 | 8 | 1 | RESISTOR 56.2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R422 | 2100-3502 | 9 | 1 | RESISTOR-TRMR 200 10% C TOP-ADJ 17-TRN | 73138 | 67WR200 |
| A32R423 | 0698-3156 | 2 | 1 | RESISTOR 14.7K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R424 | 0757-0274 | 5 | | RESISTOR 1.21K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R425 | 0757-0290 | 5 | 1 | RESISTOR 6.19K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R426 | 0698-3444 | 1 | 1 | RESISTOR 316 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R427 | 0698-8959 | 3 | 1 | RESISTOR 619K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R428 | 0757-0462 | 3 | 1 | RESISTOR 75K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R429 | 0698-6366 | 2 | 1 | RESISTOR 800 .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R430 | 0757-0472 | 5 | 1 | RESISTOR 200K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R431 | 03562-62501 | 7 | | COMPONENT KIT | 28480 | 03562-62501 |
| A32R432 | 0757-0428 | 1 | 1 | RESISTOR 1.62K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R433 | 0757-0443 | 0 | 1 | RESISTOR 11K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R434 | 0698-6624 | 5 | | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R435 | 0699-0842 | 9 | 1 | RESISTOR 6.19K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R436 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R437 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R438 | 0698-7394 | 8 | 1 | RESISTOR 698 .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R439 | 0698-6361 | 7 | | RESISTOR 8K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A32R500-R501 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R502-R503 | 0698-3454 | 3 | 2 | RESISTOR 215K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R504 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R505 | 0757-0482 | 7 | 1 | RESISTOR 511K 1% .125W F TC=0+-100 | 19701 | 5033R |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A32R506 | 0698-4429 | 4 | 1 | RESISTOR 1.87K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R507 | 0698-4471 | 6 | 1 | RESISTOR 7.15K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R508 | 0683-0475 | 1 | 1 | RESISTOR 4.7 5% .25W CF TC=0-400 | 77902 | R-25J |
| A32R509 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R510 | 0757-0273 | 4 | 1 | RESISTOR 3.01K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R511 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R512 | 0757-0416 | 7 | 1 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R513 | 0698-3266 | 5 | 1 | RESISTOR 237K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R514 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R516 | 0698-3202 | 9 | 1 | RESISTOR 1.74K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R511 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R512 | 0757-0416 | 7 | 1 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R513 | 0698-3266 | 5 | 1 | RESISTOR 237K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R514 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R516 | 0698-3202 | 9 | 1 | RESISTOR 1.74K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R517-R520 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R600-R602 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R604 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32RN100 | 1810-0523 | 2 | 2 | NETWORK-RES 14-DIP MULTI-VALUE | 7M605 | 1172 |
| A32RN200 | 1810-0523 | 2 | 2 | NETWORK-RES 14-DIP MULTI-VALUE | 7M605 | 1172 |
| A32T200 | 9100-2616 | 1 | 1 | TRANSFORMER-PULSE BIFILAR WOUND; 18.0 MM | 13606 | 9100-2616 |
| A32U100 | 1826-0581 | 5 | 2 | ANALOG MULTIPLEXER 8 CHNL 16 -CBRZ/SDR | 27014 | SL37506 |
| A32U101-U102 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A32U200 | 1826-0581 | 5 | 1 | ANALOG MULTIPLEXER 8 CHNL 16 -CBRZ/SDR | 27014 | SL37506 |
| A32U201 | 1820-1934 | 2 | 1 | D/A 8-BIT 16-CERDIP BPLR | 06665 | DAC-08 096Q |
| A32U202-U203 | 1820-3423 | 8 | 2 | IC SHF-RGTR TTL LS ASYNCHRO SERIAL-IN | 01295 | SN74LS595N |
| A32U300-U301 | 1826-0715 | 5 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A32U400 | 1826-0445 | 7 | 1 | IC V RGLTR-FXD-NEG 4.8/5.2V TO-220 PKG | 07263 | SL26583 |
| A32U401-U402 | 1826-0109 | 3 | 1 | IC OP AMP WB TO-99 PKG | 34371 | HA2-2625 B3053-032 |
| A32U403 | 1826-1127 | 7 | 1 | IC PRNC DUAL 8-TO-99 PKG | 27014 | LF412CH |
| A32U404 | 1826-0528 | 0 | 1 | IC OP AMP LOW-BIAS-H-IMPED TO-99 PKG | 27014 | SL35806 |
| A32U405 | 1826-0501 | 9 | 1 | ANALOG MULTIPLEXER 6 CHNL 16 -DIP-P | 04713 | SC45297PK |
| A32U406 | 1826-0109 | 3 | 1 | IC OP AMP WB TO-99 PKG | 34371 | HA2-2625 B3053-032 |
| A32U500 | 1826-0175 | 3 | 2 | IC COMPARATOR GP DUAL 14-DIP-P PKG | 27014 | SL26763 |
| A32U501 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A32U502 | 1826-0175 | 3 | 1 | IC COMPARATOR GP DUAL 14-DIP-P PKG | 27014 | SL26763 |
| A32U503 | 1820-2656 | 7 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A32U504 | 1820-0471 | 0 | 1 | IC INV TTL HEX 1-INP | 01295 | SN19235 |
| A32U505 | 1820-1645 | 2 | 1 | IC BFR TTL LS BUS QUAD | 01295 | SN57686N |
| A32U600 | 03562-62501 | 7 | 1 | COMPONENT KIT | 28480 | 03562-62501 |
| A32U600 | 1826-1110 | 8 | 1 | D/A 16-BIT 24-DIP-C BPLR | 8E175 | DACT02KH/2D330 |
| A32U601 | 1826-1112 | 0 | 1 | A/D 8-1/2-BIT 18-DIP-C BPLR | T01085 | TD1001J8C |
| A32U602 | 1820-3441 | 0 | 1 | IC GATE-ARY CMOS | 50167 | MB63H301P |
| A32U603 | 1820-3423 | 8 | 1 | IC SHF-RGTR TTL LS ASYNCHRO SERIAL-IN | 01295 | SN74LS595N |
| A32U604 | 1820-2711 | 5 | 1 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN71504N |
| A32U605 | 1820-2488 | 3 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A32U606 | 1820-2696 | 5 | 1 | IC FF TTL F D-TYPE POS-EDGE-TRIG COM CLK | 07263 | SL82690 |
| A32U607 | 1820-1074 | 1 | 1 | IC DRVR TTL NOR QUAD 2-INP | 01295 | SN43266 |
| A32U608 | 1820-0697 | 2 | 1 | IC DRVR TTL S NAND LINE DUAL 4-INP | 01295 | SN24665 |
| | 1251-0600 | 0 | 49 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| | 2190-0004 | 9 | 1 | WASHER-LK INTL T NO. 4 .115-IN-ID | T12345 | SF 1904-00 |
| | 2200-0103 | 2 | 1 | SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI | 83486 | 2200-0103 |
| | 5000-9043 | 6 | 1 | PIN EXTR | 28480 | 5000-9043 |
| | 2260-0001 | 5 | 1 | NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK | T1234 | 2260-0001 |
| | 1258-0141 | 8 | 1 | JMPR-REM .025P | 22526 | 65474-004 |
| | 1250-1339 | 2 | 1 | CONNECTOR-RF SM-SLD M PC 50-OHM | 98291 | 52-051-0000 |
| A33, A35 | 03562-66533 | 3 | 2 | PC BOARD-INPUT | 28480 | 03562-66533 |
| A33C100 | 0160-3440 | 8 | 1 | CAPACITOR-FXD .39UF +-5% 200VDC | 84411 | HEW-249 |
| A33C101 | 0160-4796 | 9 | 4 | CAPACITOR-FXD 3.9PF +- .25PF 100VDC CER | 27167 | CAC02COG3R9C100A |
| A33C102 | 0121-0556 | 9 | 4 | C-V .6-6PF 50V AIR | 18736 | V5027 |
| A33C103 | 0160-4796 | 9 | 1 | CAPACITOR-FXD 3.9PF +- .25PF 100VDC CER | 27167 | CAC02COG3R9C100A |
| A33C104 | 0160-2207 | 3 | 1 | CAPACITOR-FXD 300PF +-5% 300VDC MICA | 00853 | 0160-2207 |
| A33C105 | 0160-4798 | 1 | 2 | CAPACITOR-FXD 2.7PF +- .25PF 100VDC CER | 27167 | CAC02COG2R7C100A |
| A33C106 | 0121-0556 | 9 | 1 | C-V .6-6PF 50V AIR | 18736 | V5027 |
| A33C107 | 0160-4787 | 8 | 4 | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A33C108 | 0160-4571 | 16 | 16 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C109 | 0180-0210 | 8 | 4 | CAPACITOR-FXD 3.3UF+-20% 15VDC TA | 13606 | 150D335X0015A2-DYS |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A33C110 | 0180-0210 | 6 | | CAPACITOR-FXD 3.3UF+-20% 15VDC TA | 13606 | 150D335X0015A2-DYS |
| A33C111-C112 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C113 | 0160-4786 | 7 | 2 | CAPACITOR-FXD 27PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG270J100A |
| A33C200 | 0160-3440 | 8 | | CAPACITOR-FXD .39UF +-5% 200VDC | 84411 | HEW-249 |
| A33C201 | 0160-4796 | 9 | | CAPACITOR-FXD 3.9PF +--.25PF 100VDC CER | 27167 | CAC02COG3R9C100A |
| A33C202 | 0121-0556 | 9 | | C-V .6-6PF 50V AIR | 18736 | V5027 |
| A33C203 | 0160-4796 | 9 | | CAPACITOR-FXD 3.9PF +--.25PF 100VDC CER | 27167 | CAC02COG3R9C100A |
| A33C204 | 0160-2207 | 3 | | CAPACITOR-FXD 300PF +-5% 300VDC MICA | 00853 | 0160-2207 |
| A33C205 | 0160-4798 | 1 | | CAPACITOR-FXD 2.7PF +--.25PF 100VDC CER | 27167 | CAC02COG2R7C100A |
| A33C206 | 0121-0556 | 9 | | C-V .6-6PF 50V AIR | 18736 | V5027 |
| A33C207 | 0160-4787 | 8 | | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A33C208 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C209-C210 | 0180-0210 | 6 | | CAPACITOR-FXD 3.3UF+-20% 15VDC TA | 13606 | 150D335X0015A2-DYS |
| A33C211-C212 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C213 | 0160-4786 | 7 | | CAPACITOR-FXD 27PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG270J100A |
| A33C400-C403 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C504 | 0160-4787 | 8 | | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A33C505 | 0160-4792 | 5 | 1 | CAPACITOR-FXD 8.2PF +--.5PF 100VDC CER | 27167 | CAC02COG8R2D100A |
| A33C506 | 0160-4791 | 4 | 1 | CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG100J100A |
| A33C508 | 0160-4806 | 2 | 1 | CAPACITOR-FXD 39PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG390J100A |
| A33C509-C510 | 0160-4787 | 8 | | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A33C600 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C601 | 0180-1731 | 8 | 1 | CAPACITOR-FXD 4.7UF+-10% 50VDC TA | 13606 | 150D475X9050B2-DYS |
| A33C602 | 0180-2207 | 5 | 1 | CAPACITOR-FXD 100UF+-10% 10VDC TA | 13606 | 150D107X9010R2-DYS |
| A33C603 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C604 | 0180-1731 | 8 | | CAPACITOR-FXD 4.7UF+-10% 50VDC TA | 13606 | 150D475X9050B2-DYS |
| A33C605 | 0180-0097 | 7 | 1 | CAPACITOR-FXD 47UF+-10% 35VDC TA | 13606 | 150D476X9035S2-DYS |
| A33C606-C607 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C608 | 0180-0097 | 7 | | CAPACITOR-FXD 47UF+-10% 35VDC TA | 13606 | 150D476X9035S2-DYS |
| A33C609 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C610 | 0180-1794 | 3 | 1 | CAPACITOR-FXD 22UF+-10% 35VDC TA | 13606 | 150D226X9035R2-DYS |
| A33C611-C612 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33CR100 | 1902-0654 | 5 | 4 | DIODE-ZNR 33V 5% PD=1W IR=5UA | 04713 | SZ40145-025 |
| A33CR101 | 1901-0050 | 3 | 8 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR102-CR103 | 1901-0579 | 1 | 4 | DIODE-SWITCHING 40V 20MA 300NS DO-7 | 07263 | FJT1100 |
| A33CR104 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR105 | 1902-0654 | 5 | | DIODE-ZNR 33V 5% PD=1W IR=5UA | 04713 | SZ40145-025 |
| A33CR106 | 1902-0952 | 6 | 1 | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A33CR107 | 1901-0527 | 9 | 3 | DIODE-CUR RGLTR 75V DO-7 | 04713 | SCL-040 |
| A33CR108 | 1902-0952 | 6 | | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A33CR109 | 1901-0527 | 9 | 1 | DIODE-CUR RGLTR 75V DO-7 | 04713 | SCL-040 |
| A33CR200 | 1902-0654 | 5 | | DIODE-ZNR 33V 5% PD=1W IR=5UA | 04713 | SZ40145-025 |
| A33CR201 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR202-CR203 | 1901-0579 | 1 | | DIODE-SWITCHING 40V 20MA 300NS DO-7 | 07263 | FJT1100 |
| A33CR204 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR205 | 1902-0654 | 5 | | DIODE-ZNR 33V 5% PD=1W IR=5UA | 04713 | SZ40145-025 |
| A33CR206 | 1902-0952 | 6 | | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A33CR207 | 1901-0527 | 9 | | DIODE-CUR RGLTR 75V DO-7 | 04713 | SCL-040 |
| A33CR208 | 1902-0952 | 6 | | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A33CR209 | 1901-0527 | 9 | | DIODE-CUR RGLTR 75V DO-7 | 04713 | SCL-040 |
| A33CR300 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR400 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR600-CR601 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33J300 | 1251-5971 | 8 | 1 | CONN-POST TYPE 2.5-PIN-SPCG 3-CONT | 27264 | 22-12-1032 |
| A33J400 | 1250-1339 | 2 | | CONNECTOR-RF SM-SLD M PC 50-OHM | 98291 | 52-051-0000 |
| A33J701 | 1251-7755 | 0 | 1 | CONN-POST TYPE .100-PIN-SPCG 30-CONT | 00779 | 532955-5 |
| A33K100-K109 | 0490-1403 | 8 | | RELAY-REED 1A 500MA 200VDC 5VDC-COIL | 71707 | 2900-0022 |
| A33K200-K209 | 0490-1403 | 8 | | RELAY-REED 1A 500MA 200VDC 5VDC-COIL | 71707 | 2900-0022 |
| A33L600-L602 | 9140-0748 | 0 | 1 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A33L603-L604 | 9140-0029 | 0 | 1 | INDUCTOR RF-CH-MLD 100UH 10% .25DX.313LG | 99484 | 3100-12-101 |
| A33L605 | 9140-0748 | 0 | 1 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A33MP678 | 03562-04109 | 9 | 1 | COVER-SHIELD | 28480 | 03562-04109 |
| A33MP679 | 03562-04110 | 2 | 1 | COVER-SHIELD | 28480 | 03562-04110 |
| A33MP680-MP681 | 03577-20601 | 7 | 2 | SHLD-CIRC SIDE | 28480 | 03562-20601 |
| A33MP682-MP683 | 03577-20602 | 8 | 1 | SHLD-COMP SIDE | 28480 | 03562-20602 |
| A33Q100-Q101 | 1855-0460 | 0 | 1 | TRANSISTOR J-FET N-CHAN | 27014 | 1855-0460 |
| A33Q102 | 1853-0037 | 3 | 1 | TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ | 04713 | SS 2109 |
| A33Q103-Q104 | 1854-0022 | 8 | 1 | TRANSISTOR NPN SI TO-39 PD=700MW | 07263 | S17843 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|--------|-----|--|----------|--------------------|
| A32R506 | 0698-4429 | 4 | 1 | RESISTOR 1.87K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R507 | 0698-4471 | 6 | 1 | RESISTOR 7.15K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A32R508 | 0683-0475 | 1 | 1 | RESISTOR 4.7 5% .25W CF TC=0-400 | 77902 | R-25J |
| A32R509 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R510 | 0757-0273 | 4 | 1 | RESISTOR 3.01K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R511 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R512 | 0757-0416 | 7 | 1 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R513 | 0698-3266 | 5 | 1 | RESISTOR 237K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R514 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R516 | 0698-3202 | 9 | 1 | RESISTOR 1.74K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R511 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R512 | 0757-0416 | 7 | 1 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R513 | 0698-3266 | 5 | 1 | RESISTOR 237K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R514 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R516 | 0698-3202 | 9 | 1 | RESISTOR 1.74K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R517-R520 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R600-R602 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32R604 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A32RN100 | 1810-0523 | 2 | 2 | NETWORK-RES 14-DIP MULTI-VALUE | 7M605 | 1172 |
| A32RN200 | 1810-0523 | 2 | 2 | NETWORK-RES 14-DIP MULTI-VALUE | 7M605 | 1172 |
| A32T200 | 9100-2616 | 1 | 1 | TRANSFORMER-PULSE BIFILAR WOUND; 18.0 MM | 13606 | 9100-2616 |
| A32U100 | 1826-0581 | 5 | 2 | ANALOG MULTIPLEXER 8 CHNL 16 -CBRZ/SDR | 27014 | SL37506 |
| A32U101-U102 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A32U200 | 1826-0581 | 5 | 1 | ANALOG MULTIPLEXER 8 CHNL 16 -CBRZ/SDR | 27014 | SL37506 |
| A32U201 | 1820-1934 | 2 | 1 | D/A 8-BIT 16-CERDIP BPLR | 06665 | DAC-08 096Q |
| A32U202-U203 | 1820-3423 | 8 | 2 | IC SHF-RGTR TTL LS ASYNCHRO SERIAL-IN | 01295 | SN74LS595N |
| A32U300-U301 | 1826-0715 | 7 | 5 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A32U400 | 1826-0445 | 0 | 1 | IC V RGLTR-FXD-NEG 4.8/5.2V TO-220 PKG | 07263 | SL26583 |
| A32U401-U402 | 1826-0109 | 3 | 1 | IC OP AMP WB TO-99 PKG | 34371 | HA2-2625 B3053-032 |
| A32U403 | 1826-1127 | 7 | 1 | IC PRCN DUAL 8-TO-99 PKG | 27014 | LF412CH |
| A32U404 | 1826-0528 | 0 | 1 | IC OP AMP LOW-BIAS-H-IMPD TO-99 PKG | 27014 | SL35806 |
| A32U405 | 1826-0501 | 9 | 1 | ANALOG MULTIPLEXER 6 CHNL 16 -DIP-P | 04713 | SC45297PK |
| A32U406 | 1826-0109 | 3 | 1 | IC OP AMP WB TO-99 PKG | 34371 | HA2-2625 B3053-032 |
| A32U500 | 1826-0175 | 3 | 2 | IC COMPARTOR GP DUAL 14-DIP-P PKG | 27014 | SL26763 |
| A32U501 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A32U502 | 1826-0175 | 3 | 1 | IC COMPARTOR GP DUAL 14-DIP-P PKG | 27014 | SL26763 |
| A32U503 | 1820-2656 | 7 | 1 | IC GATE TTL ALS NAND QUAD 2-INP | 01295 | SN71338N |
| A32U504 | 1820-0471 | 0 | 1 | IC INV TTL HEX 1-INP | 01295 | SN19235 |
| A32U505 | 1820-1645 | 2 | 1 | IC BFR TTL LS BUS QUAD | 01295 | SN57686N |
| A32U600 | 03562-62501 | 7 | 1 | COMPONENT KIT | 28480 | 03562-62501 |
| A32U600 | 1826-1110 | 8 | 1 | D/A 16-BIT 24-DIP-C BPLR | 8E175 | DAC702KH/2D330 |
| A32U601 | 1826-1112 | 0 | 1 | A/D 8-1/2-BIT 18-DIP-C BPLR | T01085 | ADC1001J8C |
| A32U602 | 1820-3441 | 0 | 1 | IC GATE-ARY CMOS | S0167 | MB63H301P |
| A32U603 | 1820-3423 | 8 | 1 | IC SHF-RGTR TTL LS ASYNCHRO SERIAL-IN | 01295 | SN74LS595N |
| A32U604 | 1820-2711 | 5 | 1 | IC DRVYR TTL LS LINE DRVYR OCTL | 01295 | SN71504N |
| A32U605 | 1820-2488 | 3 | 1 | IC FF TTL ALS D-TYPE POS-EDGE-TRIG | 01295 | SN71171N |
| A32U606 | 1820-2696 | 5 | 1 | IC FF TTL F D-TYPE POS-EDGE-TRIG COM CLK | 07263 | SL82690 |
| A32U607 | 1820-1074 | 1 | 1 | IC DRVYR TTL NOR QUAD 2-INP | 01295 | SN43266 |
| A32U608 | 1820-0697 | 2 | 1 | IC DRVYR TTL S NAND LINE DUAL 4-INP | 01295 | SN24665 |
| | 1251-0600 | 0 | 49 | CONNECTOR-SGL CONT PIN 1.14-MM-BSC-SZ SQ | 27264 | 16-06-0034 |
| | 2190-0004 | 9 | 1 | WASHER-LK INTL T NO. 4 .115-IN-ID | T12345 | SF 1904-00 |
| | 2200-0103 | 2 | 1 | SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI | 83486 | 2200-0103 |
| | 5000-9043 | 6 | 1 | PIN EXTR | 28480 | 5000-9043 |
| | 2260-0001 | 5 | 1 | NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK | T1234 | 2260-0001 |
| | 1258-0141 | 8 | 1 | JMPR-REM .025P | 22526 | 65474-004 |
| | 1250-1339 | 2 | 1 | CONNECTOR-RF SM-SLD M PC 50-OHM | 98291 | 52-051-0000 |
| A33, A35 | 03562-66533 | 3 | 2 | PC BOARD-INPUT | 28480 | 03562-66533 |
| A33C100 | 0160-3440 | 8 | 1 | CAPACITOR-FXD .39UF +-5% 200VDC | 84411 | HEW-249 |
| A33C101 | 0160-4796 | 9 | 4 | CAPACITOR-FXD 3.9PF +- .25PF 100VDC CER | 27167 | CAC02COG3R9C100A |
| A33C102 | 0121-0556 | 9 | 4 | C-V .6-6PF 50V AIR | 18736 | V5027 |
| A33C103 | 0160-4796 | 9 | 1 | CAPACITOR-FXD 3.9PF +- .25PF 100VDC CER | 27167 | CAC02COG3R9C100A |
| A33C104 | 0160-2207 | 3 | 1 | CAPACITOR-FXD 300PF +-5% 300VDC MICA | 00853 | 0160-2207 |
| A33C105 | 0160-4798 | 1 | 2 | CAPACITOR-FXD 2.7PF +- .25PF 100VDC CER | 27167 | CAC02COG2R7C100A |
| A33C106 | 0121-0556 | 9 | 1 | C-V .6-6PF 50V AIR | 18736 | V5027 |
| A33C107 | 0160-4787 | 8 | 4 | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A33C108 | 0160-4571 | 16 | 16 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C109 | 0180-0210 | 8 | 4 | CAPACITOR-FXD 3.3UF+-20% 15VDC TA | 13606 | 150D335X0015A2-DYS |

See introduction to this section for ordering information
*Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| A33C110 | 0180-0210 | 6 | | CAPACITOR-FXD 3.3UF+-20% 15VDC TA | 13606 | 150D335X0015A2-DYS |
| A33C111-C112 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C113 | 0160-4786 | 7 | 2 | CAPACITOR-FXD 27PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG270J100A |
| A33C200 | 0160-3440 | 8 | | CAPACITOR-FXD .39UF +-5% 200VDC | 84411 | HEW-249 |
| A33C201 | 0160-4796 | 9 | | CAPACITOR-FXD 3.9PF +--.25PF 100VDC CER | 27167 | CAC02COG39C100A |
| A33C202 | 0121-0556 | 9 | | C-V .6-6PF 50V AIR | 18736 | V5027 |
| A33C203 | 0160-4796 | 9 | | CAPACITOR-FXD 3.9PF +--.25PF 100VDC CER | 27167 | CAC02COG39C100A |
| A33C204 | 0160-2207 | 3 | | CAPACITOR-FXD 300PF +-5% 300VDC MICA | 00853 | 0160-2207 |
| A33C205 | 0160-4798 | 1 | | CAPACITOR-FXD 2.7PF +--.25PF 100VDC CER | 27167 | CAC02COG27C100A |
| A33C206 | 0121-0556 | 9 | | C-V .6-6PF 50V AIR | 18736 | V5027 |
| A33C207 | 0160-4787 | 8 | | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A33C208 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C209-C210 | 0180-0210 | 6 | | CAPACITOR-FXD 3.3UF+-20% 15VDC TA | 13606 | 150D335X0015A2-DYS |
| A33C211-C212 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C213 | 0160-4786 | 7 | | CAPACITOR-FXD 27PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG270J100A |
| A33C400-C403 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C504 | 0160-4787 | 8 | | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A33C505 | 0160-4792 | 5 | 1 | CAPACITOR-FXD 8.2PF +--.5PF 100VDC CER | 27167 | CAC02COG8R2D100A |
| A33C506 | 0160-4791 | 4 | 1 | CAPACITOR-FXD 10PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG100J100A |
| A33C508 | 0160-4806 | 2 | 1 | CAPACITOR-FXD 39PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG390J100A |
| A33C509-C510 | 0160-4787 | 8 | | CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30 | 27167 | CAC02COG220J100A |
| A33C600 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C601 | 0180-1731 | 8 | 1 | CAPACITOR-FXD 4.7UF+-10% 50VDC TA | 13606 | 150D475X9050B2-DYS |
| A33C602 | 0180-2207 | 5 | 1 | CAPACITOR-FXD 100UF+-10% 10VDC TA | 13606 | 150D107X9010R2-DYS |
| A33C603 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C604 | 0180-1731 | 8 | | CAPACITOR-FXD 4.7UF+-10% 50VDC TA | 13606 | 150D475X9050B2-DYS |
| A33C605 | 0180-0097 | 7 | 1 | CAPACITOR-FXD 47UF+-10% 35VDC TA | 13606 | 150D476X9035S2-DYS |
| A33C606-C607 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C608 | 0180-0097 | 7 | | CAPACITOR-FXD 47UF+-10% 35VDC TA | 13606 | 150D476X9035S2-DYS |
| A33C609 | 0160-4571 | 8 | 1 | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33C610 | 0180-1794 | 3 | 1 | CAPACITOR-FXD 22UF+-10% 35VDC TA | 13606 | 150D226X9035R2-DYS |
| A33C611-C612 | 0160-4571 | 8 | | CAPACITOR-FXD .1UF +80-20% 50VDC CER | 04222 | SA205E104ZAA |
| A33CR100 | 1902-0654 | 5 | 4 | DIODE-ZNR 33V 5% PD=1W IR=5UA | 04713 | SZ40145-025 |
| A33CR101 | 1901-0050 | 3 | 8 | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR102-CR103 | 1901-0579 | 1 | 4 | DIODE-SWITCHING 40V 20MA 300NS DO-7 | 07263 | FJT1100 |
| A33CR104 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR105 | 1902-0654 | 5 | | DIODE-ZNR 33V 5% PD=1W IR=5UA | 04713 | SZ40145-025 |
| A33CR106 | 1902-0952 | 6 | 1 | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A33CR107 | 1901-0527 | 9 | 3 | DIODE-CUR RGLTR 75V DO-7 | 04713 | SCL-040 |
| A33CR108 | 1902-0952 | 6 | | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A33CR109 | 1901-0527 | 9 | 1 | DIODE-CUR RGLTR 75V DO-7 | 04713 | SCL-040 |
| A33CR200 | 1902-0654 | 5 | | DIODE-ZNR 33V 5% PD=1W IR=5UA | 04713 | SZ40145-025 |
| A33CR201 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR202-CR203 | 1901-0579 | 1 | | DIODE-SWITCHING 40V 20MA 300NS DO-7 | 07263 | FJT1100 |
| A33CR204 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR205 | 1902-0654 | 5 | | DIODE-ZNR 33V 5% PD=1W IR=5UA | 04713 | SZ40145-025 |
| A33CR206 | 1902-0952 | 6 | | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A33CR207 | 1901-0527 | 9 | | DIODE-CUR RGLTR 75V DO-7 | 04713 | SCL-040 |
| A33CR208 | 1902-0952 | 6 | | DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046% | 04713 | SZ30035-010 |
| A33CR209 | 1901-0527 | 9 | | DIODE-CUR RGLTR 75V DO-7 | 04713 | SCL-040 |
| A33CR300 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR400 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33CR600-CR601 | 1901-0050 | 3 | | DIODE-SWITCHING 80V 200MA 2NS DO-35 | 07263 | FDH 6308 |
| A33J300 | 1251-5971 | 8 | 1 | CONN-POST TYPE 2.5-PIN-SPCG 3-CONT | 27264 | 22-12-1032 |
| A33J400 | 1250-1339 | 2 | | CONNECTOR-RF SM-SLD M PC 50-OHM | 98291 | 52-051-0000 |
| A33J701 | 1251-7755 | 0 | 1 | CONN-POST TYPE .100-PIN-SPCG 30-CONT | 00779 | 532955-5 |
| A33K100-K109 | 0490-1403 | 8 | | RELAY-REED 1A 500MA 200VDC 5VDC-COIL | 71707 | 2900-0022 |
| A33K200-K209 | 0490-1403 | 8 | | RELAY-REED 1A 500MA 200VDC 5VDC-COIL | 71707 | 2900-0022 |
| A33L600-L602 | 9140-0748 | 0 | 1 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A33L603-L604 | 9140-0029 | 0 | 1 | INDUCTOR RF-CH-MLD 100UH 10% .25DX.313LG | 99484 | 3100-12-101 |
| A33L605 | 9140-0748 | 0 | 1 | INDUCTOR 250UH 25% .25DX.5LG Q=3 | 04213 | 1670-1 |
| A33MP678 | 03562-04109 | 9 | 1 | COVER-SHIELD | 28480 | 03562-04109 |
| A33MP679 | 03562-04110 | 2 | 1 | COVER-SHIELD | 28480 | 03562-04110 |
| A33MP680-MP681 | 03577-20601 | 7 | 2 | SHLD-CIRC SIDE | 28480 | 03562-20601 |
| A33MP682-MP683 | 03577-20602 | 8 | | SHLD-COMP SIDE | 28480 | 03562-20602 |
| A33Q100-Q101 | 1855-0460 | 0 | 1 | TRANSISTOR J-FET N-CHAN | 27014 | 1855-0460 |
| A33Q102 | 1853-0037 | 3 | 1 | TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ | 04713 | SS 2109 |
| A33Q103-Q104 | 1854-0022 | 8 | 1 | TRANSISTOR NPN SI TO-39 PD=700MW | 07263 | S17843 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|--------|-----|---|----------|-----------------------|
| A33Q105 | 1853-0037 | 3 | | TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ | 04713 | SS 2109 |
| A33Q200-Q201 | 1855-0460 | 0 | | TRANSISTOR J-FET N-CHAN | 27014 | 1855-0460 |
| A33Q202 | 1853-0037 | 3 | | TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ | 04713 | SS 2109 |
| A33Q203-Q204 | 1854-0022 | 8 | | TRANSISTOR NPN SI TO-39 PD=700MW | 07263 | S17843 |
| A33Q205 | 1853-0037 | 3 | | TRANSISTOR PNP SI TO-39 PD=1W FT=100MHZ | 04713 | SS 2109 |
| A33Q509 | 1855-0091 | 3 | 1 | TRANSISTOR J-FET N-CHAN D-MODE SI | 27014 | NS5141 |
| A33Q512-Q520 | 1855-0091 | 3 | | TRANSISTOR J-FET N-CHAN D-MODE SI | 27014 | NS5141 |
| A33R100 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R101 | 0698-6305 | 9 | 2 | RESISTOR 900K .1% .25W F TC=0+-25 | 19701 | 5043R |
| A33R102 | 0698-6979 | 3 | 2 | RESISTOR 111.1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R103 | 0698-6975 | 9 | 2 | RESISTOR 10.1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R104 | 0698-6306 | 0 | 2 | RESISTOR 990K .1% .25W F TC=0+-25 | 19701 | 5043R |
| A33R106 | 0698-7332 | 4 | 1 | RESISTOR 1M 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R107 | 0757-0123 | 3 | 4 | RESISTOR 34.8K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R108-R109 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R110 | 0757-0123 | 3 | | RESISTOR 34.8K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R111 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R112 | 2100-3874 | 8 | 2 | RESISTOR-TRMR 5K 10% C TOP-ADJ 17-TRN | 32997 | 3299W-DM3-502 |
| A33R113 | 0757-0280 | 3 | 8 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R114 | 0757-0393 | 9 | 8 | RESISTOR 47.5 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R115 | 0698-3558 | 8 | 2 | RESISTOR 4.02K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R116 | 0757-0393 | 9 | | RESISTOR 47.5 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R117 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R118-R119 | 0757-0393 | 9 | | RESISTOR 47.5 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R120 | 0837-0315 | 5 | 1 | PTC RESISTOR | 75263 | RL3312-200-120-50-PTO |
| A33R200 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R201 | 0698-6305 | 9 | | RESISTOR 900K .1% .25W F TC=0+-25 | 19701 | 5043R |
| A33R202 | 0698-6979 | 3 | | RESISTOR 111.1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R203 | 0698-6975 | 9 | | RESISTOR 10.1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R204 | 0698-6306 | 0 | | RESISTOR 990K .1% .25W F TC=0+-25 | 19701 | 5043R |
| A33R206 | 0698-7332 | 4 | | RESISTOR 1M 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R207 | 0757-0123 | 3 | | RESISTOR 34.8K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R208-R209 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R210 | 0757-0123 | 3 | | RESISTOR 34.8K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R211 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R212 | 2100-3874 | 8 | | RESISTOR-TRMR 5K 10% C TOP-ADJ 17-TRN | 32997 | 3299W-DM3-502 |
| A33R213 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R214 | 0757-0393 | 9 | | RESISTOR 47.5 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R215 | 0698-3558 | 8 | | RESISTOR 4.02K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R216 | 0757-0393 | 9 | | RESISTOR 47.5 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R217 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R218 | 0757-0393 | 9 | | RESISTOR 47.5 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R219 | 0757-0393 | 9 | | RESISTOR 47.5 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R400 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R401 | 0698-6624 | 5 | 2 | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R402 | 0698-6362 | 8 | 3 | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R403 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R404 | 0698-6348 | 0 | 1 | RESISTOR 3K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R405 | 0757-0416 | 7 | 1 | RESISTOR 511 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R406 | 0698-3178 | 8 | 1 | RESISTOR 487 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R407 | 0698-6699 | 4 | 1 | RESISTOR 127 .25% .125W F TC=0+-50 | 19701 | 5033R |
| A33R408 | 0698-8634 | 1 | 1 | RESISTOR 1.05K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R409 | 0698-6624 | 5 | | RESISTOR 2K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R410 | 0698-6362 | 8 | | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R411 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R500 | 0698-6362 | 8 | | RESISTOR 1K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R501 | 0698-4463 | 6 | 1 | RESISTOR 845 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A33R503 | 0757-0401 | 0 | | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R504 | 0698-6320 | 8 | 4 | RESISTOR 5K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A33R505 | 0698-6320 | 8 | | RESISTOR 5K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A33R506 | 0698-6630 | 3 | 1 | RESISTOR 20K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R507 | 0698-3557 | 7 | 1 | RESISTOR 806 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R508 | 0698-6329 | 7 | 1 | RESISTOR 845 1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R509 | 0698-6322 | 0 | 1 | RESISTOR 4K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A33R510 | 0698-6361 | 7 | 1 | RESISTOR 8K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R511 | 0698-8046 | 9 | 1 | RESISTOR 16K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R512 | 0698-8047 | 0 | 1 | RESISTOR 32K .1% .125W F TC=0+-25 | 19701 | 5033R |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------|
| A33R513 | 0698-8049 | 2 | 1 | RESISTOR 64K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R514 | 0698-8053 | 8 | 1 | RESISTOR 128K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R515 | 0698-8050 | 5 | 1 | RESISTOR 256K .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R516 | 0699-0676 | 7 | 1 | RESISTOR 511K .1% .125W F TC=0+-50 | 19701 | 5033R |
| A33R517 | 0699-0730 | 4 | 1 | RESISTOR 1M .1% .125W F TC=0+-25 | 19701 | 5033R |
| A33R518 | 0698-3511 | 3 | 1 | RESISTOR 665 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R521 | 0698-6320 | 8 | 1 | RESISTOR 5K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A33R522 | 0757-0283 | 6 | 1 | RESISTOR 2K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R523 | 0757-0273 | 4 | 1 | RESISTOR 3.01K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R524 | 0698-6320 | 8 | 1 | RESISTOR 5K .1% .125W F TC=0+-25 | 91637 | CMF-55-1, T-9 |
| A33R525 | 0757-0401 | 0 | 4 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R526 | 0698-4528 | 4 | 3 | RESISTOR 210K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A33R527-R528 | 0757-0446 | 3 | 2 | RESISTOR 15K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R529 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R531-R532 | 0698-4528 | 4 | 1 | RESISTOR 210K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A33R533 | 0698-4487 | 4 | 1 | RESISTOR 25.5K 1% .125W F TC=0+-100 | 91637 | CMF-55-1, T-1 |
| A33R535 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R600 | 0757-0280 | 3 | 1 | RESISTOR 1K 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33R601 | 0757-0401 | 0 | 1 | RESISTOR 100 1% .125W F TC=0+-100 | 19701 | 5033R |
| A33RN300-RN301 | 1810-0231 | 9 | 2 | NETWORK-RES 8-SIP 2.2K OHM X 7 | 11236 | 750-81-R2.2K |
| A33RN500-RN501 | 1810-0371 | 8 | 2 | NETWORK-RES 8-SIP 100.0K OHM X 7 | 11236 | 750-81-R100K |
| A33U100 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A33U200 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A33U300-U301 | 1858-0047 | 5 | 2 | TRANSISTOR ARRAY 16-PIN PLSTC DIP | 13606 | ULN-2003A |
| A33U302-U303 | 1820-3423 | 8 | 3 | IC SHF-RGTR TTL LS ASYNCHRO SERIAL-IN | 01295 | SN74LS595N |
| A33U400 | 1826-0715 | 7 | 4 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A33U401 | 1826-0581 | 5 | 1 | ANALOG MULTIPLEXER 8 CHNL 16 -CBRZ/SDR | 27014 | SL37506 |
| A33U402 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A33U500-U501 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| A33U502 | 1820-1273 | 2 | 1 | IC BFR TTL LS NOR QUAD 2-INP | 01295 | SN53649 |
| A33U503-U505 | 1826-0138 | 8 | 1 | IC COMPARATOR GP QUAD 14-DIP-P PKG | 27014 | SL24958 |
| A33U506 | 1820-3423 | 8 | 1 | IC SHF-RGTR TTL LS ASYNCHRO SERIAL-IN | 01295 | SN74LS595N |
| A33U507 | 1826-0175 | 3 | 1 | IC COMPARATOR GP DUAL 14-DIP-P PKG | 27014 | SL26763 |
| A33U508 | 1826-0715 | 7 | 1 | IC OP AMP LOW-NOISE 8-DIP-P PKG | 18324 | CC3802 |
| | 0515-0411 | 0 | 8 | SCREW-MACH M3 X 0.5 22MM-LG PAN-HD | 16941 | 0515-0411 |
| | 5000-9043 | 6 | 1 | PIN EXTR | 28480 | 5000-9043 |
| | 9100-1788 | 6 | 1 | CORE-FERRITE CHOKE-WIDEBAND;IMP:>680 | 02114 | VK200 20/4B |
| A34 | SEE A32 | | | | | |
| A35 | SEE A33 | | | | | |
| DSPL | 1345A/C13/500 | 9 | 1 | DISPLAY/CABLE ASSEMBLY | 28480 | 1345A/C13/500 |
| MP100 | 03562-00201 | 4 | 1 | PANEL-FRONT | 22670 | 03562-00201 |
| MP101 | 03562-00202 | 5 | 1 | PANEL-FRONT SUB | 28480 | 03562-00202 |
| MP102 | 03562-20602 | 1 | 2 | NUT-BNC | 76854 | 03562-20602 |
| MP103 | 1250-0102 | 5 | 2 | CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM | 24931 | 28J3109-1 |
| MP104 | 1250-0698 | 4 | 2 | CONNECTOR-RF BNC FEM SGL-HOLE-FR | 90949 | 31-10 |
| MP105 | 1250-0083 | 1 | 3 | CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM | 90949 | 31-221-1020 |
| MP106 | 1510-0038 | 8 | 1 | BINDING POST ASSY SGL THD-STUD | L01005 | 1510-0038 |
| MP107 | 5041-0202 | 7 | 1 | HALF-CHWHT | 28480 | 5041-0202 |
| MP108 | 5061-8008 | 9 | 2 | CABLE ASSY, RPG | 28480 | 5061-8008 |
| | 1251-4182 | 1 | 4 | CONNECTOR-SGL CONT SKT .025-IN-BSC-SZ SQ | 22526 | 47565 |
| | 0960-0684 | 2 | 1 | RPG QDES-8831 | 28480 | 0960-0684 |
| | 1251-5043 | 5 | 1 | CONN-POST TYPE .100-PIN-SPCG CRP | 22526 | 65039-032 |
| MP109 | 0370-3069 | 2 | 2 | KNOB RPG 1 1/8" | 28480 | 0370-3069 |
| MP200 | 03562-00203 | 6 | 1 | PANEL-REAR | 28480 | 03562-00203 |
| MP201 | 3101-2299 | 2 | 5 | SWITCH-SL DPDT STD 5A 250VAC SLDR-LUG | D8351 | 4021.0512 |
| MP202 | 03562-01201 | 6 | 1 | BRACKET-FAN | 28480 | 03562-01201 |
| MP203 | 03562-34301 | 6 | 1 | SERIAL PLATE 3562A | 28480 | 03562-34301 |
| MP204 | 03562-04104 | 4 | 1 | SHIELD-NUT PLATE | 28480 | 03562-04104 |
| MP206 | 2110-0543 | 3 | 1 | FUSEHOLDER BODY EXTR PST; BAYONET; TND | H9027 | FEC031.1603 |
| MP207 | 2110-0545 | 5 | 1 | FUSEHOLDER CAP BAYONET; 6.3A, 250V MAX | H9027 | FEK031.1613 |
| MP208 | 3150-0218 | 4 | 1 | FILTER-AIR 32 STD MESH MET SCREEN | 28480 | 3150-0218 |
| MP209 | 3160-0408 | 5 | 1 | FAN-IBAX 90-CFM 19-28VDC | 82877 | MD24B2 |
| MP210 | 7120-4835 | 0 | 1 | LABEL-INFORMATION .75-IN-WD 2-IN-LG PPR | 35860 | 7120-4835 |
| MP211 | 7121-0270 | 1 | 1 | LABEL-INFORMATION .5-IN-WD 1-IN-LG MYLAR | 22670 | 7121-0270 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|---------------------------------------|----------|------------------|
| MP212 | 9135-0261 | 1 | 1 | LINE FILTER | 05245 | F3186 |
| MP213 | 03562-29301 | 5 | 1 | FILTER-DISPLAY | 22670 | 03562-29301 |
| MP214 | 03582-04104 | 8 | 1 | GUARD-FAN SW | 28480 | 03582-04104 |
| MP300 | 03562-00101 | 3 | 1 | GUSSET-CENTER | 28480 | 03562-00101 |
| MP301 | 03562-00102 | 4 | 1 | DECK-PWR SUPPLY | 28480 | 03562-00102 |
| MP303 | 03562-00103 | 5 | 1 | CARD CAGE-FRONT | 28480 | 03562-00103 |
| | 03562-00104 | 6 | 1 | CARD CAGE-CENTER | 28480 | 03562-00104 |
| | 0403-0510 | 3 | 6 | GUIDE-PC BOARD | 28480 | 0403-0510 |
| | 0403-0511 | 4 | 6 | GUIDE-PC BOARD | 28480 | 0403-0511 |
| | 0590-1380 | 2 | 5 | THD-INSR-STDF 6MM L | 46384 | S0S-M4-6 |
| MP304 | 03562-00105 | 7 | 1 | CARD CAGE-REAR | 28480 | 03562-00105 |
| MP305 | 03562-00106 | 8 | 1 | PLENUM-PWR SPLY | 28480 | 03562-00106 |
| MP306 | 03562-00603 | 0 | 2 | SHIELD-ANALOG, FRONT END | 28480 | 03562-00603 |
| MP307 | 03562-01204 | 9 | 1 | BRACKET-DISPLAY | 28480 | 03562-01204 |
| MP308 | 03562-04101 | 1 | 1 | PLATE-SIDE | 28480 | 03562-04101 |
| MP309 | 03562-04108 | 8 | 1 | COVER-SIDE DIG | 28480 | 03562-04108 |
| MP310 | 03562-48301 | 5 | 2 | CARD GUIDE | 28480 | 03562-48301 |
| MP311 | 03562-04111 | 3 | 1 | SHIELD-SIDE | 28480 | 03562-04111 |
| MP400 | 03562-00601 | 8 | 2 | SHIELD-INPUT | 28480 | 03562-00601 |
| | 0403-0510 | 3 | 1 | GUIDE-PC BOARD | 28480 | 0403-0510 |
| | 0403-0511 | 4 | 1 | GUIDE-PC BOARD | 28480 | 0403-0511 |
| MP401 | 03562-00602 | 9 | 2 | COVER SHIELD | 28480 | 03562-00602 |
| MP402 | 03562-01211 | 8 | 1 | BRACKET-FRONT | 28480 | 03562-01211 |
| MP404 | 03562-01207 | 2 | 1 | BRKT-CAP | 28480 | 03562-01207 |
| MP405 | 03562-01208 | 3 | 1 | BRKT-SWITCH, ON/OFF | 28480 | 03562-01208 |
| MP406 | 03562-04102 | 2 | 1 | COVER-TOP PLENUM | 28480 | 03562-04102 |
| MP407 | 03562-04103 | 3 | 1 | COVER-BOTTOM PLENUM | 28480 | 03562-04103 |
| MP408 | 03562-04104 | 4 | 2 | SHIELD-NUT PLATE | 28480 | 03562-04104 |
| MP409 | 03562-01209 | 4 | 1 | BRKT-LINE FILTER | 28480 | 03562-01209 |
| MP400 | 03562-04105 | 5 | 1 | MOTHER BOARD SHIELD | 28480 | 03562-04105 |
| MP501 | 03562-04106 | 6 | 1 | COVER-POWER SUPPLY | 28480 | 03562-04106 |
| MP502 | 03562-04107 | 7 | 1 | COVER-1345A DISPLAY | 28480 | 03562-04107 |
| MP503 | 03562-48306 | 0 | 1 | RETAINER, DIGITAL BOARD | 28480 | 03562-48306 |
| MP504 | 03562-01212 | 9 | 1 | RETAINER, ANALOG BOARD | 28480 | 03562-01212 |
| MP505 | 5001-0441 | 2 | 2 | TRIM-SIDE | 28480 | 5001-0441 |
| MP506 | 5040-7201 | 8 | 4 | FOOT | 28480 | 5040-7201 |
| MP507 | 5040-7202 | 9 | 1 | TRIM TOP | 28480 | 5040-7202 |
| MP509 | 5060-9805 | 4 | 2 | STRAP HANDLE | 28480 | 5060-9805 |
| MP510 | 5061-9436 | 9 | 1 | COVER, TOP | 28480 | 5061-9436 |
| MP511 | 5061-9448 | 3 | 1 | COVER, BOTTOM | 28480 | 5061-9448 |
| MP512 | 5060-9948 | 6 | 2 | SIDE COVER, PERFORATED | 28480 | 5060-9948 |
| MP513 | 8160-0360 | 3 | 4 | RFI ROUND STRIP STL MSH/SIL RBR SN-PL | C01185 | 02-0101-0053-05 |
| MP514 | 0890-0100 | 8 | 2 | TUBING-HS .093-D/.046-RCVD .02-WALL | 06090 | RNF-100-3/32-WHT |
| MP603 | 5040-7278 | 9 | 8 | KEY-CAP EXT | 28480 | 5040-7278 |
| MP603 | 5041-0376 | 6 | 8 | KEYCAP-BLANK | 28480 | 5041-0376 |
| MP604 | 5041-2099 | 4 | 1 | KEY-CAP PRESET | 28480 | 5041-2099 |
| MP605 | 5041-2738 | 8 | 1 | KEY-CAP LOCAL | 28480 | 5041-2738 |
| MP606 | 5041-2839 | 0 | 1 | KEY-CAP A | 28480 | 5041-2839 |
| MP607 | 5041-2840 | 3 | 1 | KEY-CAP B | 28480 | 5041-2840 |
| MP608 | 5041-2900 | 6 | 1 | KEY-CAP AVG | 28480 | 5041-2900 |
| MP609 | 5041-2909 | 5 | 1 | KEY-CAP BACK SPACE | 28480 | 5041-2909 |
| MP610 | 5041-2910 | 8 | 1 | KEY-CAP - | 28480 | 5041-2910 |
| MP611 | 5041-2911 | 9 | 1 | KEY-CAP - | 28480 | 5041-2911 |
| MP612 | 5041-2912 | 0 | 2 | KEY-CAP ARO UP/DN | 28480 | 5041-2912 |
| MP613 | 5041-2914 | 2 | 1 | KEY-CAP 2 | 28480 | 5041-2914 |
| MP614 | 5041-2915 | 3 | 1 | KEY-CAP 3 | 28480 | 5041-2915 |
| MP615 | 5041-2916 | 4 | 1 | KEY-CAP 4 | 28480 | 5041-2916 |
| MP616 | 5041-2917 | 5 | 1 | KEY-CAP 5 | 28480 | 5041-2917 |
| MP617 | 5041-2918 | 6 | 1 | KEY-CAP 6 | 28480 | 5041-2918 |
| MP618 | 5041-2919 | 7 | 1 | KEY-CAP 7 | 28480 | 5041-2919 |
| MP619 | 5041-2920 | 0 | 1 | KEY-CAP 8 | 28480 | 5041-2920 |
| MP620 | 5041-2921 | 1 | 1 | KEY-CAP 9 | 28480 | 5041-2921 |
| MP621 | 5041-2924 | 4 | 1 | KEY-CAP SCALE | 28480 | 5041-2924 |
| MP622 | 5041-2927 | 7 | 1 | KEY-CAP FREQ | 28480 | 5041-2927 |
| MP623 | 5041-2974 | 4 | 1 | KEY-CAP SINGLE | 28480 | 5041-2974 |
| MP624 | 5041-2988 | 0 | 1 | KEY-CAP MARKER VALVE | 28480 | 5041-2988 |
| MP625 | 5041-2989 | 1 | 1 | KEY-CAP O NO | 28480 | 5041-2989 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

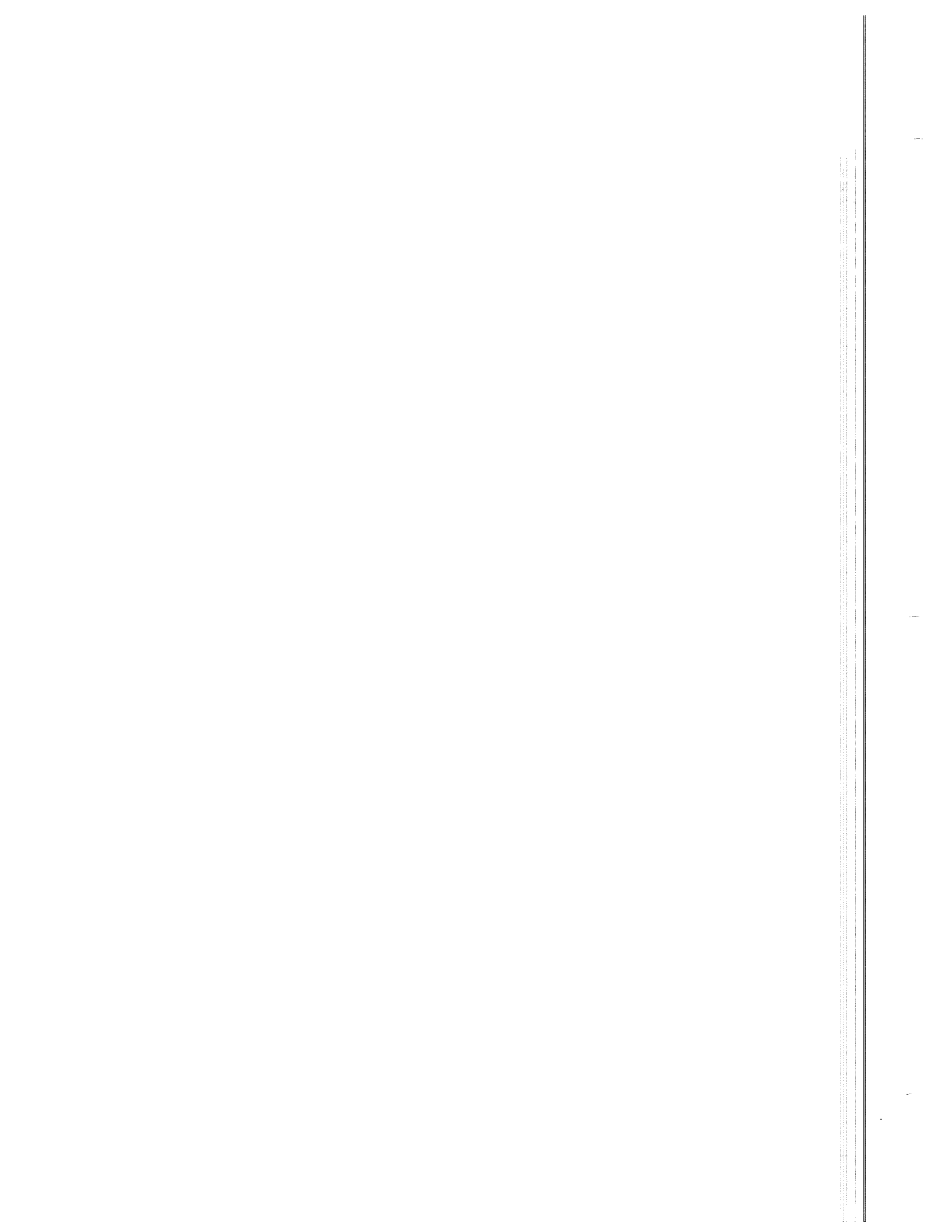
| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|-------------------------------------|----------|-----------------|
| MP626 | 5041-2990 | 4 | 1 | KEY-CAP 1 YES | 28480 | 5041-2990 |
| MP627 | 5041-2991 | 5 | 1 | KEY-CAP ARM | 28480 | 5041-2991 |
| MP628 | 5041-2992 | 6 | 1 | KEY-CAP TRIG DELAY | 28480 | 5041-2992 |
| MP629 | 5041-2993 | 7 | 1 | KEY-CAP ENGR UNITS | 28480 | 5041-2993 |
| MP630 | 5041-2994 | 8 | 1 | KEY-CAP SELECT TRIG | 28480 | 5041-2994 |
| MP631 | 5041-2995 | 9 | 1 | KEY-CAP INPUT COUPLE | 28480 | 5041-2995 |
| MP632 | 5041-2996 | 0 | 1 | KEY-CAP STATE/TRACE | 28480 | 5041-2996 |
| MP633 | 5041-2997 | 1 | 1 | KEY-CAP MEAS DISP | 28480 | 5041-2997 |
| MP633 | 5041-2998 | 2 | 1 | KEY-CAP FRONT BACK | 28480 | 5041-2998 |
| MP634 | 5041-2999 | 3 | 1 | KEY-CAP UPPER LOWER | 28480 | 5041-2999 |
| MP635 | 5041-3000 | 9 | 1 | KEY-CAP A & B | 28480 | 5041-3000 |
| MP636 | 5041-4501 | 7 | 1 | KEY-CAP SPCL MARKER | 28480 | 5041-4501 |
| MP637 | 5041-4502 | 8 | 1 | KEY-CAP Y OFF | 28480 | 5041-4502 |
| MP638 | 5041-4503 | 9 | 1 | KEY-CAP X OFF | 28480 | 5041-4503 |
| MP639 | 5041-4504 | 0 | 1 | KEY-CAP UNITS | 28480 | 5041-4504 |
| MP640 | 5041-4505 | 1 | 1 | KEY-CAP CO-ORD | 28480 | 5041-4505 |
| MP641 | 5041-4506 | 2 | 1 | KEY-CAP SOURCE | 28480 | 5041-4506 |
| MP642 | 5041-4507 | 3 | 1 | KEY-CAP SELECT MEAS | 28480 | 5041-4507 |
| MP643 | 5041-4508 | 4 | 1 | KEY-CAP MEAS MODE | 28480 | 5041-4508 |
| MP644 | 5041-4509 | 5 | 1 | KEY-CAP SPCL FCTN | 28480 | 5041-4509 |
| MP645 | 5041-4510 | 8 | 1 | KEY-CAP SAVE RECALL | 28480 | 5041-4510 |
| MP646 | 5041-4511 | 9 | 1 | KEY-CAP HP-1B FCTN | 28480 | 5041-4511 |
| MP647 | 5041-4512 | 0 | 1 | KEY-CAP DISC | 28480 | 5041-4512 |
| MP648 | 5041-4513 | 1 | 1 | KEY-CAP CURVE FIT | 28480 | 5041-4513 |
| MP649 | 5041-4514 | 2 | 1 | KEY-CAP AUTO MATH | 28480 | 5041-4514 |
| MP650 | 5041-4515 | 3 | 1 | KEY-CAP PAUSE CONT | 28480 | 5041-4515 |
| MP651 | 5041-4516 | 4 | 1 | KEY-CAP WINDOW | 28480 | 5041-4516 |
| MP652 | 5041-4517 | 5 | 1 | KEY-CAP | 28480 | 5041-4517 |
| MP653 | 5041-4518 | 6 | 1 | KEY-CAP START | 28480 | 5041-4518 |
| MP654 | 5041-4519 | 7 | 1 | KEY-CAP MATH | 28480 | 5041-4519 |
| MP655 | 5041-4520 | 0 | 1 | KEY-CAP SYNTH | 28480 | 5041-4520 |
| MP656 | 5041-4521 | 1 | 1 | KEY-CAP HELP | 28480 | 5041-4521 |
| MP656 | 5041-4522 | 2 | 1 | KEY-CAP RANGE | 28480 | 5041-4522 |
| MP657 | 5041-4523 | 3 | 1 | KEY-CAP AUTO SEQ | 28480 | 5041-4523 |
| MP658 | 5041-4524 | 4 | 1 | KEY-CAP X | 28480 | 5041-4524 |
| MP659 | 5041-4525 | 5 | 1 | KEY-CAP Y | 28480 | 5041-4525 |
| MP660 | 5041-4526 | 6 | 1 | KEY-CAP CAL | 28480 | 5041-4526 |
| MP661 | 5041-4527 | 7 | 1 | KEY-CAP VIEW INPUT | 28480 | 5041-4527 |
| MP662 | 5041-4565 | 3 | 1 | KEY-HALF | 28480 | 5041-4565 |
| W1 | 03562-61601 | 6 | 2 | CABLE-INPUT | 28480 | 03562-61601 |
| | 03562-20601 | 0 | 1 | SHIELD, INPUT CABLE | 28480 | 03562-20601 |
| W2 | 03562-61602 | 7 | 1 | CABLE-POWER, ON/OFF | 28480 | 03562-61602 |
| W4 | 03562-61604 | 9 | 1 | CABLE-SOURCE | 28480 | 03562-61604 |
| W5 | 03562-61605 | 0 | 1 | CABLE-TRIGGER | 28480 | 03562-61605 |
| W6 | 03562-61606 | 1 | 1 | CABLE-EXT REF. | 28480 | 03562-61606 |
| W7 | 03562-61607 | 2 | 1 | CABLE-SAMPLE | 28480 | 03562-61607 |
| W8 | 03562-61608 | 3 | 1 | CABLE-SYNC OUT | 28480 | 03562-61608 |
| W9 | 03562-61609 | 4 | 2 | CABLE (RF)-INPUT/ADC | 28480 | 03562-61609 |
| W10 | 03562-61610 | 7 | 1 | CABLE-KEYBOARD | 28480 | 03562-61610 |
| W13 | 03562-61613 | 0 | 1 | CABLE-POWER/MOTHERBOARD | 28480 | 03562-61613 |
| W14 | 03562-61614 | 1 | 1 | CABLE-DISPLAY I/O | 28480 | 03562-61614 |
| W16 | 03562-61616 | 3 | 1 | CABLE-FAN/PWR | 28480 | 03562-61616 |
| W17 | 03562-61617 | 4 | 1 | CABLE-DISP.ADJ. | 28480 | 03562-61617 |
| W18 | 03562-61618 | 5 | 3 | CABLE-POWER PRIM | 28480 | 03562-61618 |
| W24 | 03562-61624 | 3 | 2 | CABLE-GRD | 28480 | 03562-61624 |
| W190-W192 | 03562-61619 | 6 | 3 | CABLE-DISPLAY XYZ | 28480 | 03562-61619 |
| | 8120-1378 | 1 | 1 | POWERCORD, US/CAN STRGHT--GRAY | 16428 | KH-7081 |
| | 2110-0056 | 3 | 1 | FUSE 6A 250V NTD 1.25X.25 UL | 75915 | 312006 |
| | 03562-90000 | 0 | 1 | MANUAL, OPER. | K01001 | 03562-90000 |
| | 03562-90009 | 9 | 1 | MANUAL-PERFORMANCE TEST | 28480 | 03562-90009 |
| | 03562-90030 | 6 | 1 | MANUAL-PROGM | K01001 | 03562-90030 |
| | 03562-90890 | 6 | 1 | MANUAL ASSEMBLY | 28480 | 03562-90890 |
| | 0515-0413 | 2 | 39 | SCREW-MACH M4 X 0.7 6MM-LG PAN-HD | 16941 | 0515-0413 |
| | 0515-0210 | 7 | 38 | SCREW-MACH M4 X 0.7 8MM-LG PAN-HD | 16941 | 0515-0210 |
| | 0515-1331 | 5 | 16 | SCR, M4X0.7X6 FH | 77250 | 0515-1331 |
| | 0515-0407 | 4 | 12 | SCREW-MACH M3 X 0.5 10MM-LG PAN-HD | 16941 | 0515-0407 |
| | 0515-1232 | 5 | 11 | SCREW-MACH M3.5 X 0.6 8MM-LG PAN-HD | 77250 | 0515-1232 |

See introduction to this section for ordering information
 *Indicates factory selected value

Table 4-3 Replaceable Parts cont.

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|--------|-----|--|----------|-----------------|
| | 0515-0396 | 9 | 8 | SCREW-MACH M4.0X10MM | 16941 | 2510-0046 |
| | 0515-0211 | 8 | 7 | SCREW-MACH M3 X 0.5 6MM-LG PAN-HD | 16941 | 0515-0211 |
| | 2950-0043 | 8 | 7 | NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK | H01042 | 2950-0043 |
| | 2190-0009 | 4 | 6 | WASHER-LK INTL T NO. 8 .168-IN-ID | T12345 | 1908-00 |
| | 0535-0006 | 1 | 6 | NUT-HEX DBL-CHAM M4 X 0.7 3.2MM-THK | H01043 | 0535-0006 |
| | 0403-0179 | 0 | 6 | BUMPER FOOT-ADH MTG | 76381 | SJ 5012 BLK |
| | 2190-0016 | 3 | 5 | WASHER-LK INTL T 3/8 IN .377-IN-ID | T12345 | 1920-02 |
| | 2190-0054 | 9 | 5 | WASHER-LK INTL T 1/2 IN .505-IN-ID | T12345 | 1924-12 |
| | 0515-0414 | 3 | 5 | SCREW-MACH M4 X 0.7 10MM-LG PAN-HD | 16941 | 0515-0414 |
| | 0515-0657 | 6 | 5 | SCREW-MACH M3.5 X 0.6 8MM-LG | M01088 | 0515-0657 |
| | 2190-0007 | 2 | 4 | WASHER-LK INTL T NO. 6 .141-IN-ID | T12345 | 1906-00-00-2580 |
| | 0515-0147 | 9 | 4 | SCREW-MACH M3.5 X 0.6 20MM-LG PAN-HD | 83486 | 0515-0147 |
| | 0515-1132 | 4 | 4 | SCREW-MACH M5 X 0.8 10MM-LG | M01088 | 0515-1132 |
| | 2360-0195 | 0 | 4 | SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI | 01536 | 2360-0195 |
| | 0535-0007 | 2 | 4 | NUT-HEX DBL-CHAM M3.5 X 0.6 2.8MM-THK | H01043 | 0535-0007 |
| | 0535-0013 | 0 | 4 | NUT-THUMB M3.5 X 0.6 5MM-THK 8.6MM-WD | L01005 | 0535-0013 |
| | 0360-1632 | 0 | 3 | TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR | 79963 | 761-3/8 |
| | 2950-0035 | 8 | 3 | NUT-HEX-DBL-CHAM 15/32-32-THD | T123 | 2950-0035 |
| | 1400-1122 | 0 | 3 | CLAMP-CABLE .187-DIA .735-WD NYL | 34785 | 021-0188 |
| | 3050-0066 | 8 | 2 | WASHER-FL MTLK NO. 6 .147-IN-ID | 73734 | 1451 |
| | 3050-0067 | 9 | 2 | WASHER-FL MTLK 5/16 IN .375-IN-ID | 73734 | 31-550 |
| | 0515-0066 | 1 | 2 | SCREW-MACH M3.5 X 0.6 6MM-LG PAN-HD | 83486 | 0515-0066 |
| | 0515-0081 | 0 | 2 | SCREW-MACH M3.5 X 0.6 10MM-LG | 83486 | 0515-0081 |
| | 0515-0482 | 5 | 2 | SCREW-SKT-HD-CAP M3 X 0.5 8MM-LG | A01148 | 0515-0482 |
| | 0361-1040 | 6 | 2 | RVT-BLD DMHD .125D .06GRP AL | 19738 | 1125-0404 |
| | 2950-0054 | 1 | 2 | NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK | T123 | 2950-0054 |
| | 7120-3416 | 1 | 2 | LABEL-WARNING 1.25-IN-WD 2.75-IN-LG | M01073 | 7120-3416 |
| | 0400-0011 | 3 | 2 | GROMMET-RND .375-IN-ID .5-IN-GRV-OD | S02026 | 500 |
| | 0400-0062 | 4 | 1 | GROMMET-RND .5-IN-ID .625-IN-GRV-OD | 51633 | 8069 |
| | 2190-0047 | 0 | 1 | WASHER-LK 82 CTSK EXT T NO. 6 .142-IN-ID | T12345 | 1506-00 |
| | 2190-0060 | 7 | 1 | WASHER-LK INTL T 1/4 IN .256-IN-ID | T12345 | 1214-10 |
| | 2190-0575 | 9 | 1 | WASHER-LK INTL T 1/2 IN .64-IN-ID | 73734 | 2190-0575 |
| | 2950-0006 | 3 | 1 | NUT-HEX-DBL-CHAM 1/4-32-THD .094-IN-THK | 73734 | 9000 |

See introduction to this section for ordering information
 *Indicates factory selected value



SECTION V

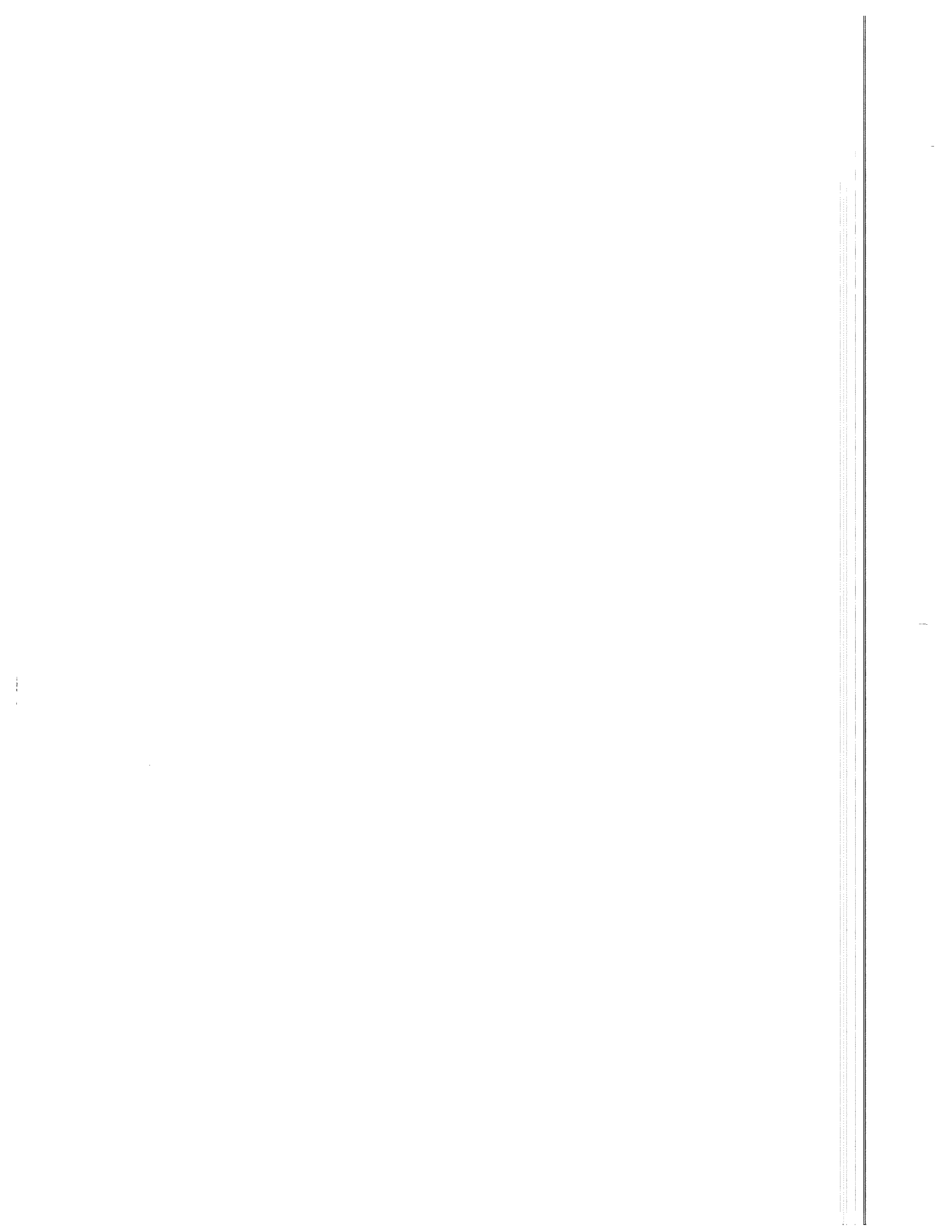
MANUAL BACKDATING

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| 5-2 | Manual Changes Supplement | 5-1 |
| 5-3 | Format | 5-1 |
| 5-4 | A1 Digital Source | 5-1 |
| 5-5 | A2 CPU | 5-1 |
| 5-6 | A3 Program ROM | 5-2 |
| 5-7 | A4 Local Oscillator | 5-2 |
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SECTION V

MANUAL BACKDATING

5-1 INTRODUCTION

This revision of this manual applies directly to all instruments. Earlier versions of this instrument, however, differ in design and appearance from those currently being produced. The information in this section documents the earlier instrument configurations and associated servicing procedures.

5-2 MANUAL CHANGES SUPPLEMENT

As Hewlett-Packard continues to improve the performance of the HP 3562A, corrections and modifications to the manual may be required. Required changes are documented by a yellow Manual Changes supplement and/or revised pages. To keep the manual up-to-date, periodically request the most recent supplement, available from the nearest Hewlett-Packard office (see sales and support offices listing at the back of this manual).

5-3 FORMAT

Design and component changes within the instrument are noted by the "Δ" symbol. When this symbol appears, refer to the appropriate assembly heading in this section for the manual changes.

5-4 A1 DIGITAL SOURCE

Current revision: B

Previous revisions:

Revision A has U104 installed in a socket (part number 1200-0474). Revision A differs from Revision B in table A1-6. Change the signatures for U112 as follows:

| Component | Pin | Signature |
|-----------|-----|-----------|
| U112 | 12 | OPHC |
| | 16 | OPHC |

5-5 A2 CPU

Current revision: C

Previous revisions:

Revision B differs from revision C as follows:

1. There is no J021 on revision B.
2. Reference designator C101 is C1000 on revision B.

5-6 A3 PROGRAM ROM

Current revision: B

Previous revisions: None

5-7 A4 LOCAL OSCILLATOR

Current revision: C

Previous revisions:

Revision B is electrically identical to revision C. The following components are in sockets in revision B:

| Component | Socket Part Number |
|-----------|--------------------|
| U20 | 1200-0567 |
| U36 | 1200-0654 |
| U57 | 1200-0638 |
| U47 | 1200-0638 |
| U33 | 1200-0639 |

Revision A differs from revision B as follows:

- Signature analysis connector J1 is mislabeled. It should be labeled as follows:

J1-1 GND
 J1-3 CLK
 J1-4 STP
 J1-4 SRT

- Change the following part numbers in the Replaceable Parts list:

U20 to 03562-60342
 U29 to 03562-60341

- In table A4-2, change the signatures for U20 and U29 as follows:

| Component | Pin | Signature | Component | Pin | Signature |
|-----------|-----|-----------|-----------|-----|-----------|
| U20 | 9 | P1A2 | U29 | 9 | UH9P |
| | 10 | 9149 | | 10 | HF11 |
| | 11 | P43P | | 11 | 11C0 |
| | 13 | 9C68 | | 13 | 6582 |
| | 14 | 12C0 | | 14 | P104 |
| | 15 | 2H8P | | 15 | 4791 |
| | 16 | 6C7P | | 16 | 90AF |
| | 17 | 6PA1 | | | |

4. Change the A4 schematic in section IX as shown in figure 5-A4a.

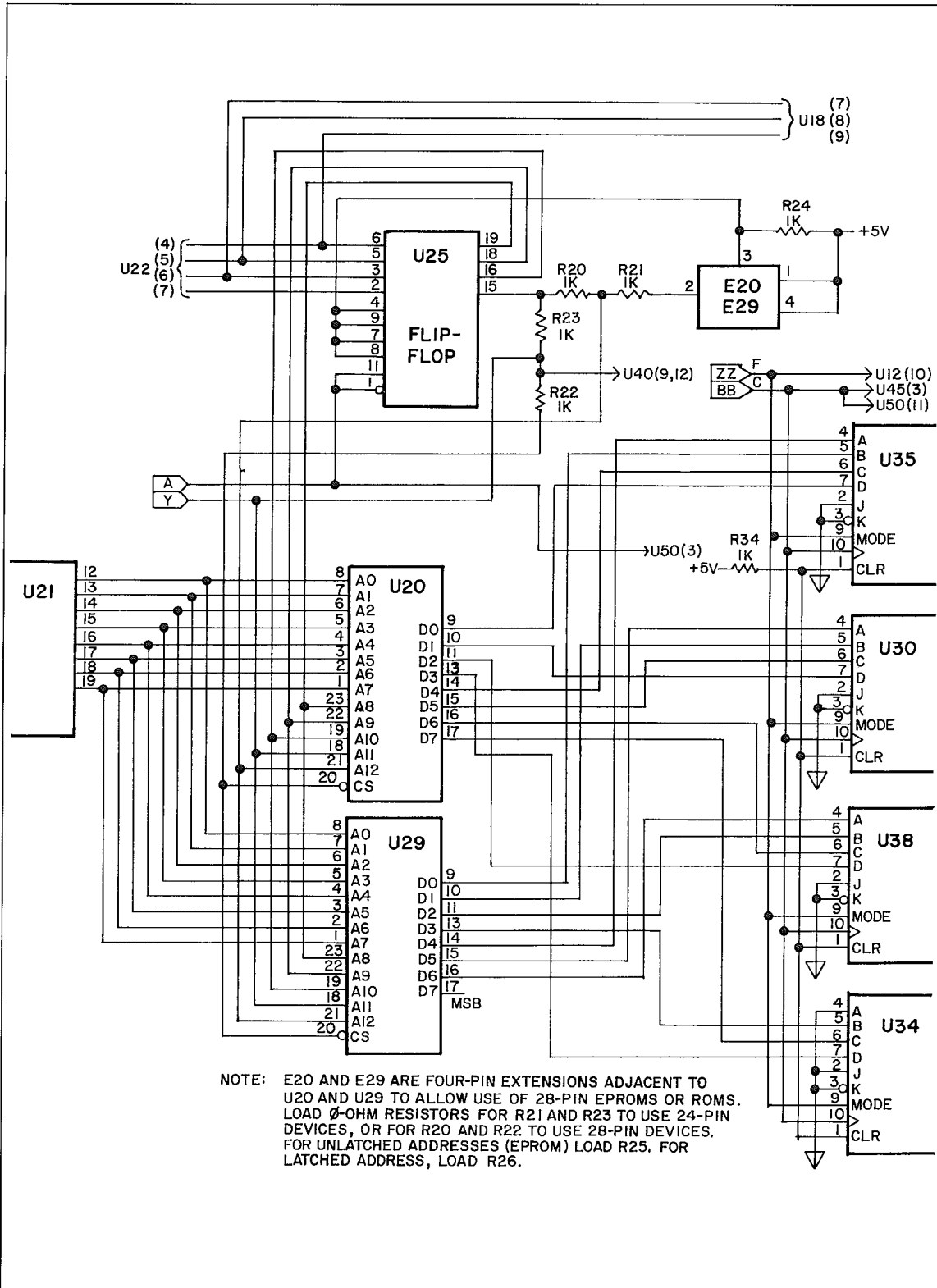


Figure 5-A4a Local Oscillator Schematic Revision A

5. Change the component locator as shown in figure 5-A4b.

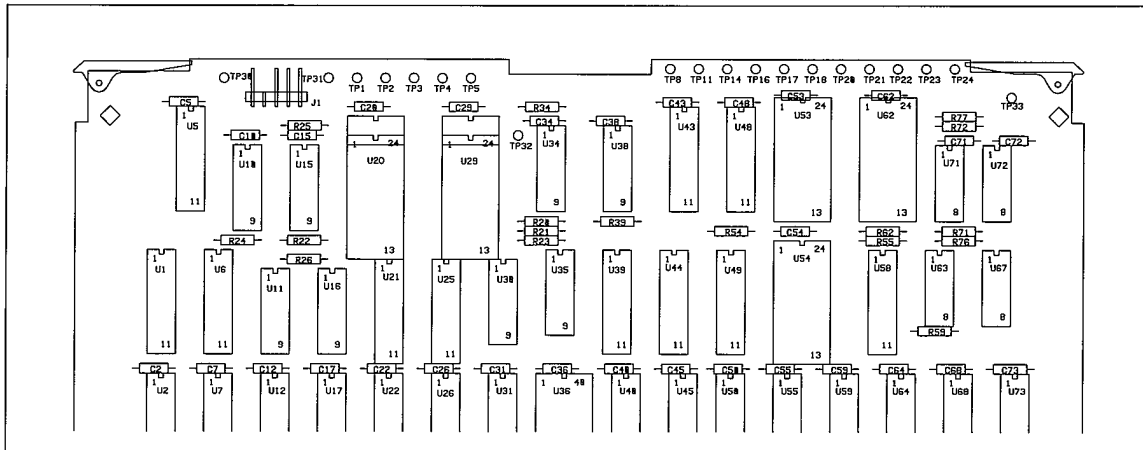


Figure 5-A4b Local Oscillator Component Locator Revision A

5-8 A5 DIGITAL FILTER

Current revision: E

Previous revisions: All revisions are electrically the same as revision E.

Revisions A through D: The following components are in sockets:

| Component | Socket Part Number |
|-----------|--------------------|
| U107 | 1200-0607 |
| U109 | 1200-0638 |
| U110 | 1200-0638 |
| U512 | 1200-0638 |
| U206 | 1200-0700 |
| U306 | 1200-0700 |

Revisions A and B: All jumpers are identified with a "W" rather than a "J".

| Revs. A and B | Later Revs. |
|---------------|-------------|
| W002 | J002 |
| W003 | J003 |
| W004 | J004 |
| W005 | J005 |
| W006 | J006 |
| W007 | J007 |

Revision A: Make the following changes:

1. Polarity marks for CR1 and CR2 are at the wrong end of the component.

2. Change test point labels as follows:

| Test Point | Rev A | Other Revs. |
|------------|--------|-------------|
| TP9 | CHFB1 | CH1FB1 |
| TP10 | CHFB2 | CH1FB2 |
| TP14 | CH1SRT | CH1STRT |
| TP21 | XCVRE1 | XCVREN1 |
| TP22 | XCVRE2 | XCVREN2 |

3. The test position for W7 is different on revision A. To put W7 in the normal (N) position, take the jumpers off. To put W7 in the test (T) position, set the jumpers as shown in figure 5-A5.

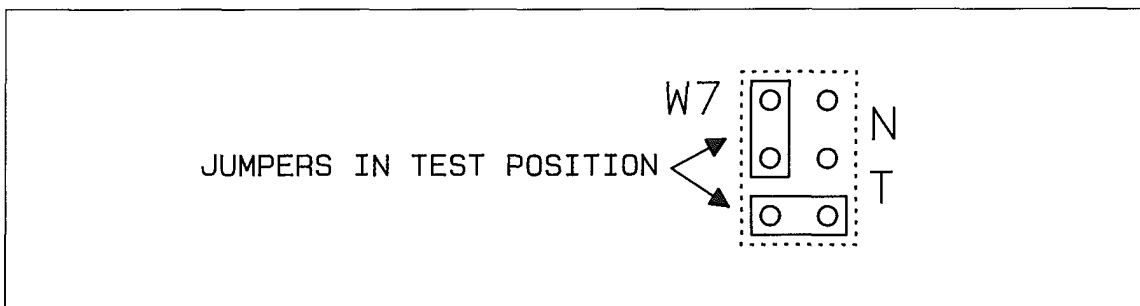


Figure 5-A5 Digital Filter W7 Position Revision A

5-9 A6 DIGITAL FILTER CONTROLLER

Current revision: C

Previous revisions are all electrically the same as revision C:

Revision B: Component U208 is in a socket (part number 1200-0700).

Revision A: Make the following changes:

1. The following components are in sockets:

| Component | Socket Part Number |
|-----------|--------------------|
| U206 | 1200-0638 |
| U208 | 1200-0700 |
| U309 | 1200-0700 |

2. Jumper J2 is identified as W2 on revision A.

5-10 A7 FLOATING POINT PROCESSOR

Current revision: B

Previous revisions:

Revision A is electrically identical to revision B. The following components are in different locations on the revision A component locator:

C43, U114, and U115 are closer to the top of the board.

R17 is located just above and parallel to C47.

5-11 A8 GLOBAL RAM

Current revision: B

Previous revisions:

Revision A is electrically identical to revision B. The test jumpers J3 through J9 are not labeled on revision A. Normal (N) position is to the left, test (T) position to the right.

5-12 A9 FAST FOURIER TRANSFORM PROCESSOR

Current revision: B

Previous revisions:

Revision A is electrically identical to revision B. On the revision A component locator, C117 is located directly above U117.

5-13 A12 MOTHER BOARD

Current revision: B

Previous revisions:

Revision A is electrically identical to revision B.

5-14 A15 KEYBOARD

Current revision: B

Previous revisions:

Revision A is electrically identical to revision B. On the revision A component locator, J9 is located just below U404.

5-15 A17 DISPLAY INTERFACE

Current revision: A

Previous revisions: None

5-16 A18 POWER SUPPLY

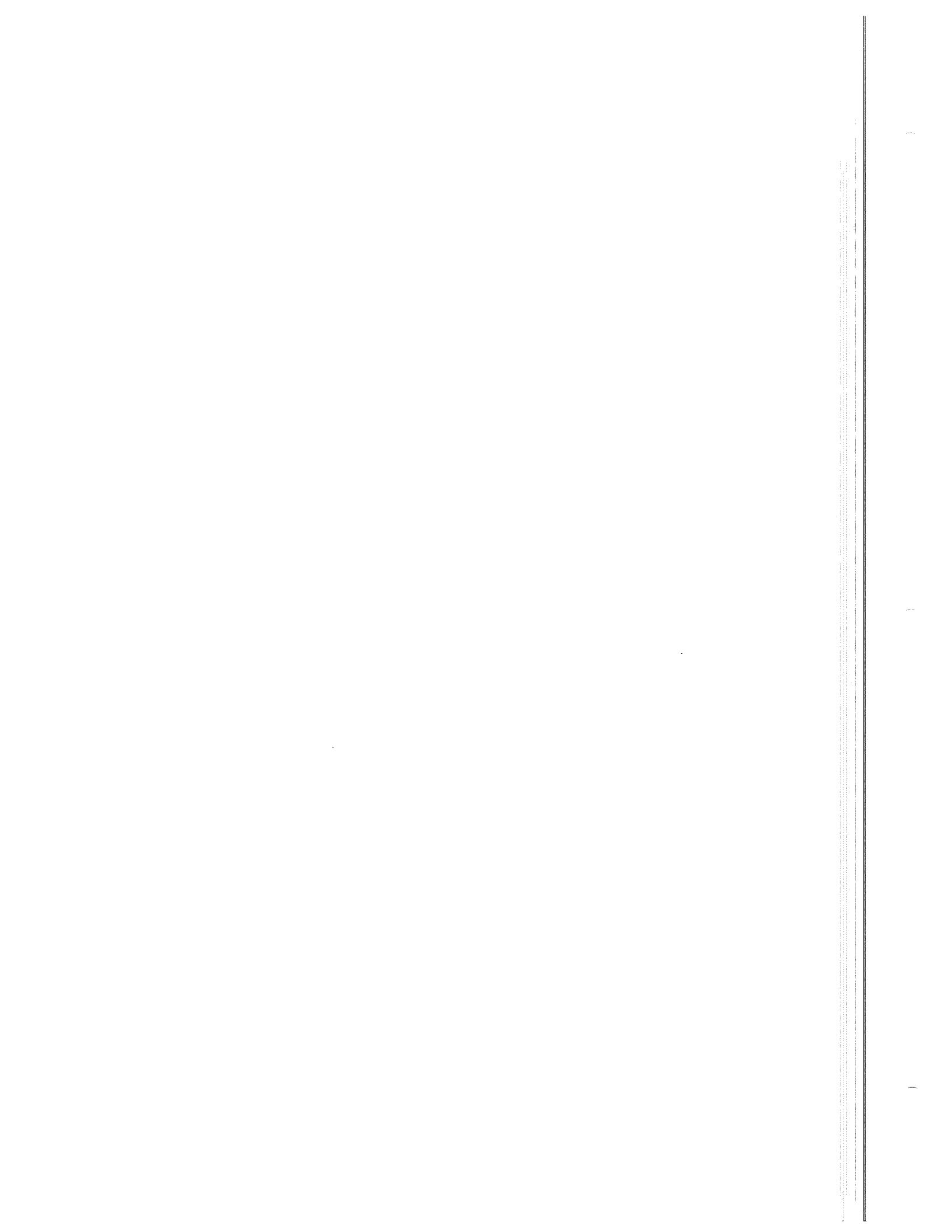
Current revision: C

Previous revisions:

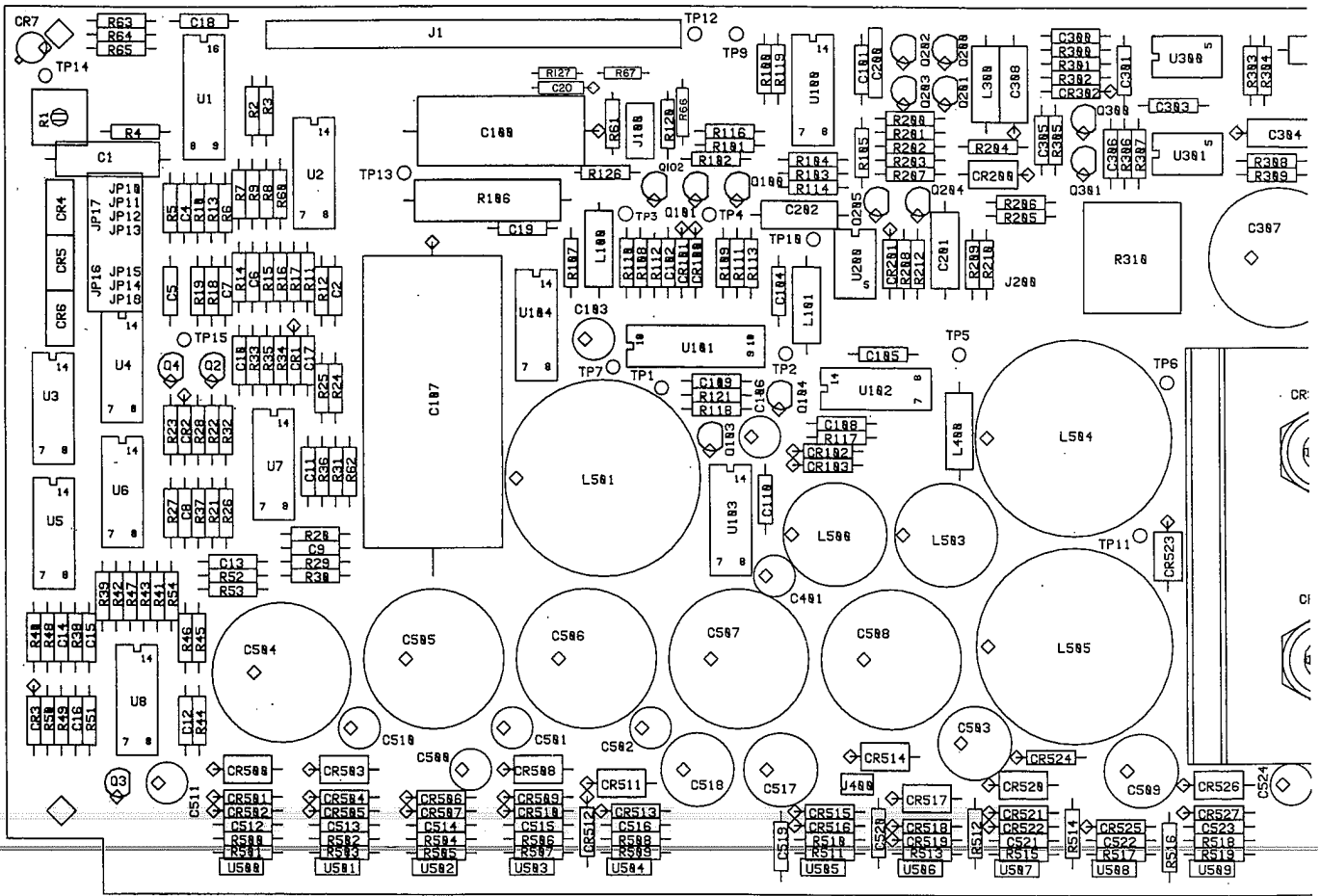
Revisions A and B differ from revision C as follows:

1. Change the Replaceable Parts List, table 5-3, as follows:
 - a. Change the following components:
 - C108 and C109 to 0160-4787, 22 pF.
 - C200 to 0160-0128, 2.2 μ F.
 - C304 to 0180-0374, 10 μ F.
 - R116 to 0757-0401, 100 OHM.
 - R126 and R304 to 0757-0442, 10K.
 - b. Delete the following components:
 - C527, C528, C529, and C530.
 - CR530, CR531, CR532, and CR533.
 - c. Add the following components:
 - R104, 0757-0280, 1K.
 - R114, 0698-3228, 49.9K.
 - R118, 0698-3279, 4.99K.
 - R208, 0757-0465, 100K.
 - Q103 and Q104, 1854-0215, NPN 2N3904.
 - Q205, 1853-0036, PNP 2N3906.
 - U100, 1820-3183, 74HC03 CMOS.
2. Remove A18, component locator revision C, and schematic revision C, and replace them with figures 5-A18a and 5-A18c.

Revision A was modified to be electrically identical to revision B (see figure 5-A18b).



MODEL 3562A



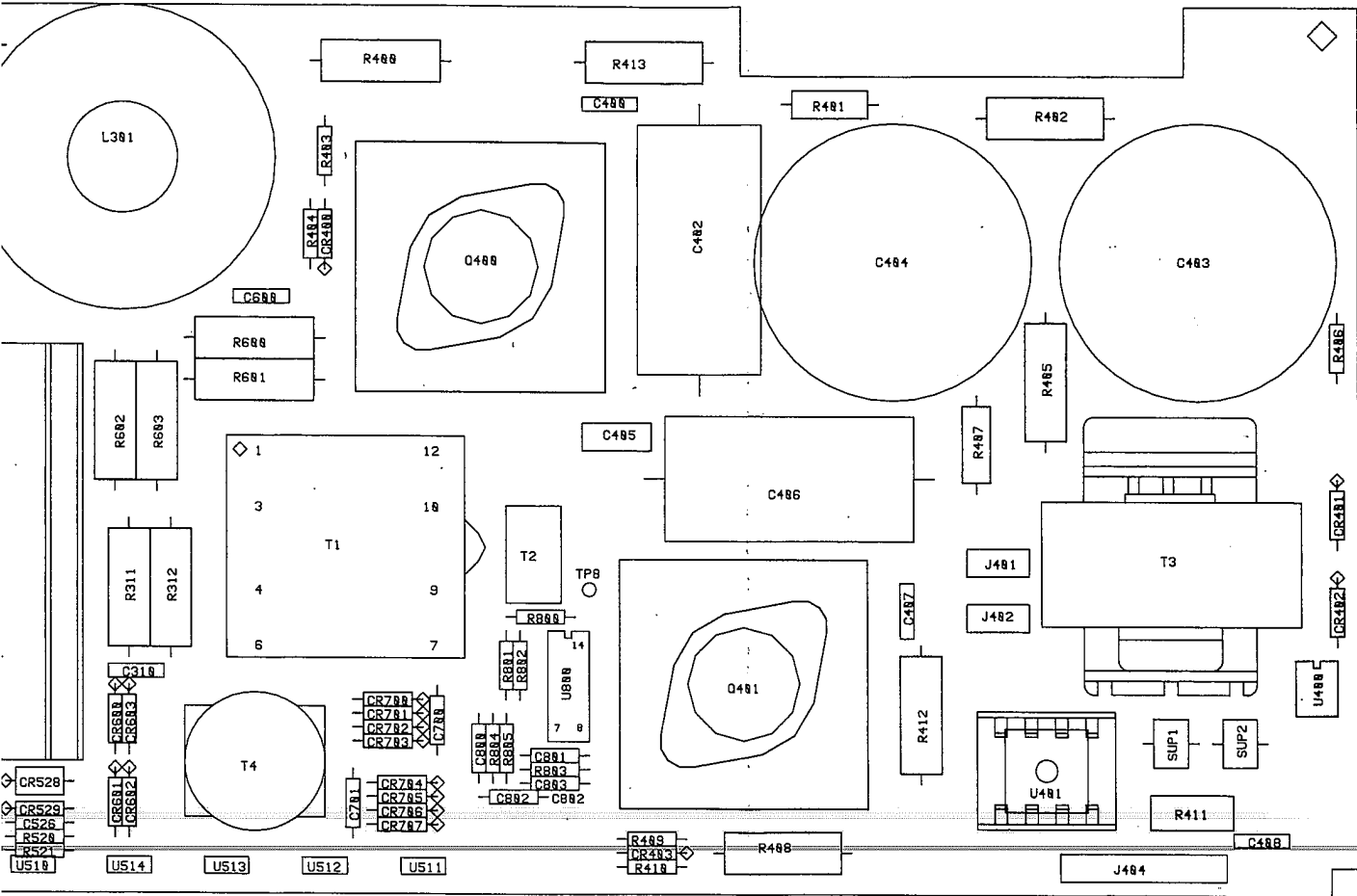
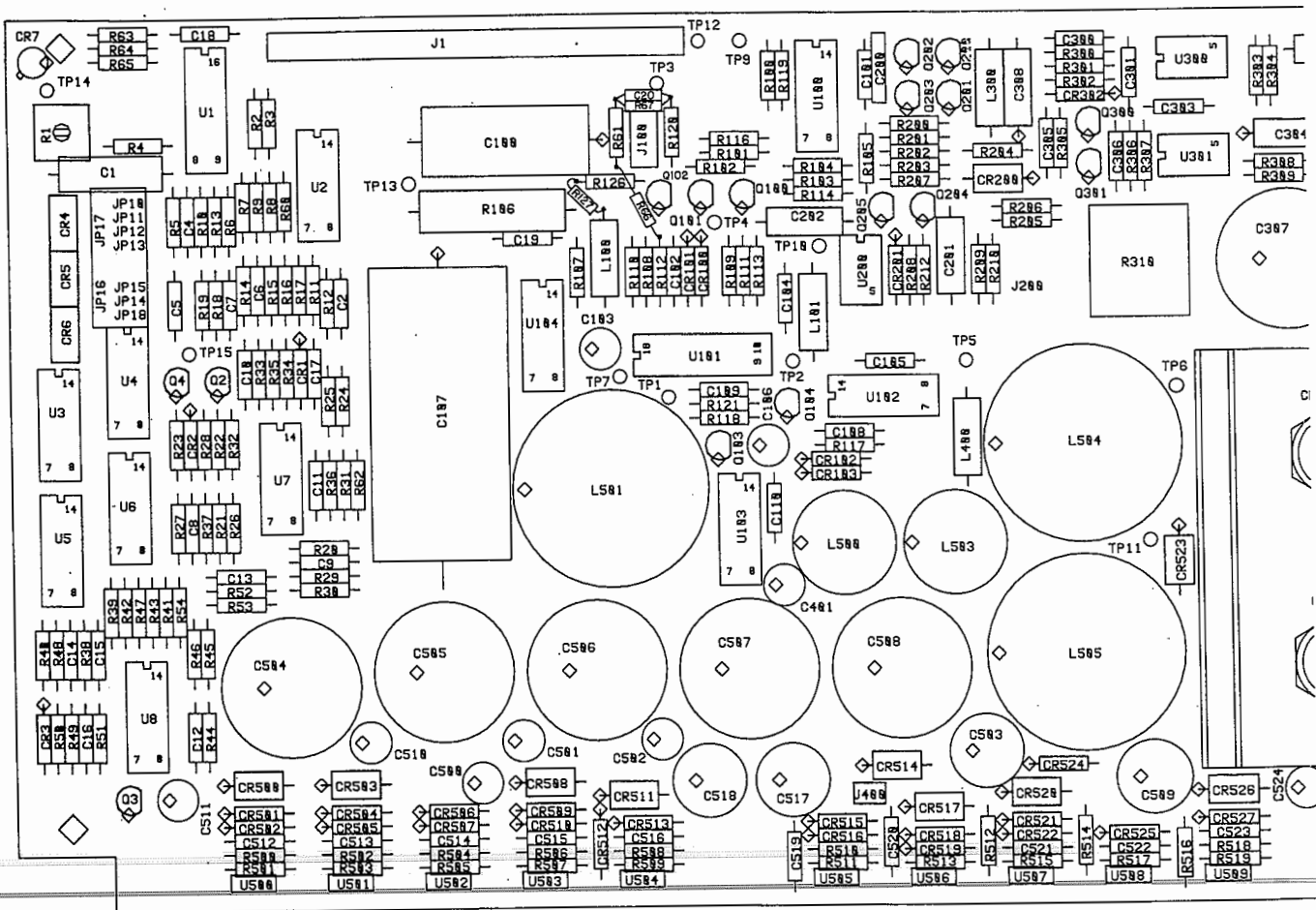


Figure 5-A18a Power Supply Component Locator Revision B

MODEL 3562A



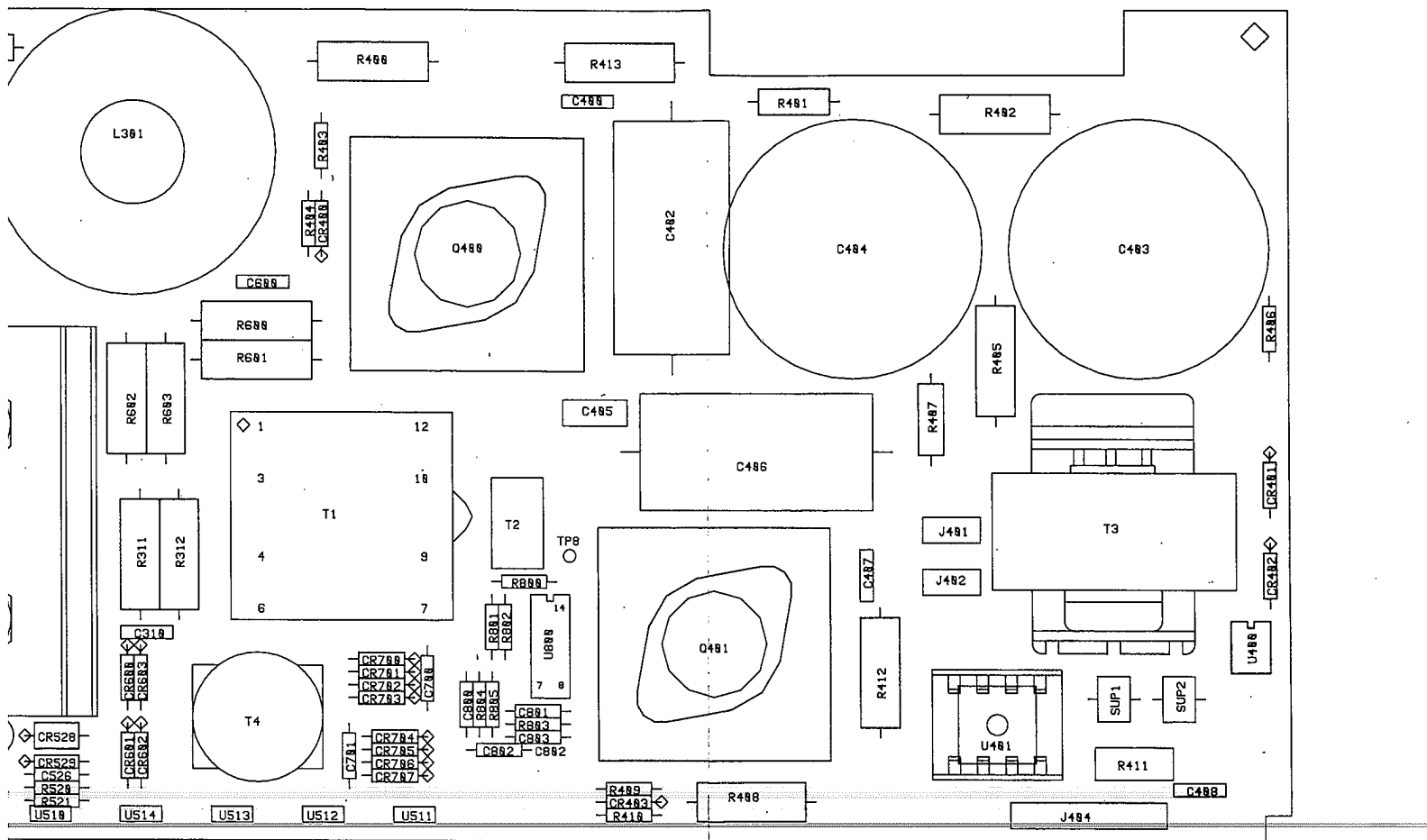
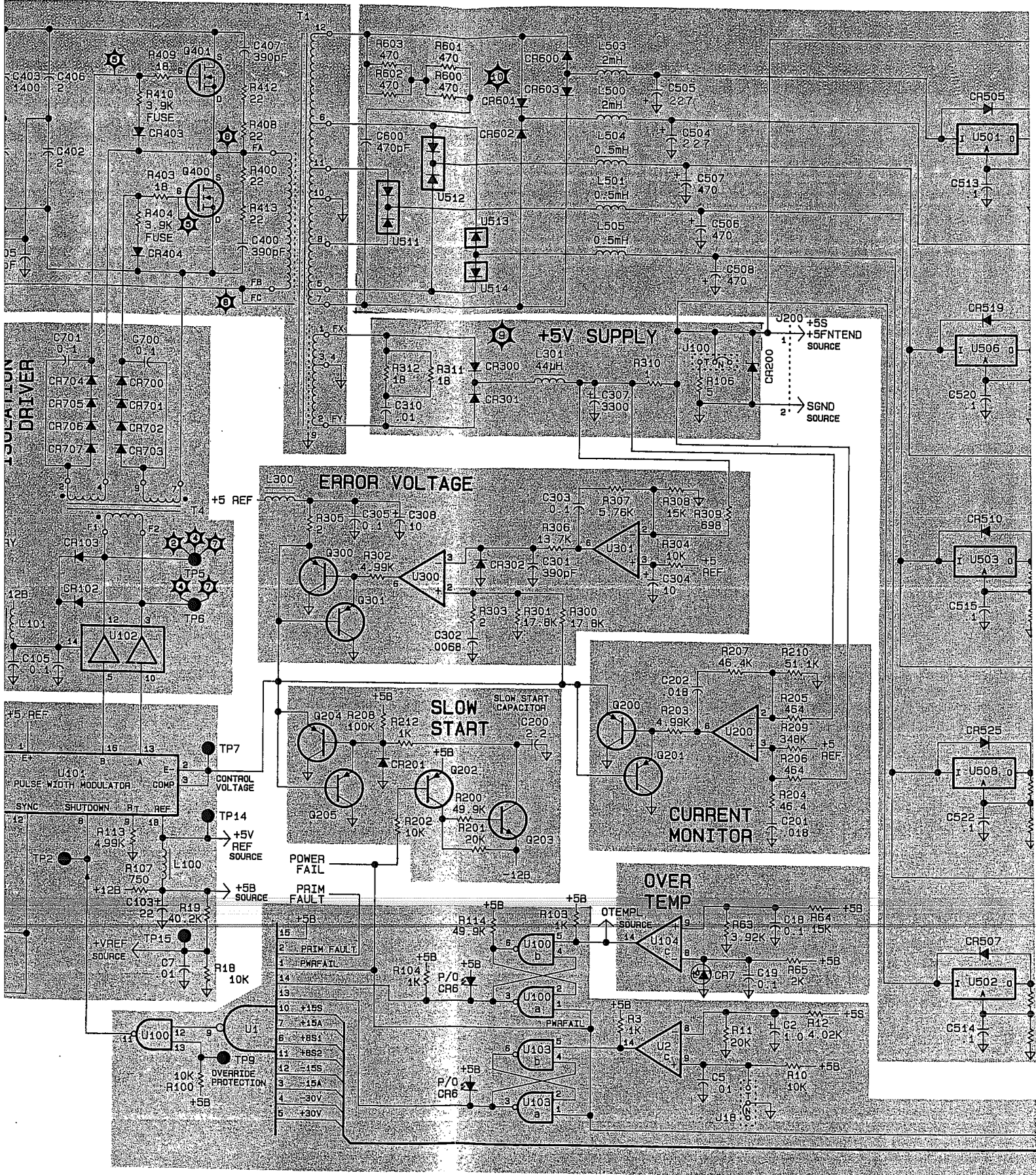
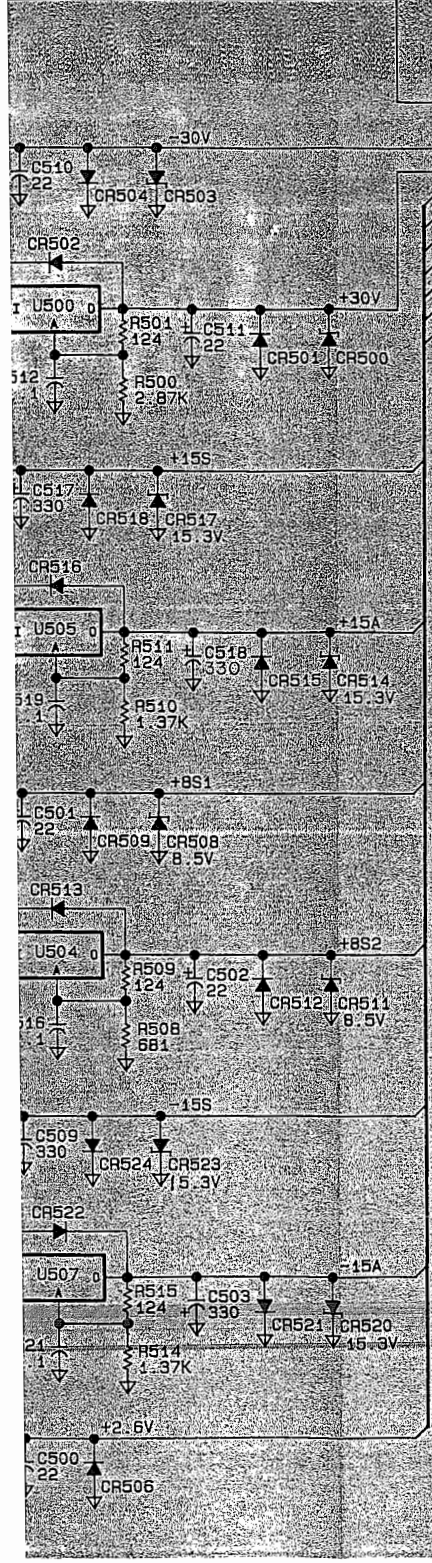


Figure 5-A18b Power Supply Component Locator Revision A

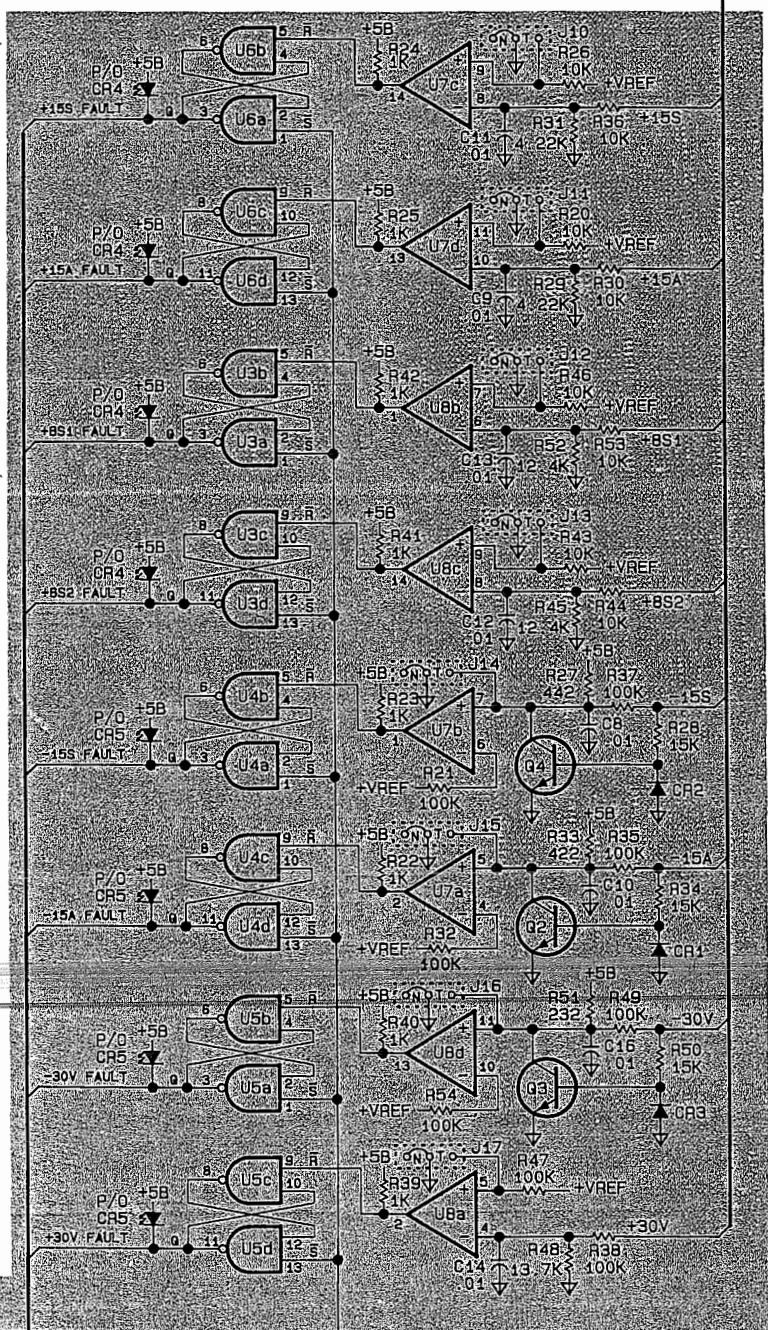


SECONDARY LINEAR SUPPLIES



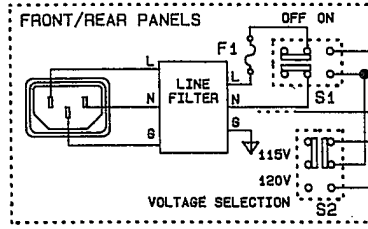
| | | |
|----------------|-------------|----|
| FROM U2 (13) | PWRUP | 15 |
| FROM U104 (13) | PWRDNL | 14 |
| FROM U104 (14) | OTEMPL | 13 |
| FROM U100 (9) | SMPDUT | 12 |
| | +5S/+5FNEND | 5 |
| | (KEY) | 11 |
| | -30V | 2 |
| | +30V | 1 |
| | +15S | 9 |
| | +15A | 3 |
| | +8S1 | 7 |
| | +8S2 | 8 |
| | -15S | 10 |
| | -15A | 4 |
| | +2.6V | 6 |

TO A12

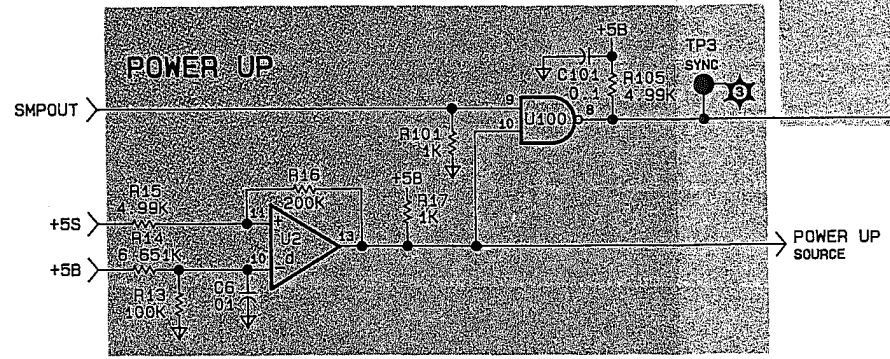
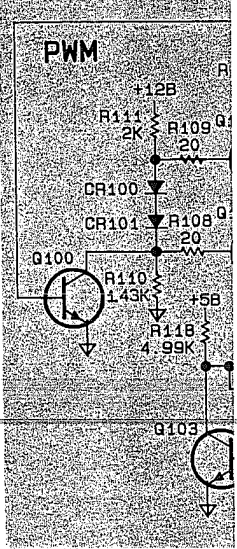
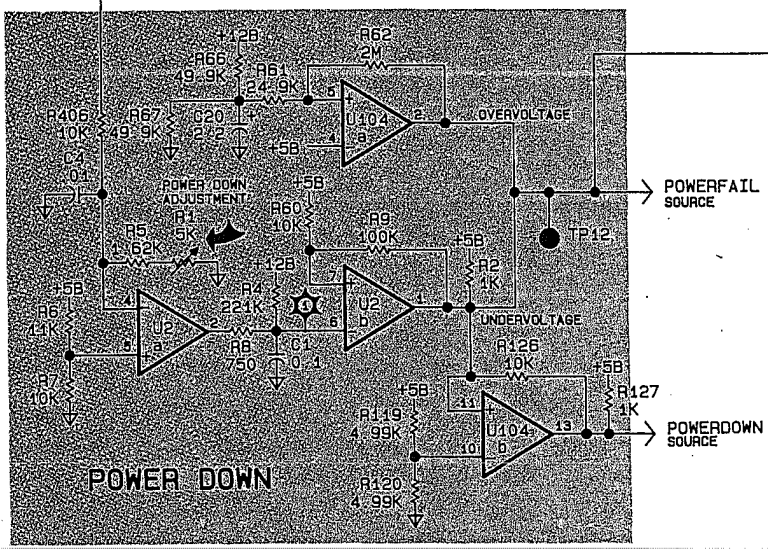
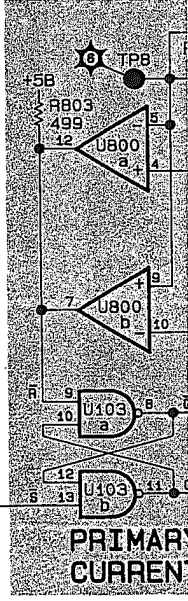
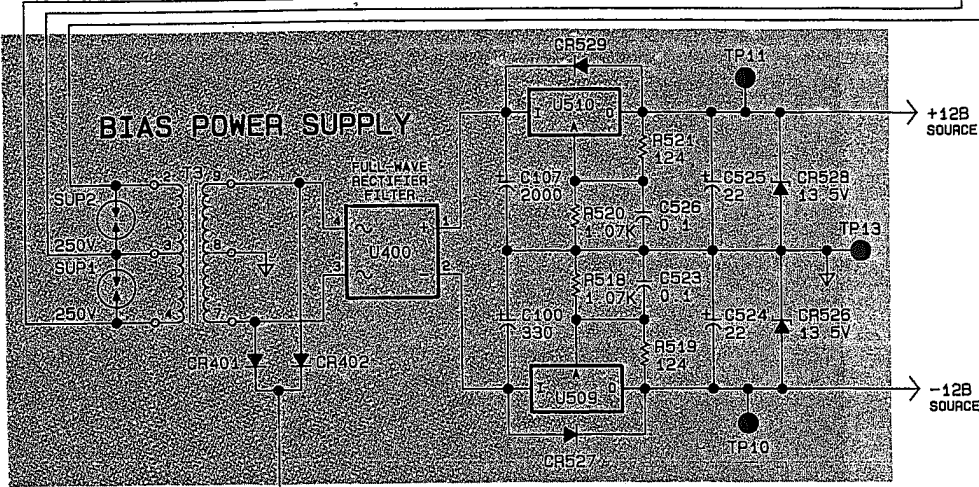
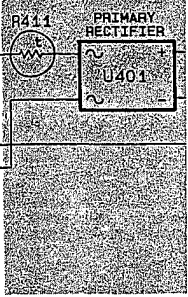


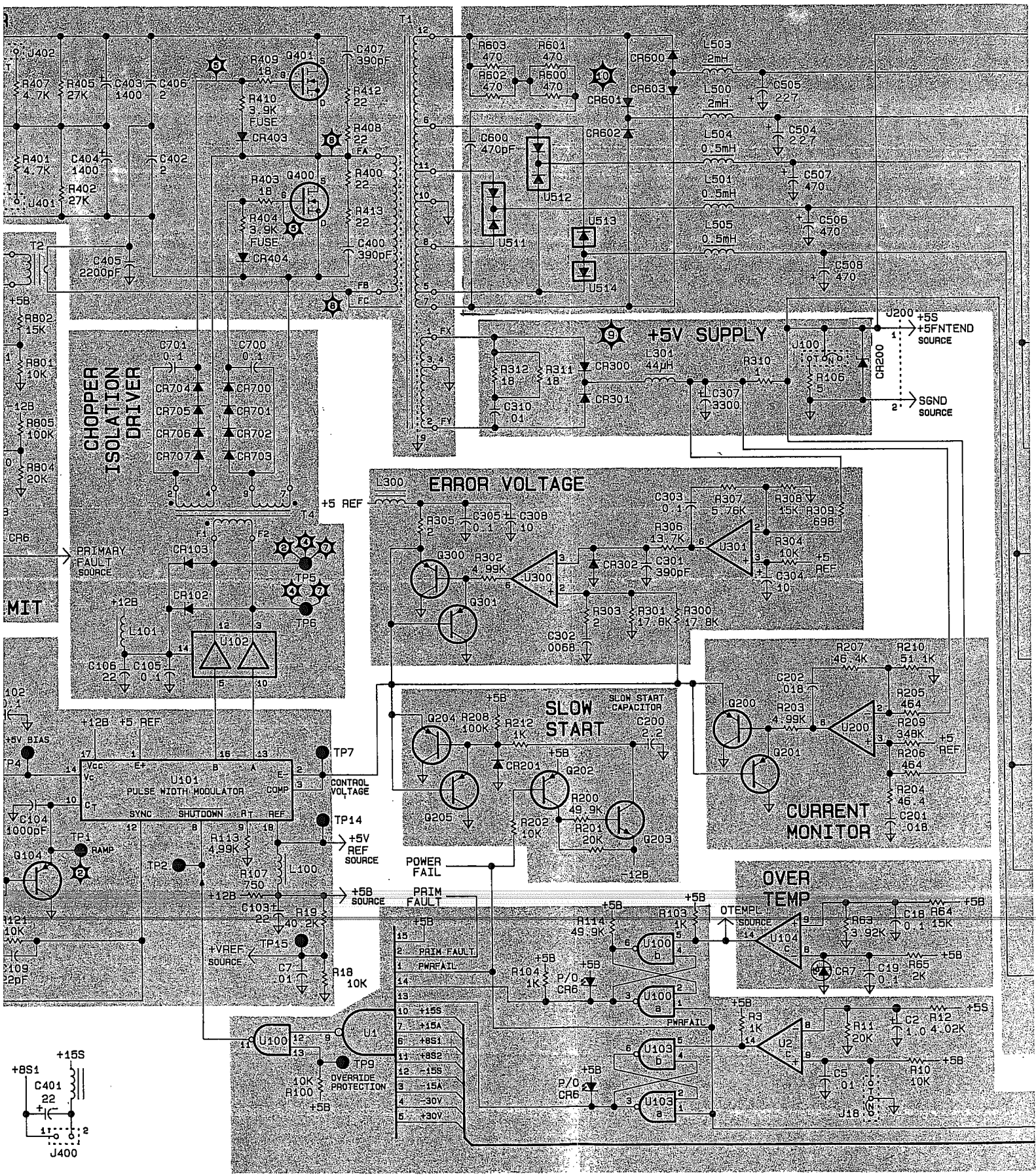
PROTECTION MONITOR

Figure 5-A18c Power Supply Schematic Revisions A and B



PRIMARY P





CHOPPER ISOLATION DRIVER

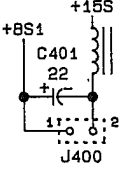
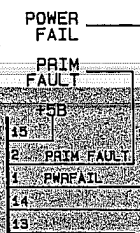
+5V SUPPLY

ERROR VOLTAGE

SLOW START

CURRENT MONITOR

OVER TEMP



5-17 A22 HP-IB

Current revision: A

Previous revisions: None

5-18 A30 ANALOG SOURCE

Current revision: C

Previous revisions:

Revision B is electrically identical to revision C.

The revision B component locator differs from revision C in the spacing of three groups of axial lead components. These components are located to the right of U600, U456, and U503.

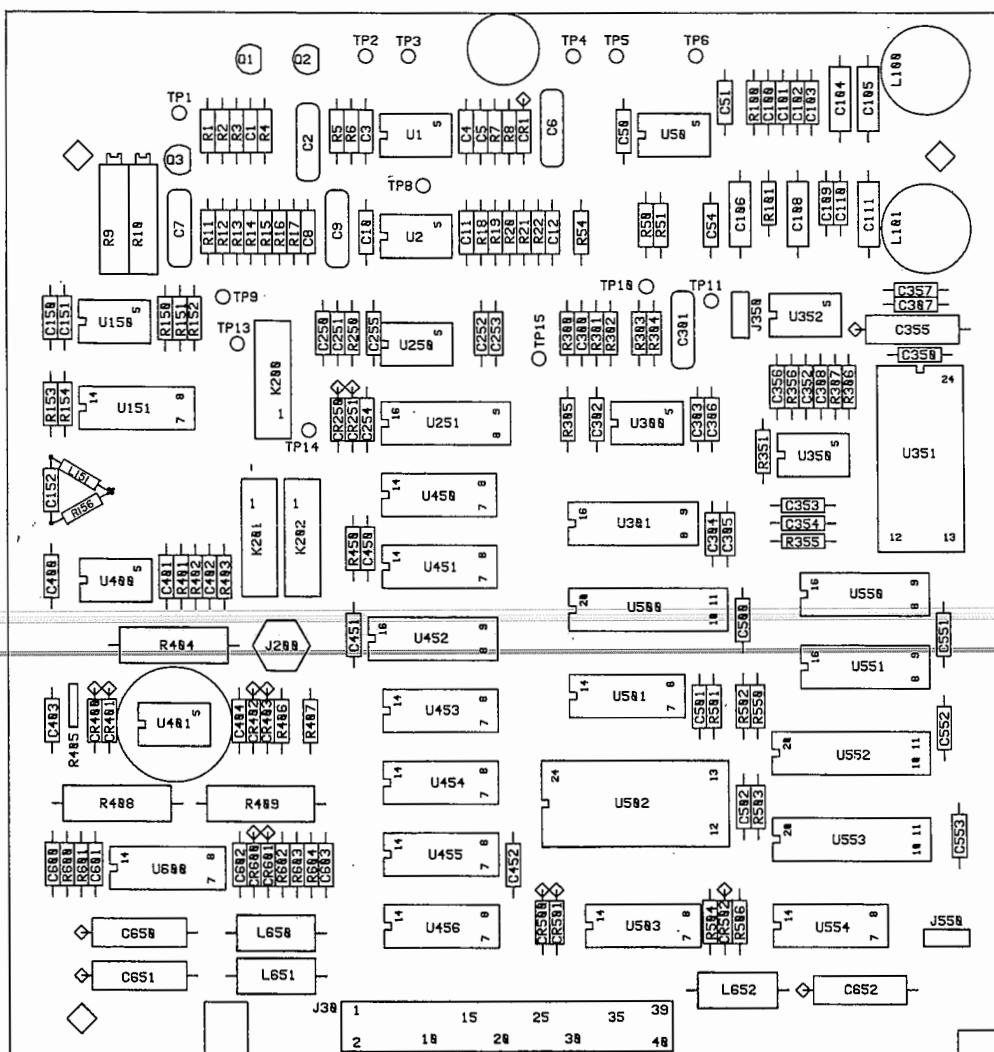


Figure A30 Analog Source Component Locator Revisions B & C

5-19 A31 TRIGGER

Current revision: B

Previous revisions:

Revision A differs from revision B as follows (see figures 5-A31a and 5-A31b):

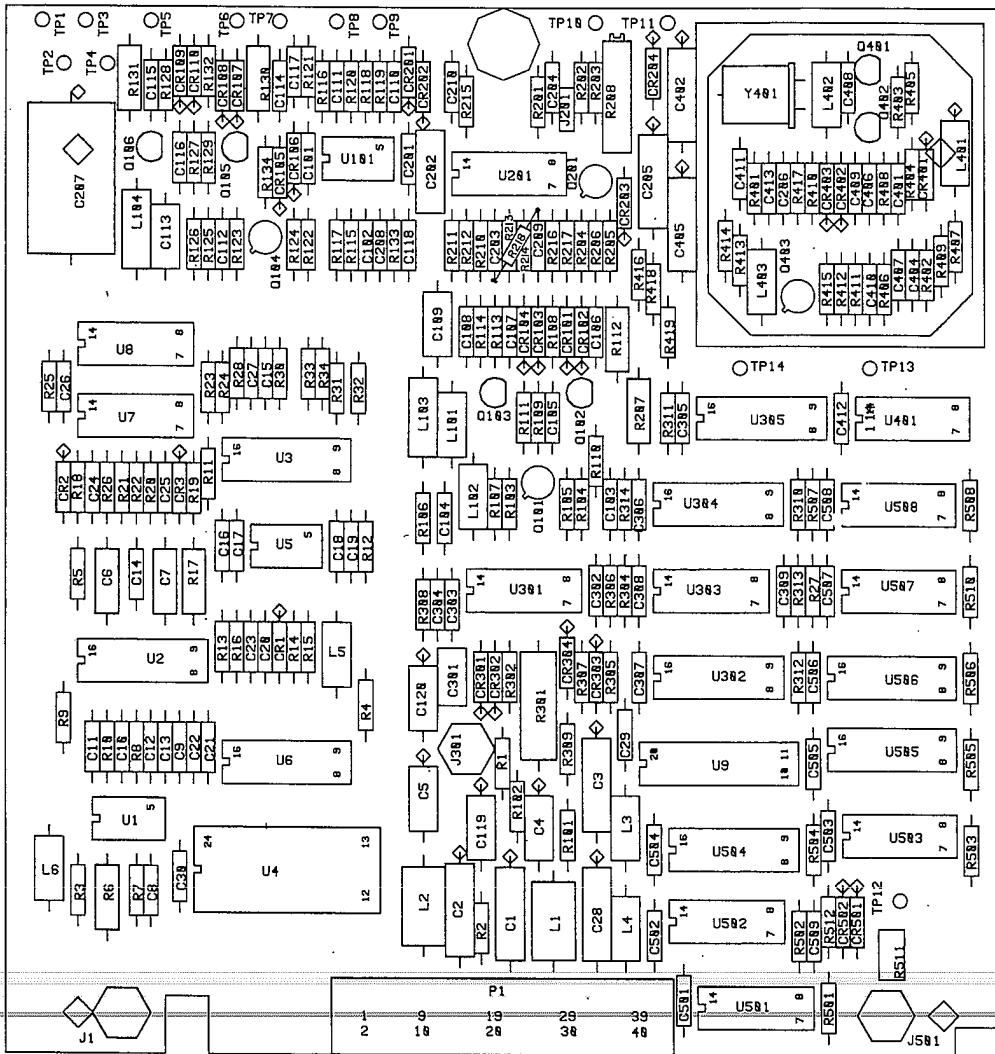
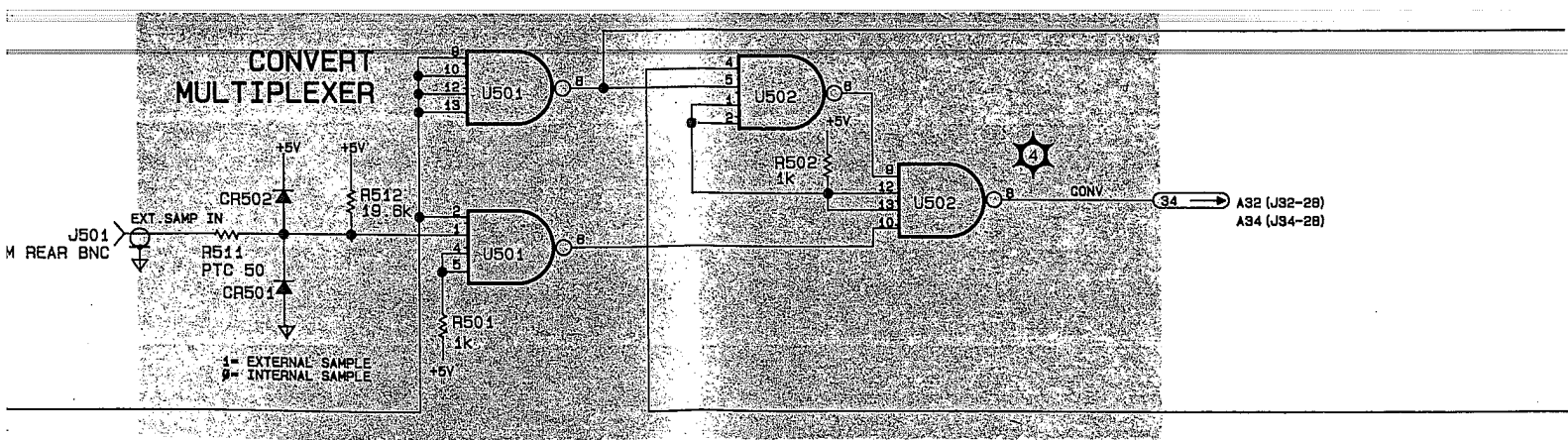
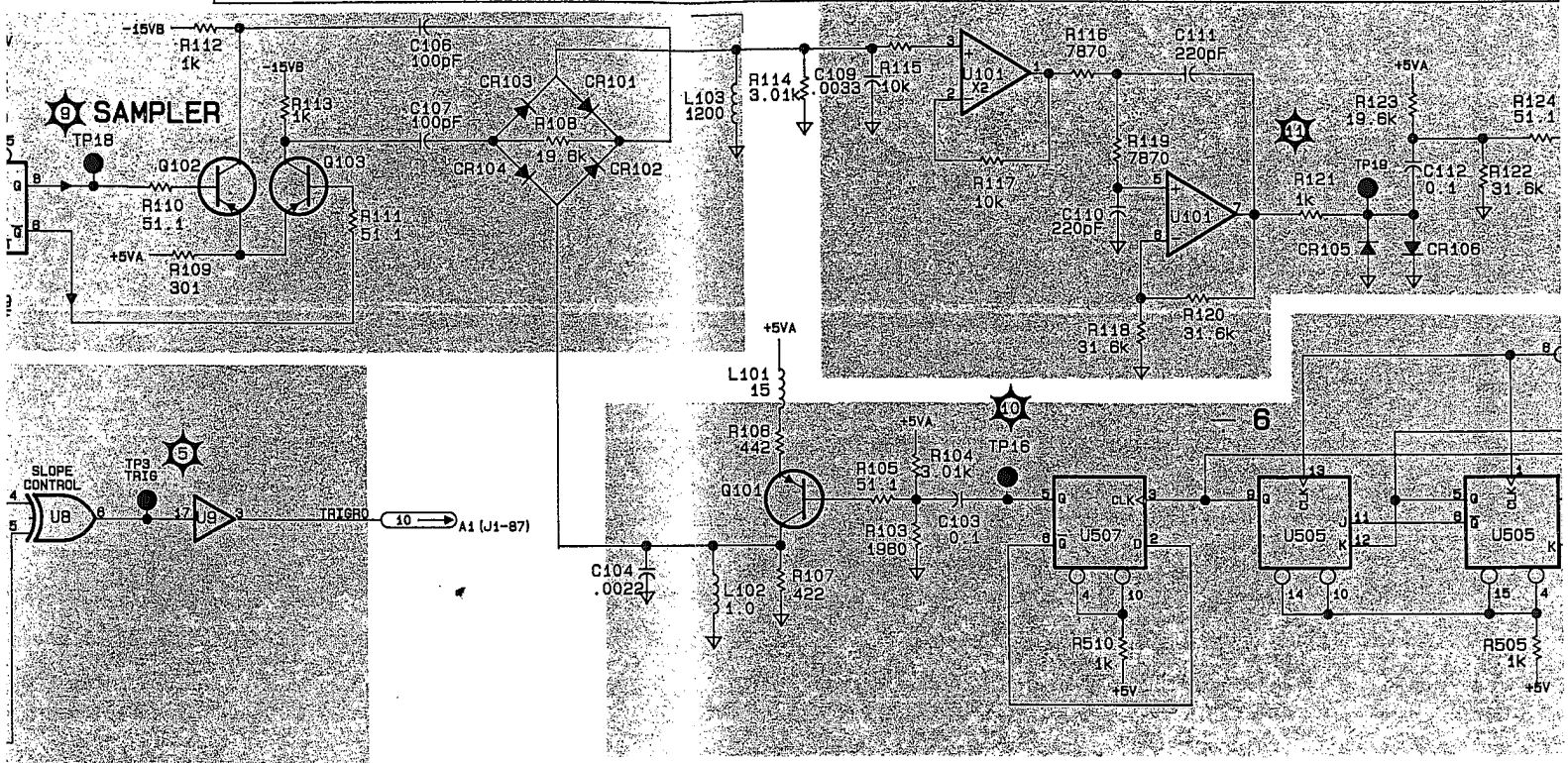
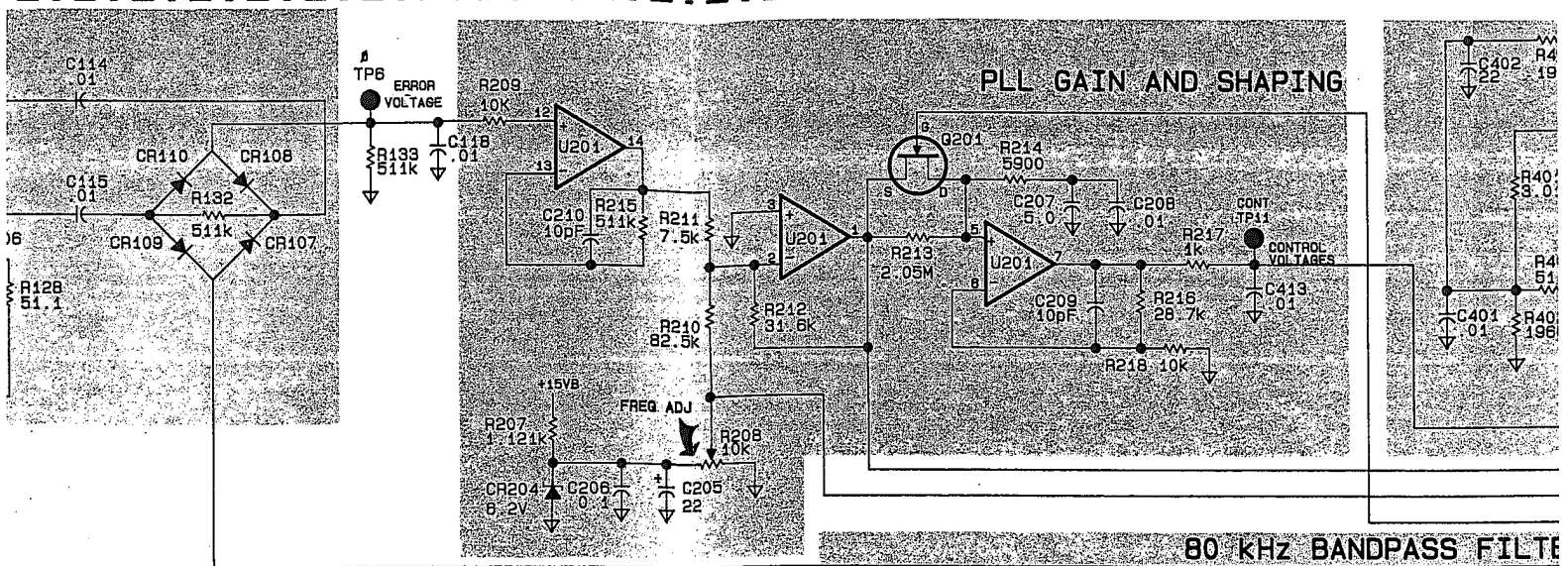


Figure 5-A31a Trigger Component Locator Revision A



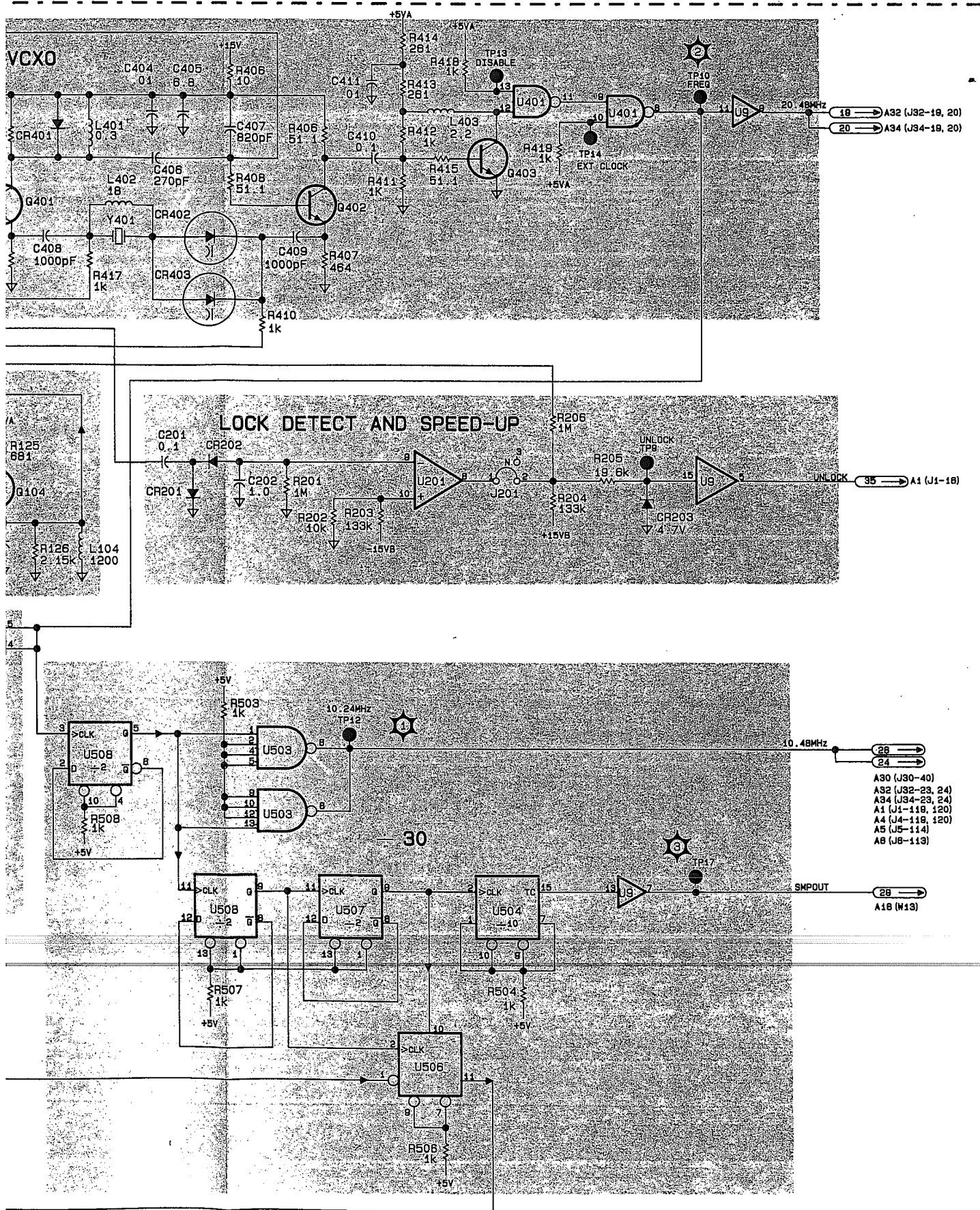


Figure 5-A31b Trigger Schematic Revision A

1. The following components are not on revision A:

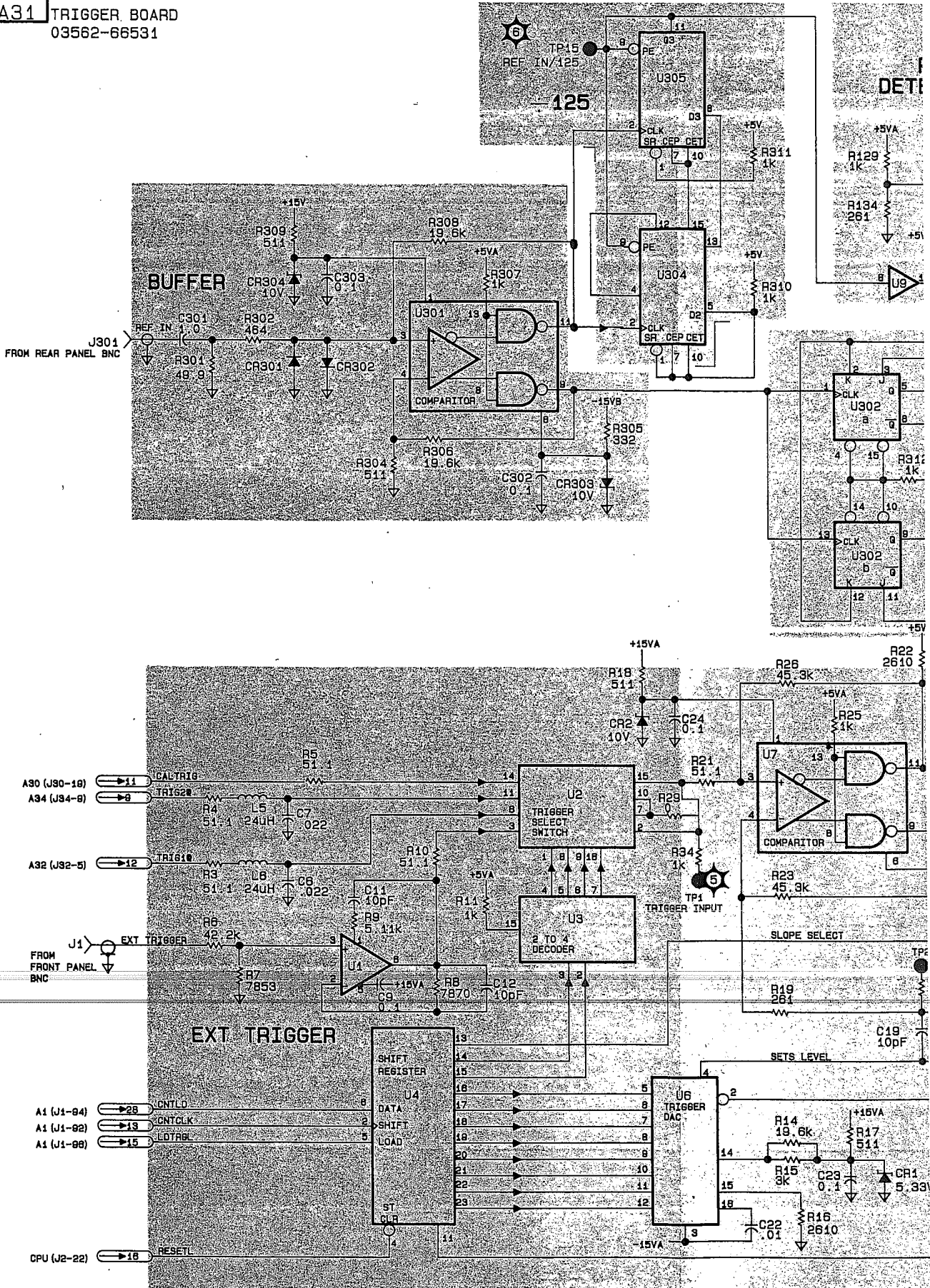
| Reference | HP P/N |
|-----------|-----------|
| R209 | 0757-0442 |
| R29 | 8150-3375 |
| TP15-19 | 1251-0600 |

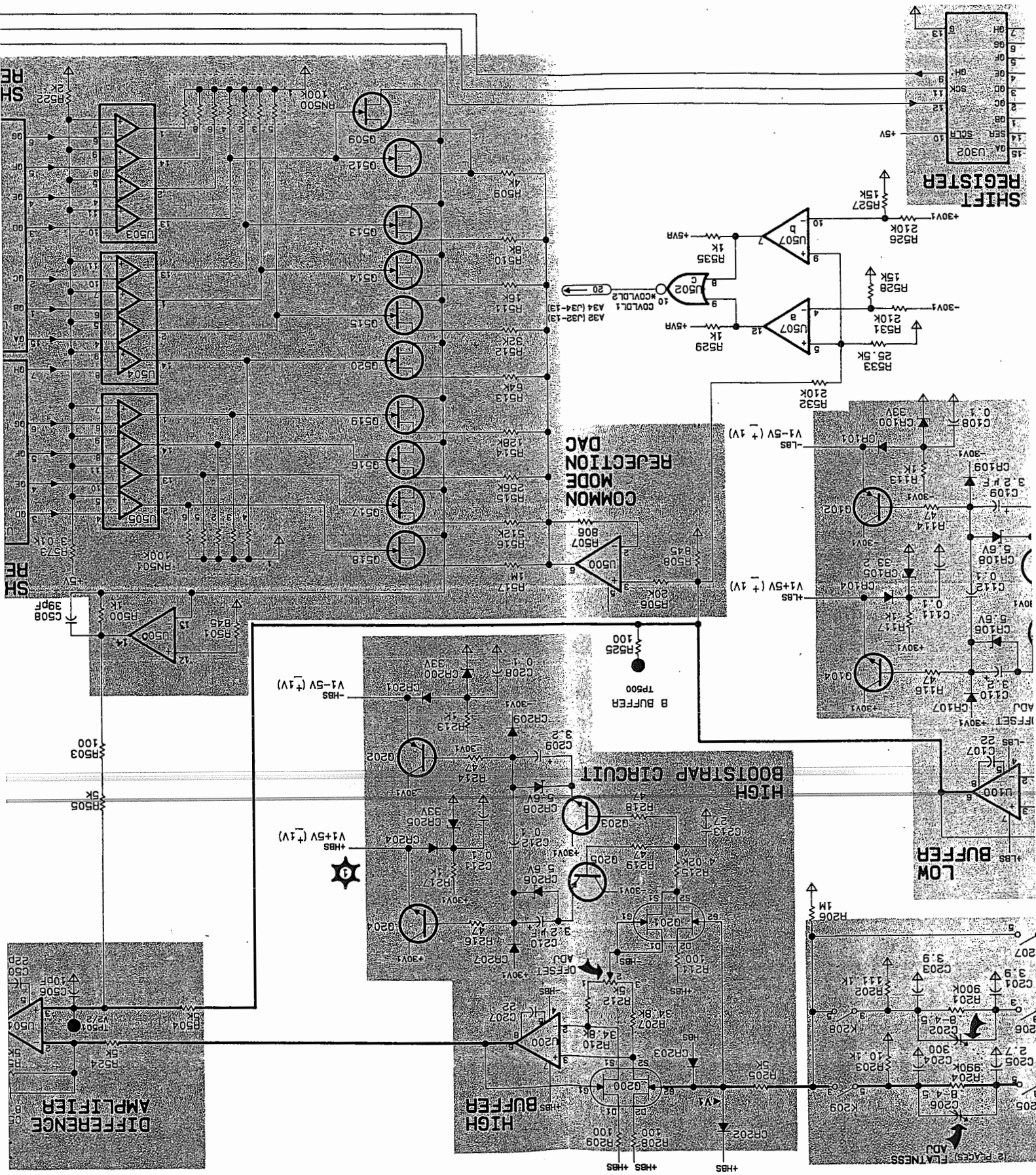
2. The following test locations on revision A correspond to the test points listed for revision B:

| Revision A Test Location | Revision B Test Point |
|-----------------------------|--------------------------|
| U305(11) | TP15 |
| U507(5) | TP16 |
| U9(7) | TP17 |
| U303(8) | TP18 |
| CR105 anode | TP19 |

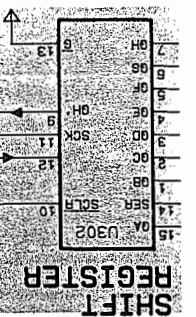
3. The pulse width of REF IN/125 (A31 U305(11), TP15) is different.

A31 TRIGGER BOARD
09562-66531





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COMMON MODE REJECTION DAC

HIGH BOOTSTRAP CIRCUIT

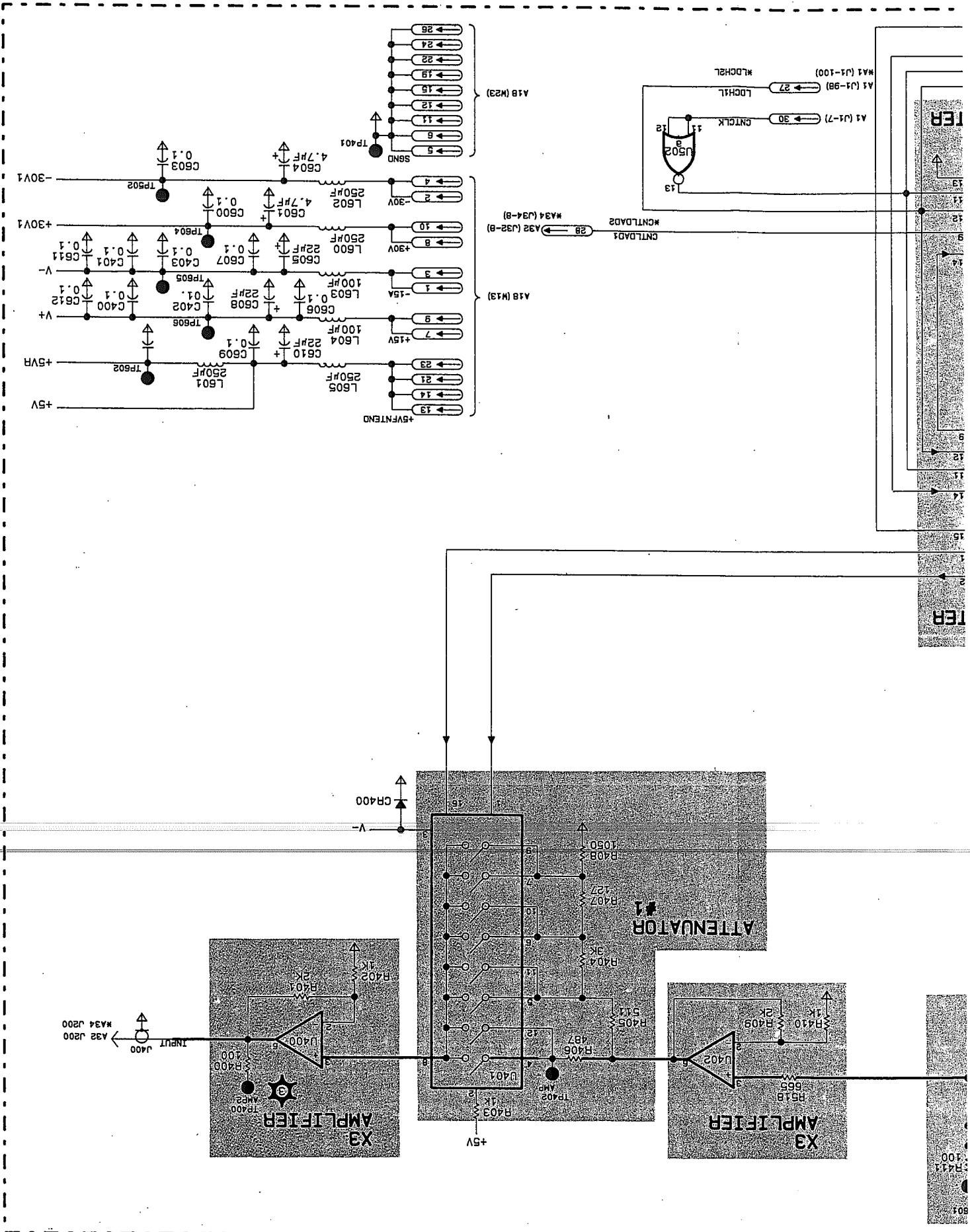
LOW BUFFER

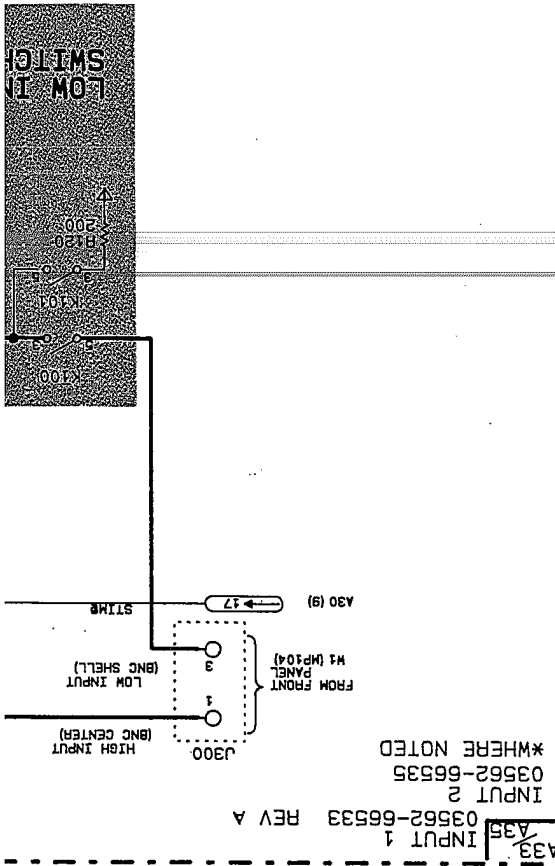
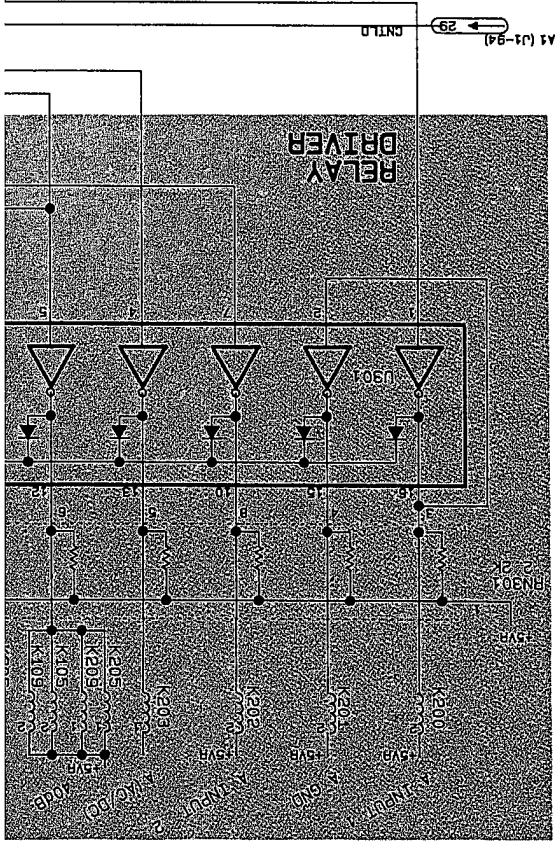
DIFFERENCE AMPLIFIER

HIGH BUFFER

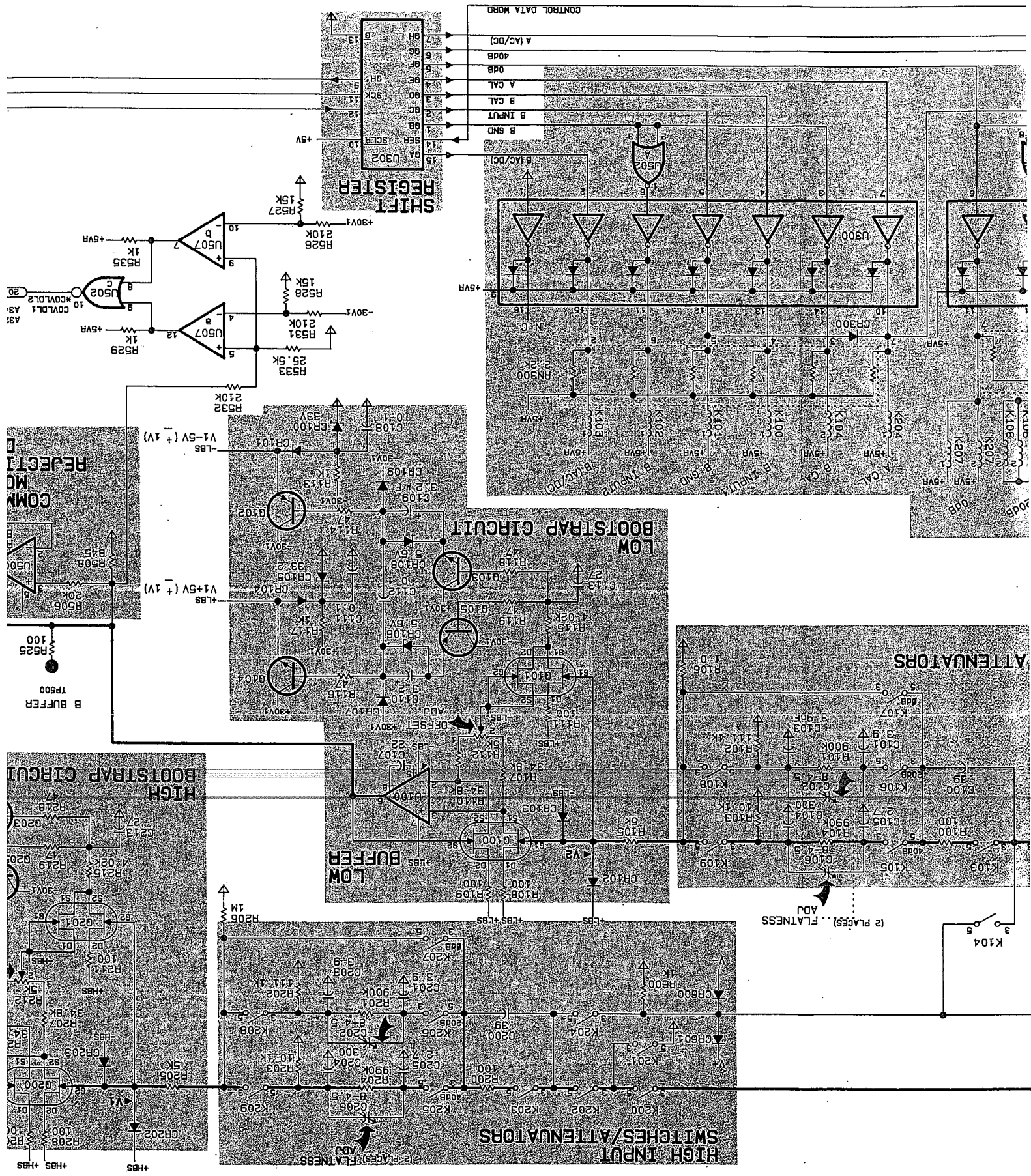
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Figure 5-A33b Input Schematic Revision A





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SECTION VI

CIRCUIT DESCRIPTIONS

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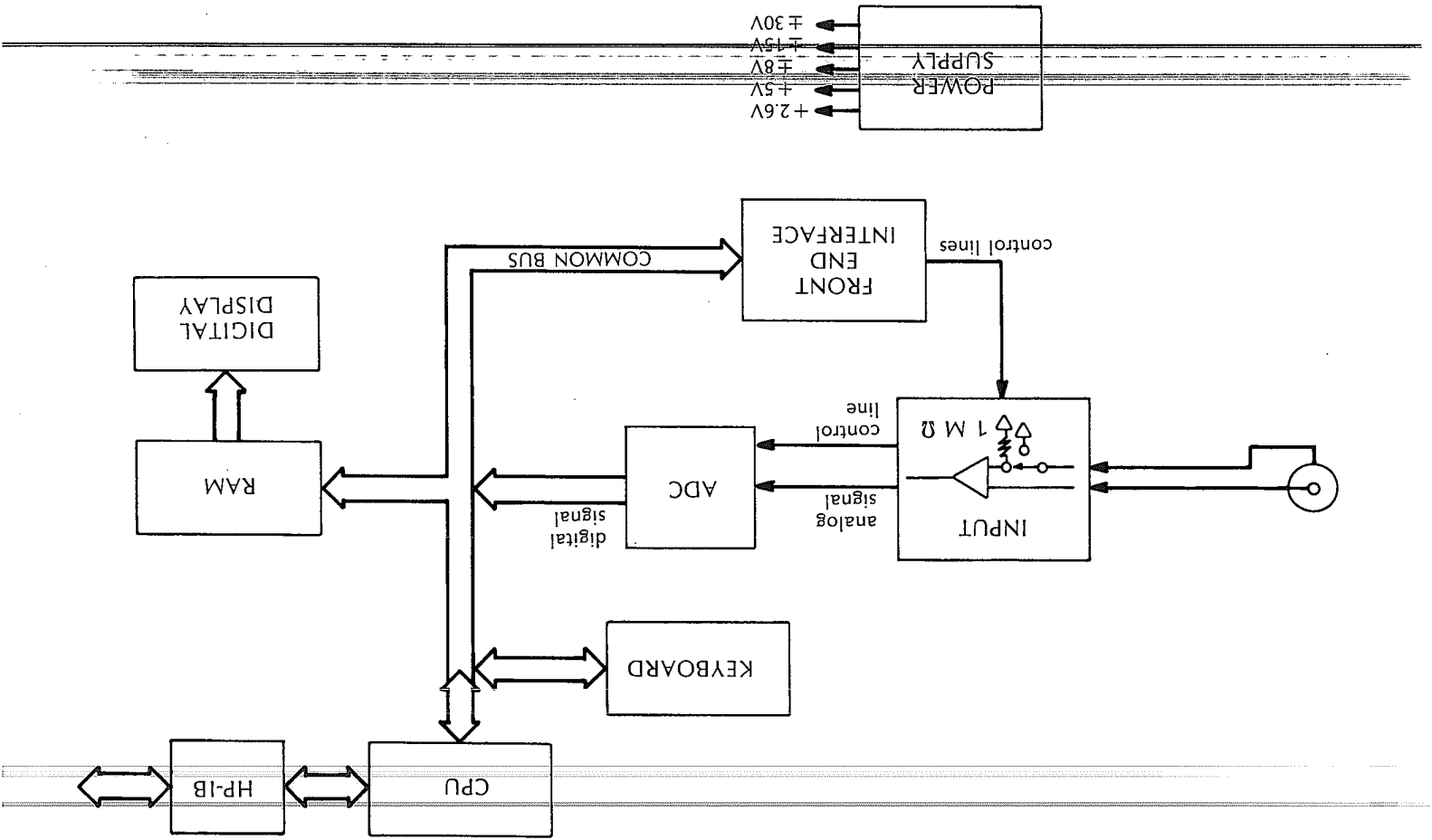
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Figure 6-1 Waveform Recorder



SECTION VI

CIRCUIT DESCRIPTION

6-1 INTRODUCTION

This section provides the overall instrument description and the detailed description of each assembly to a functional block. The overall instrument description describes the interaction of the HP 3562A's individual assemblies. Use this section to gain an overall understanding of the HP 3562A's operation. Use the circuit descriptions along with the schematics in Section IX to understand the operation of an assembly. Refer to the end of this section for a description of the signals that operate between assemblies.

6-2 OVERALL INSTRUMENT DESCRIPTION

To understand the operation of the HP 3562A, the measurement it makes must be understood. The HP 3562A uses the Fast Fourier Transform (FFT) algorithm to make frequency domain measurements. The FFT algorithm takes time domain data and operates on it to produce a frequency spectrum. Recall that the Fourier transform, of which the FFT is a special case, states that all time domain waveforms can be represented as a summation of sine waves in the frequency domain.

Since the FFT is a special case of the more general Fourier transform, it requires special data collection requirements in order to operate. All the numerical values associated with the FFT such as sample rate, number of frequency data points, time required for a complete conversion, and others are all related to powers of two. For example, a time record is defined to be N consecutive, equally spaced samples of the input where N is a multiple of 2. This time record is transformed as a complete block into a complete block of frequency lines. With a Dynamic Signal Analyzer we do not get a valid result until a full time record has been gathered.

Taking a simple look at an FFT dynamic signal analyzer, the hardware can be characterized as a digital waveform recorder with a great amount of computation power. This view is illustrated by the waveform recorder diagram in figure 6-1.

In the waveform recorder, the signal is fed into the input assembly for proper amplitude scaling and then converted to digital data by the ADC (Analog to Digital Converter) assembly. The input and ADC assemblies receive the signals to control the amplitude scaling and conversion from the front end interface. The front end interface is programmed directly from the CPU (Central Processing Unit). The digital output of the ADC is then stored into RAM and displayed. HP-IB is included for remote control and a keyboard for local control.

In figure 6-2, the instrument is expanded to include two separate input sections and ADCs. A source is also included to make network measurements. All measurement assemblies are connected to the CPU through a common bus.

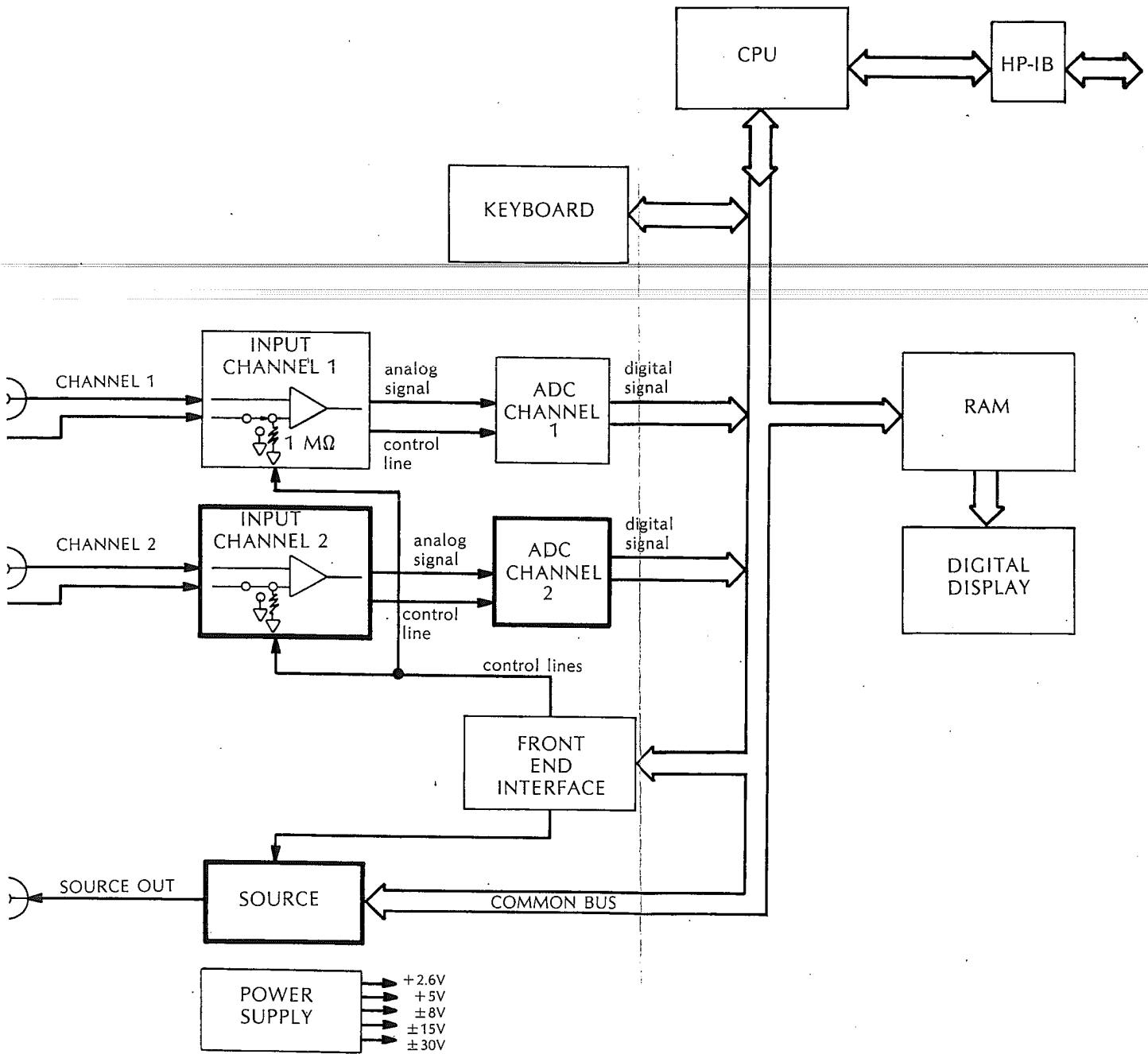


Figure 6-2 Two Channel Waveform Recorder with Source

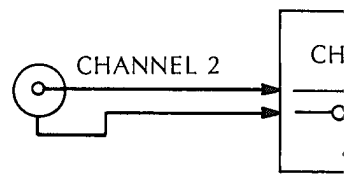
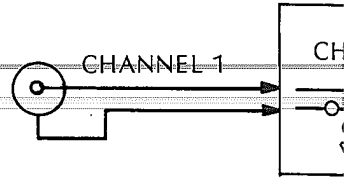
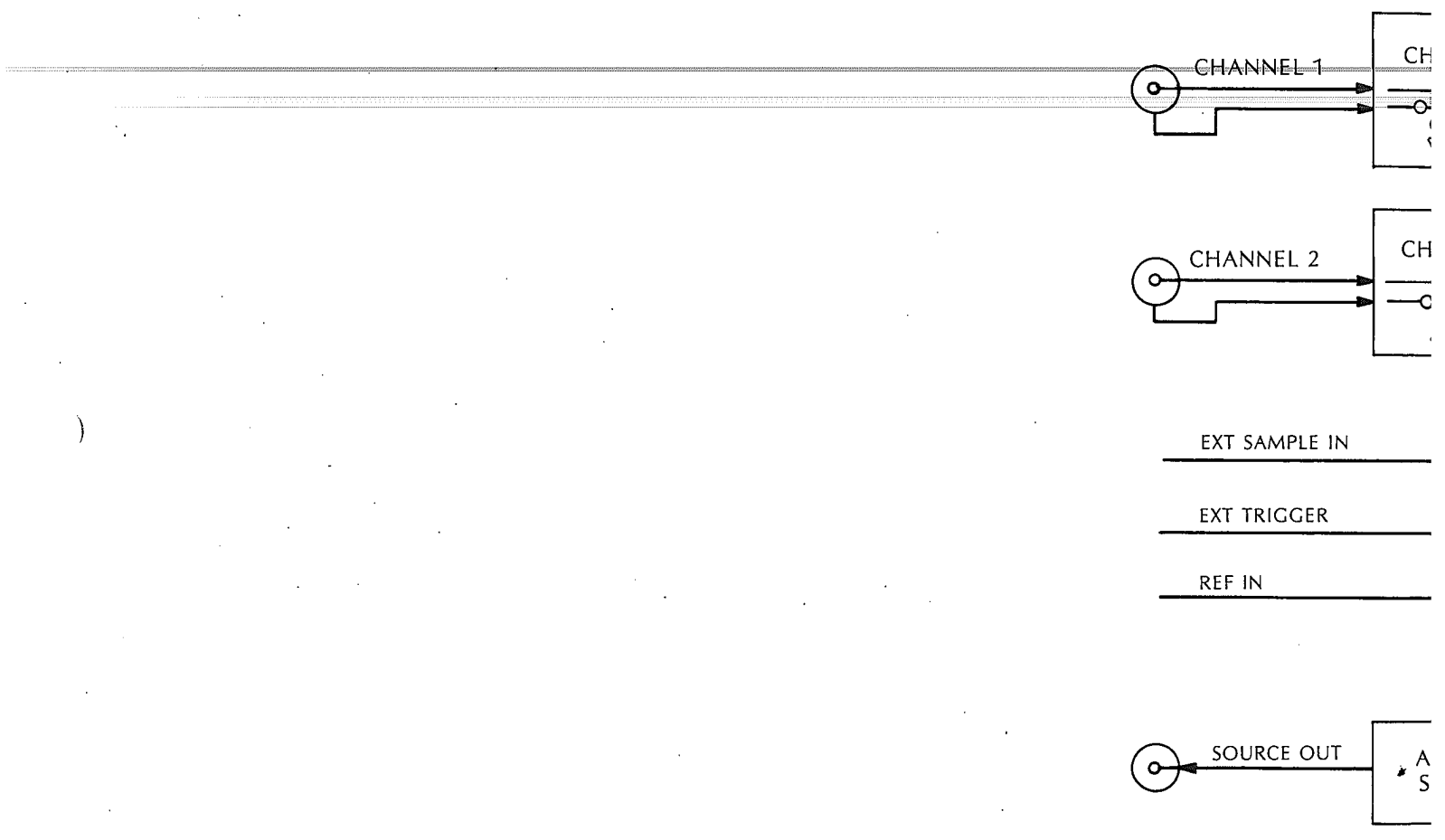
In figure 6-3, the two channel waveform recorder is converted into a two channel, fixed span, dynamic signal analyzer with source by adding the digital filter, FFT, and FPP (Floating Point Transform Processor) assemblies. The digital filter allows the user to look at the input spectrum with different resolution bandwidths and different shaped resolution bandwidth filters. The FFT assembly operates on the digital data out of the digital filter to provide a frequency domain representation of the input signal. The FFT data is stored in the RAM and displayed. The FPP is a bit slice processor which makes all the fast numerical calculations. A digital source assembly is added to simplify the CPU bus structure. This assembly controls all the digital settings for the input, ADC, and source assemblies. The CPU is now dedicated to supervising and controlling the operations of the instrument.

In figure 6-3, a trigger assembly was also added. The trigger assembly allows the instrument to operate in external trigger, external reference in, and external sample modes.

In figure 6-4, the analyzer becomes the HP 3562A by adding the local oscillator and program ROM assemblies. The local oscillator provides digital sine and cosine signals for the digital source and digital filter. The digital source distributes the digital sine to the analog source assembly for conversion to an analog signal. The digital filter uses the sine and cosine signals for zoom measurements. In a zoom measurement, a narrow frequency span is selected (<100 kHz) for a high resolution close-up shot of a frequency spectrum.

The program ROM assembly was added to give the instrument more program memory space. The common bus was split into two bus structures: the system data bus and the global data bus. The system bus is used to transfer commands from the system CPU to the other assemblies. The global bus is used to transfer measurement data between the assemblies.

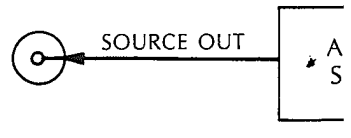
In the HP 3562A process control is distributed away from the system CPU. Each assembly has its own processor or state machine which controls its local operations. The system CPU tells each assembly which process to execute and monitors the overall functioning and data processing of the instrument.



EXT SAMPLE IN

EXT TRIGGER

REF IN



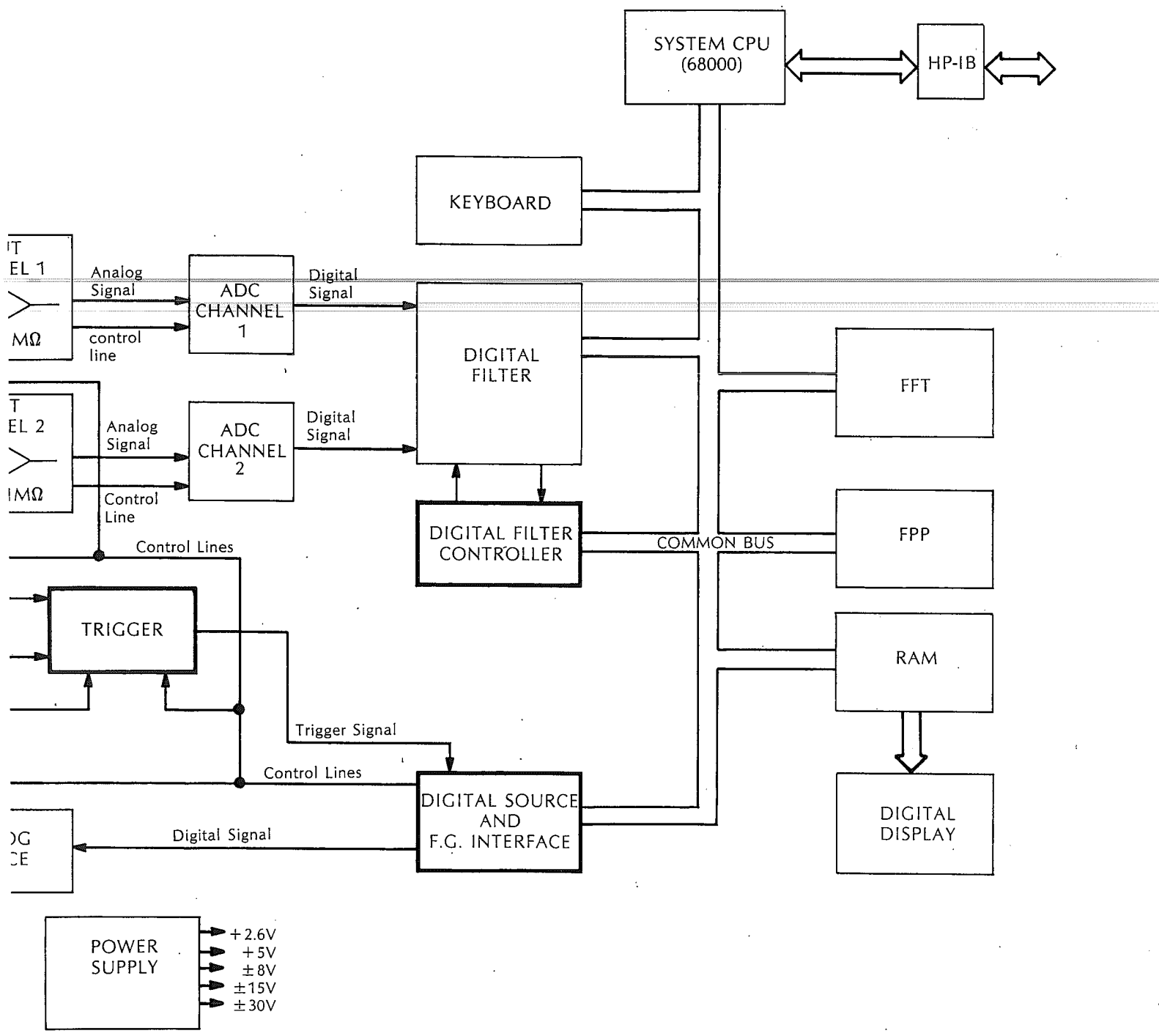
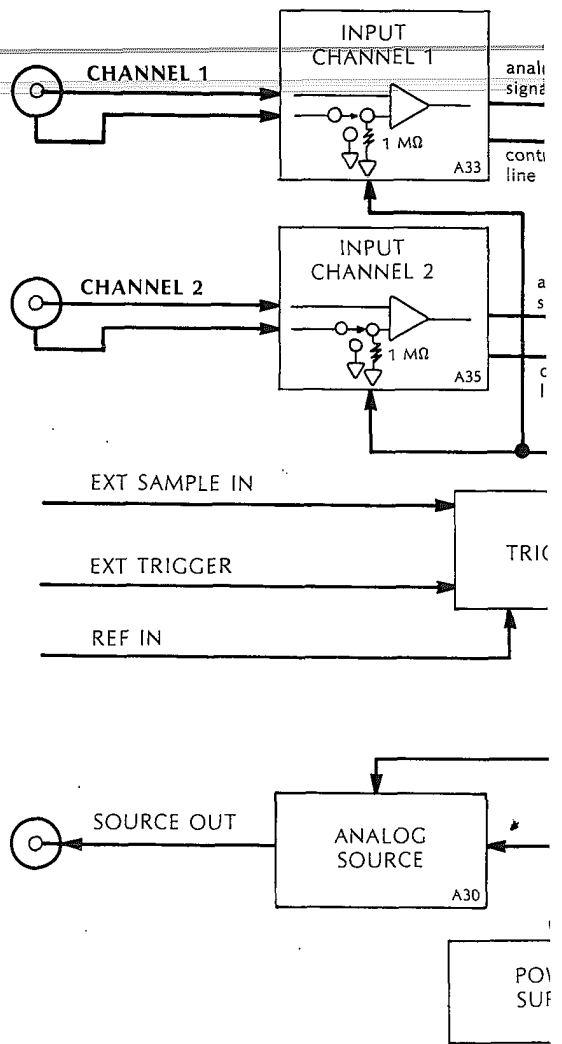


Figure 6-3 Two Channel Fixed Span Analyzer with Source



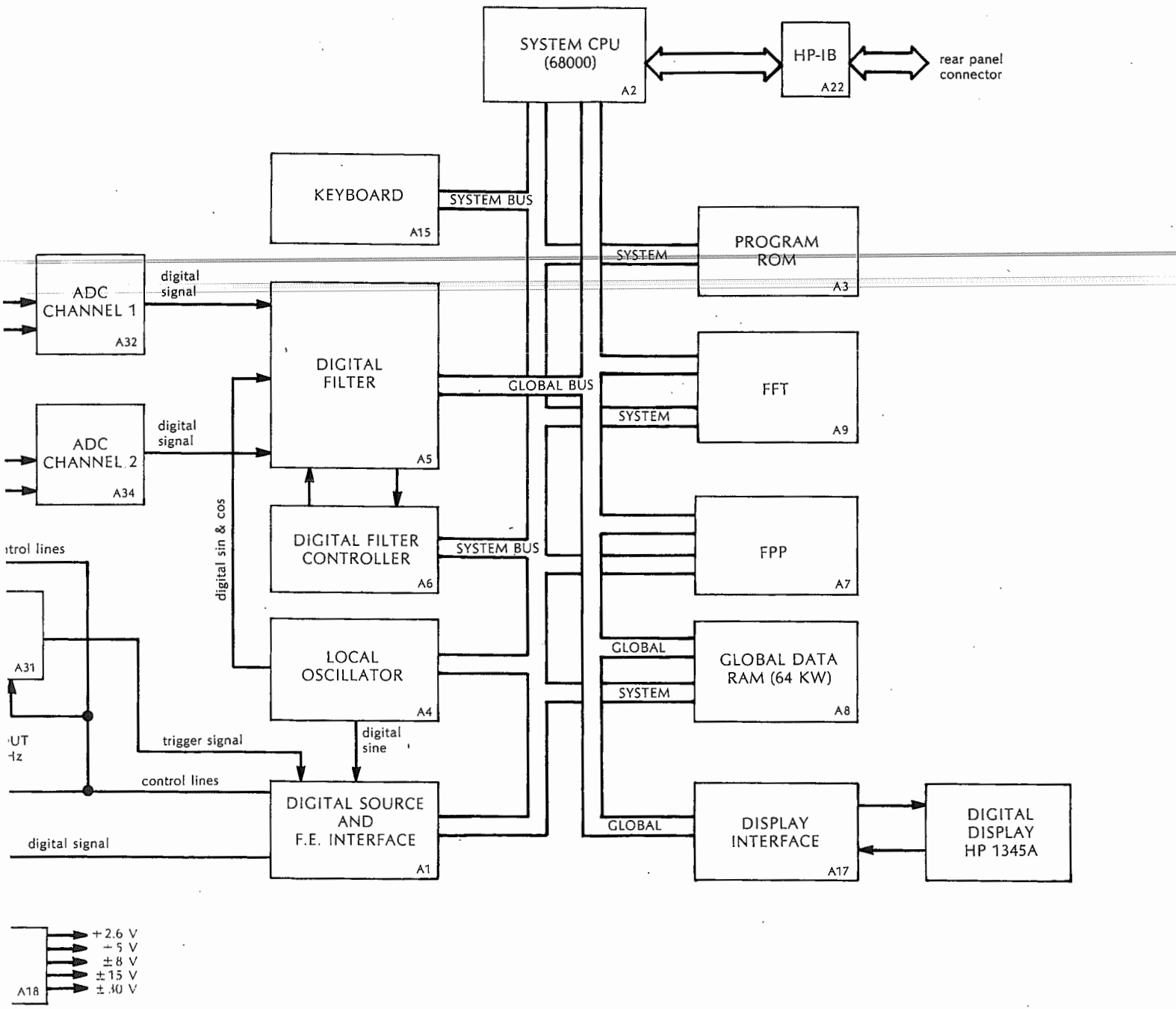


Figure 6-4 HP 3562A Block Diagram

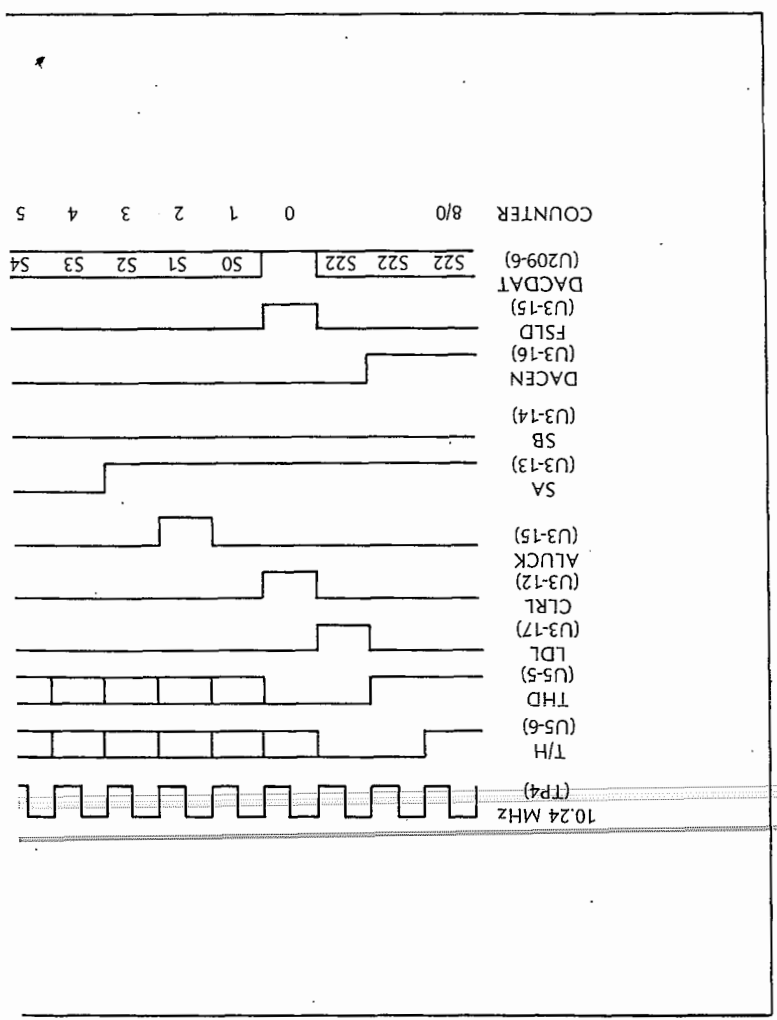
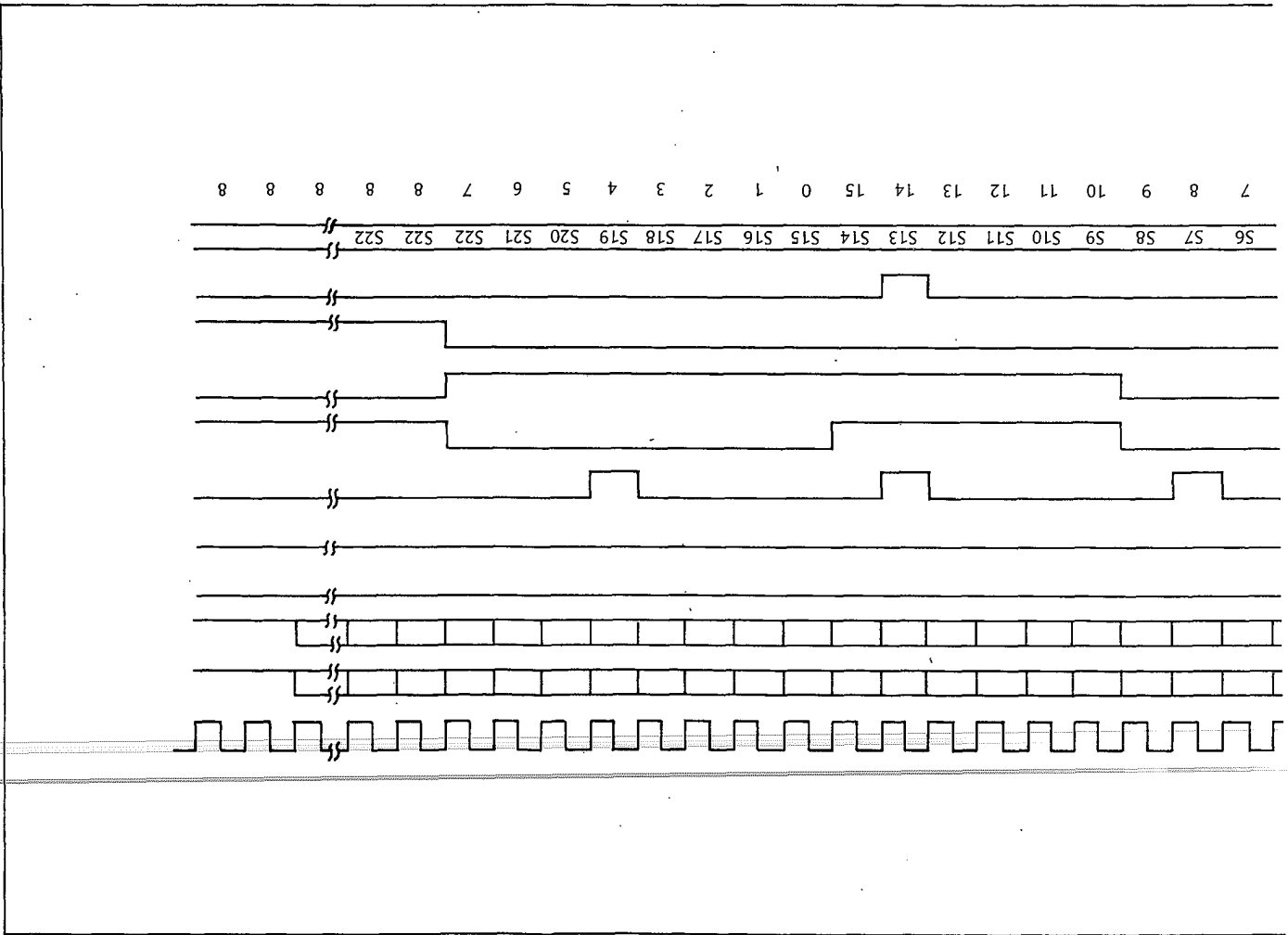


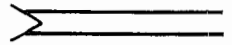
Figure 6-A1a Digital Source Timing



Sample
Clock
(SAMP)



DS
DATA
BUS



NOTE: FULL SPA
BASE BAI
MODE

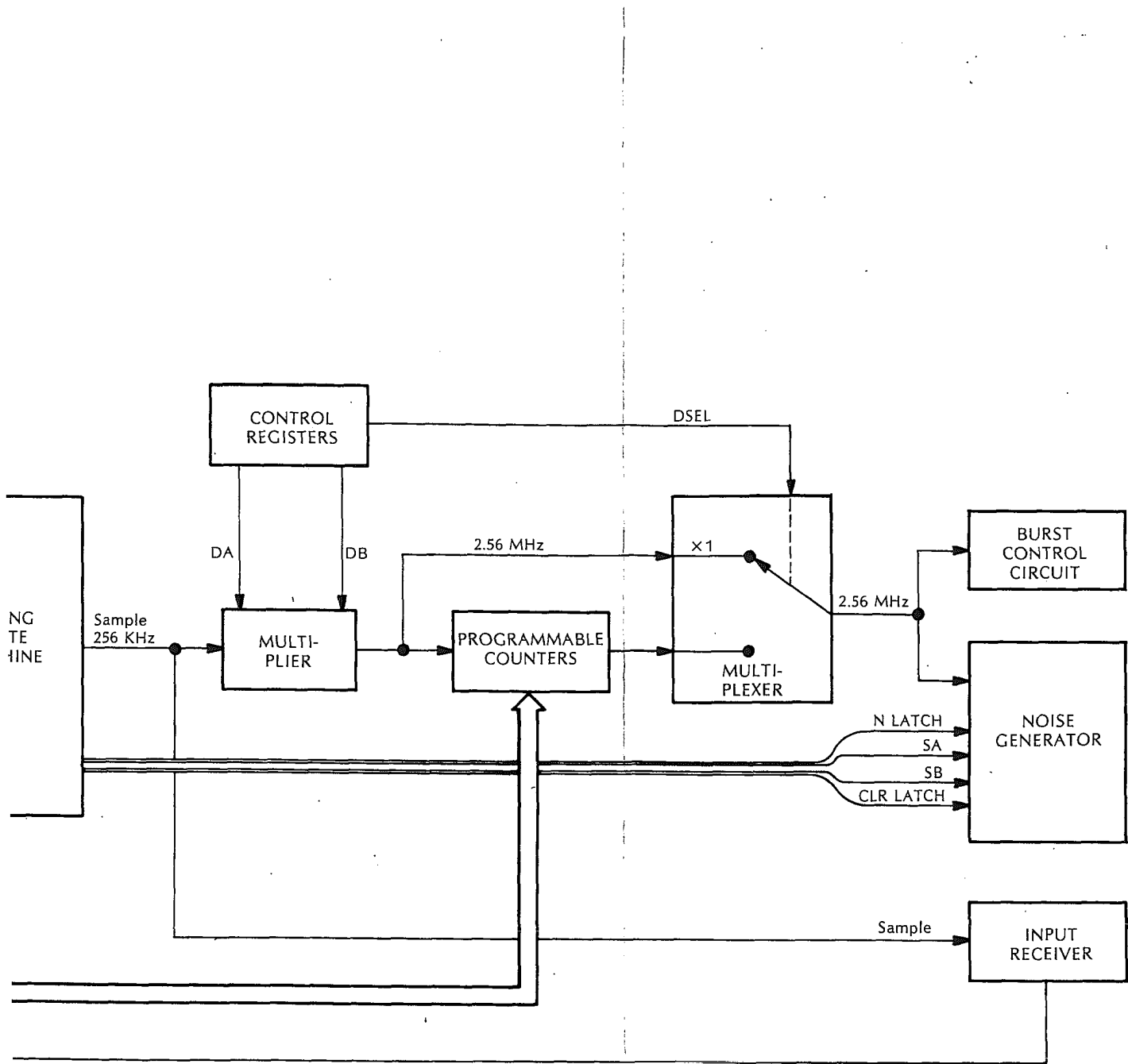


Figure 6-A1b Timing Control Circuit

Phase Resolution Circuit

(Refer to figure 6-A1c) The phase resolution circuit is used in external and internal triggered measurements. This circuit insures that the phase of a triggered measurement is accurate. Since the trigger moment does not always occur on a sample and hold edge (SAMP), there is a time delay and a phase error in the data. The phase resolution circuit counts the time between samples and the time between a sample and a trigger. It puts this information on the DS data bus which is read by the system CPU.

The ARML signal from the A6 Digital Filter Controller initializes the phase circuit and starts the trigger measurement process. This signal is only active when a triggered measurement is made. When the phase resolution circuit receives this signal, it sets BFST low and waits for the next sample clock (SAMP) from the ADC board. On the next sample clock the phase circuit starts counting and counts until a trigger signal (TRIGROL, REMTGL, SWTRIG, or BURSTRIG) is received. If another sample clock is received before the trigger signal, the phase state machine starts the count over and continues to wait for the trigger signal, clearing the counters each time a sample clock is received. When a trigger signal is received, the counters latch the first count into their output registers and continue counting until the next sample clock. On the next sample clock after the trigger signal, the second count is latched into the counters' output registers. BFST signal is then sent to the digital filter controller telling it to start taking data.

The phase resolution circuit now has a count between sample points and a count between the first sample point and the trigger point. When the RDPH1L or RDPH2L signal from the device decoder PAL becomes active, the phase resolution circuit puts the requested count on the DS data bus. The timing information is held until the next ARML signal is received or until it is read by the system CPU.

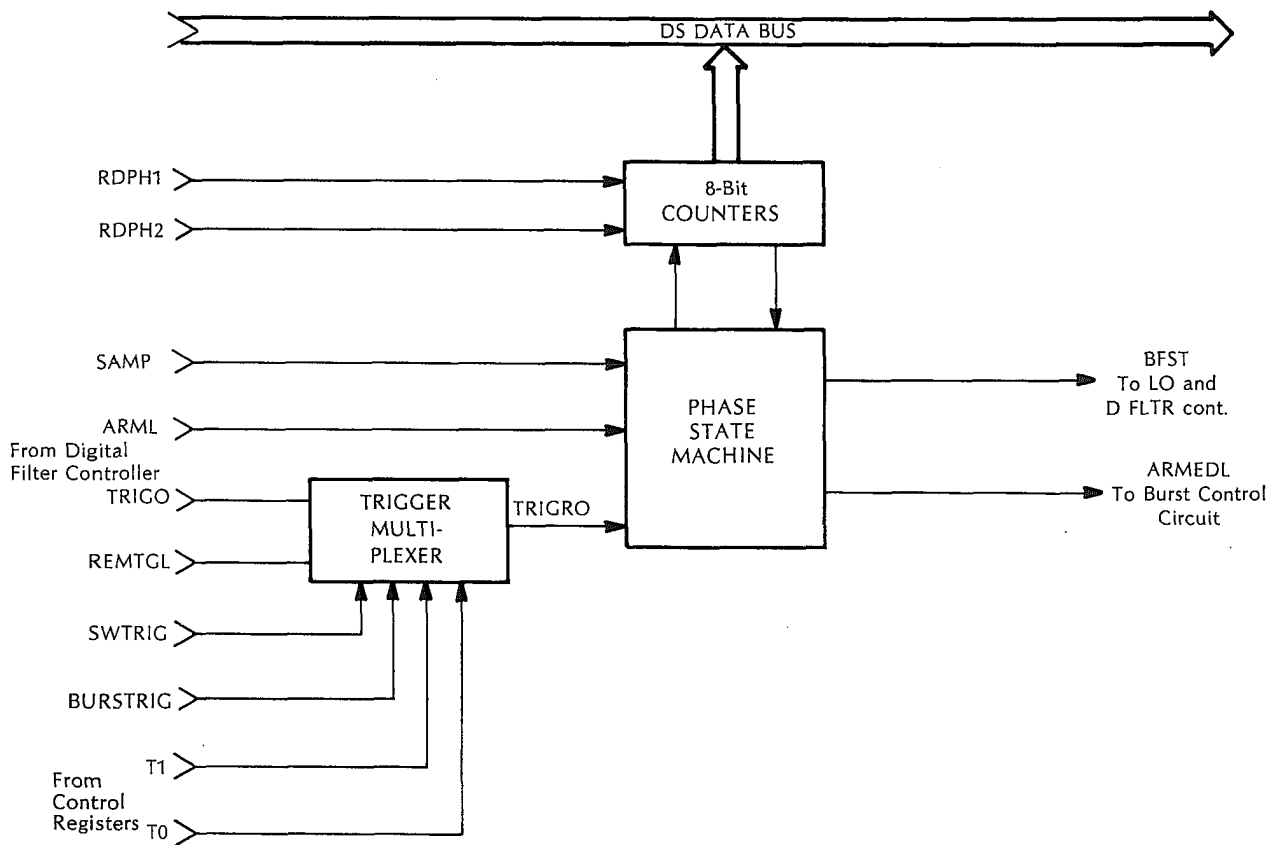


Figure 6-A1c Phase Resolution Circuit

Burst Control Circuit

(Refer to figure 6-A1d) The burst control circuit controls the burst length and generates the pulse signal (NCLK) to the local oscillator. It provides the gating signal (BURSTEN) that gates the analog source on and off during the burst and chirp modes. The burst control circuit also provides the SYNC OUT signal to the rear panel. This signal is high when the burst is on and is low when the burst is off.

When SELCNTRSL is active and WRITEL is low, a data word from the system CPU is latched into the programmable counters to set the time the burst is on and off. After the counters are programmed, the CONT signal from the control registers to the burst gate goes low. In freerun mode the freerun bit (U102-9) is set and the burst counters count blocks. The burst control circuit then gates the analog source on and off. In the triggered mode, the burst process starts when the ARMEDL signal from the phase resolution circuit goes low. The counters only count when ARMEDL is low. The ARMEDL signal also causes the burst control circuit to send the NCLK signal to the local oscillator. When NCLK is received by the local oscillator, the LO is set to the starting frequency of the burst. The local oscillator sends data (NDAT) to the digital source synchronized to NCLK. The data is processed by the LO input receiver and multiplier. DACDAT data is sent to the analog source at the same time the burst control circuit turns on the analog source.

After the burst is completed, the burst state machine checks to see if the ARMEDL signal is still active. If ARMEDL is active, the process repeats. All burst control operations are synchronized to the sample and trigger signals by the timing control circuit and the ARMEDL signal.

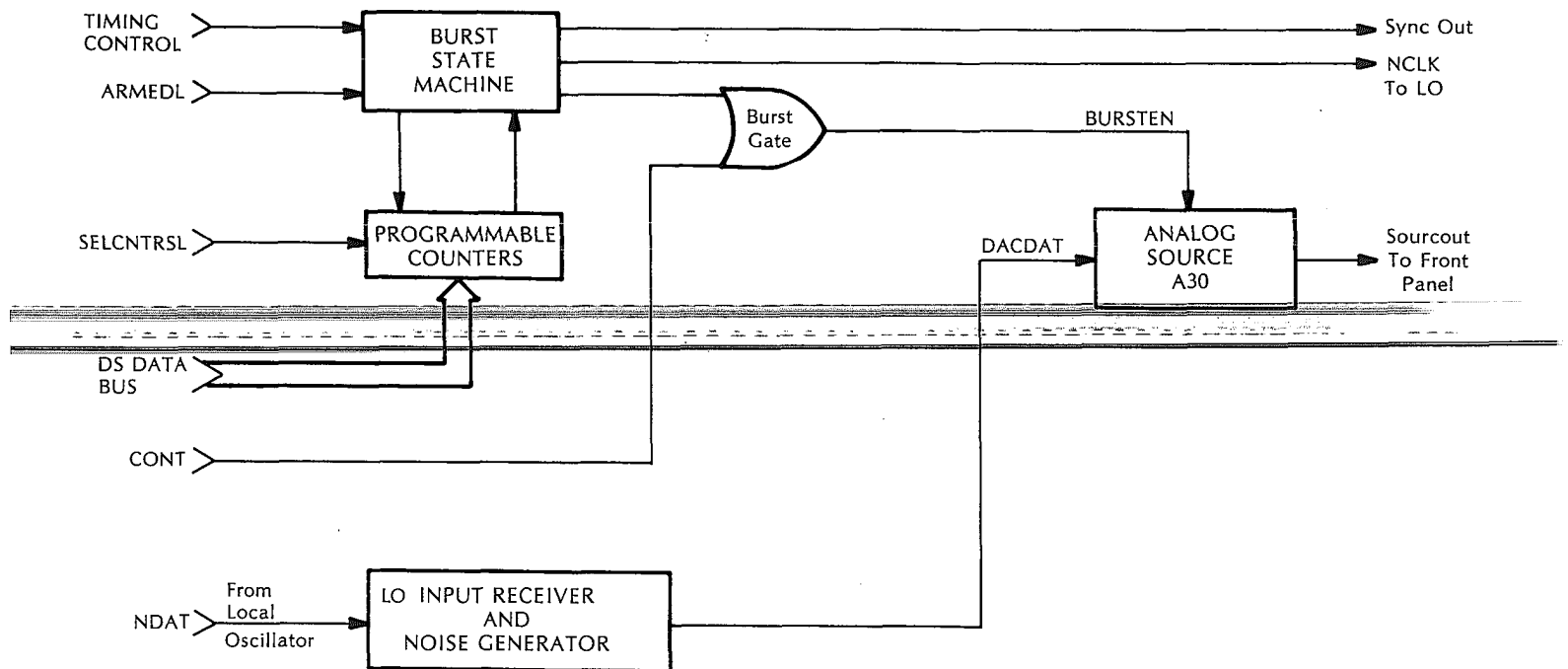


Figure 6-A1d Burst Control Circuit

LO Input Receiver

(Refer to figure 6-A1e) The purpose of the LO input receiver is to synchronize the local oscillator input data (NDAT) to the sample rate (SAMP). This is necessary because in external sample mode the LO data does not come at a regular rate. To synchronize the data to the sample rate, the LO input receiver shifts the serial data in and converts it to parallel data. The LO input receiver then clocks this data using the SAMPLE signal from the timing control circuit. After the data is synchronized, it is converted back to serial data and sent to the multiplier.

Multiplier

The multiplier is used to multiply the LO data by the noise and send it to the analog source. This is done with a parallel noise word and a serial LO word. This provides the means for frequency shifting the noise. When in zoom mode, the frequency shifting process shifts the center of the noise power frequency band to the frequency of the sine data from the local oscillator. When in chirp or sine mode, the output of the noise generator is forced to a constant so that LO data is passed through the multiplier with only an inversion.

Noise Generator

The noise generator produces a binary random sequence that is used for band-limited random noise and burst noise signals. The noise generator is a 32-bit shift register with feedback to generate a pseudorandom sequence. This sequence is multiplied by a squared analog random signal. This randomizes the feedback of the shift register. The analog random noise is a zener diode biased so that it is barely on and is thus noisy. The output of the zener diode is amplified until it is at a high enough level to square up. The noise filter is used to produce noise with necessary bandwidth. The bandwidth is determined by the rate that the noise is shifted into the noise filter. The rate the noise is shifted into the noise filter is determined by the effective sample rate.

The output of the noise generator is parallel loaded into the multiplier and mixed with the data from the local oscillator. This process is controlled by the timing state machine.

Internal Signal Descriptions

ARMEDL

ARMED

Active Low

Signal from the phase resolution circuit to the status register and the burst control circuit. ARMEDL goes low on the first sample point following the ARML signal. It goes high after the trigger point.

BRST

BURST RESET

Used to abort a burst in the burst control circuit. When low BRST causes the A30 Analog Source to output zero if the instrument is in the burst mode. This signal should be high for normal operation.

- BUSYL** PHASE COUNTERS BUSY
Active Low
This signal from the phase counters goes low after an ARML has occurred and goes high after the counters finish counting. BUSYL is sent to the status registers.

- C10FSE** 10x EFFECTIVE SAMPLE RATE CLOCK
In baseband mode this clock occurs at 10 times the effective sample rate.

- CHIRPL** CHIRP
Active Low
When this control signal is low, the sinusoidal signal from the A4 Local oscillator is passed through the digital source board without mixing with the random noise.

- CNTRL BUSY** CONTROL BUSY
This is the digital source handshake signal for sending the control data word (CNTLD). If it is "1", the digital source is sending the word. If it is "0", the digital source is ready to send another control data word. This signal is from the control register to the status registers.

- CONT** CONTINUOUS
When this control signal is high, the digital source keeps the A30 Analog Source enabled. When low, the analog source is gated by the burst control circuit.

- CONTROL** CONTROL
Signal from the device decoder PAL that latches the control word from the DS data bus.

- COUNTENL** COUNT ENABLE
Active Low
ARML starts the phase state machine which sets sets COUNTENL low and the counters start counting.

DA, DB DA, DB

~~These two signals from the control registers set the effective sample rate multipliers.~~

| Example Frequency Spans | DA (U1-3) | DB (U4-12) | MULT (U1) | DSEL (U101-2) |
|-------------------------|-----------|------------|-----------|---------------|
| 1 kHz | 0 | 0 | x 1 | 1 |
| 3.125 kHz | 0 | 1 | x 2 | 1 |
| 10 kHz | 1 | 0 | x 5 | 1 |
| 100 kHz | 1 | 1 | x10 | 0 |
| 20 kHz | 1 | 0 | x 5 | 0 |
| 50 kHz | 0 | 1 | x 2 | 0 |

DESTA DESTINATION A, DESTINATION B
DESTB These control signals determine where the serial control word (CNTLD) is sent.

| DESTA | DESTB | Assembly |
|-------|-------|-----------------------------------|
| 0 | 0 | A30 Analog Source (LDSRC) |
| 0 | 1 | A31 Trigger (LDTRG) |
| 1 | 0 | A33 Channel 1 & A32 ADC 1 (LDCH1) |
| 1 | 1 | A35 Channel 2 & A34 ADC 2 (LDCH2) |

DMID MIDDLE DATA
 DMID is the A4 Local Oscillator input signal before the multiplier. This signal goes to the status register.

DSA START DSA START, DSA STOP
DSA STOP These control signals are used for the signature analysis start and stop bits.

DSEL DIVIDER SELECT
 Signal from the control registers that selects the multiplied sample rate or the divided sample rate for the burst control circuit and the noise generator. A high selects the divided sample rate. (Refer to DA, DB for chart)

ENLDL ENABLE LOAD
 Active Low
 Enable load from the control registers determines when the serial command word (CNTLD) is sent to the A30 Analog Source, the A31 Trigger, The A33, A35 Input boards, or the A32, A34 ADC boards.

FREERUN FREERUN
 Signal from the control registers. When in the freerun mode, this signal is high.

LDCH1 LOAD
LDCH2 These signals are used to monitor the load pulses to the analog assemblies.
LDTRG
LDSRC

NSR NOISE SHIFT REGISTER DATA
 This is the data that is shifted into the noise filter. In normal operation this includes the addition of the analog random noise. The analog random noise is disabled in the test mode.

SELCNTRSL SELECT COUNTERS
 Active Low
 This signal from the device decoder PAL along with DSA1 and DSA2 enables the counters for programming.

STATUSL STATUS
 When STEST is active, the digital source is in the self-test mode. STEST is from the device decoder PAL to the test register. STEST latches the self-test data word into the test register.

SWARML SOFTWARE ARM
Active Low
Signal from the control registers that overrides the software arming of the phase counters and the buffer start. This signal is used for self-test and should be high in normal operation.

SWTRIG SOFTWARE TRIGGER
If SWTRIG is selected with T1 and T0, a trigger occurs on the low to high transition of the SWTRIG signal.

T0 TRIGGER SELECT
T1 T0 and T1 select where the trigger signal will come from.

| T0 | T1 | Trigger Source |
|----|----|----------------------------|
| 0 | 0 | A31 Trigger Board (TRIGRO) |
| 0 | 1 | HP-IB Trigger (REMTGL) |
| 1 | 0 | Software Trigger (SWTRIG) |
| 1 | 1 | Source Trigger (BURSTRIG) |

The system CPU may initiate a trigger by setting SWTRIG low, then high.

T10M TEST 10 MHz CLOCK
In the digital source self-test mode this signal becomes the 10 MHz clock, the LO serial data clock, and the serial data shift clock.

TDREQ DATA REQUEST
This signal is used when in the self-test mode as the data request line.

TEST TEST
This signal enables the self-test signals to be multiplexed into the data paths and clock lines. This signal must be low for the assembly to function in the normal mode.

TLODAT TEST LOCAL OSCILLATOR DATA
This signal is used as the LO serial data for the self-test instead of using LO data.

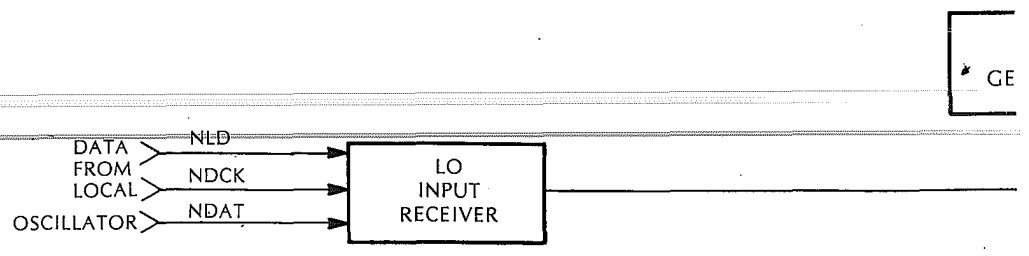
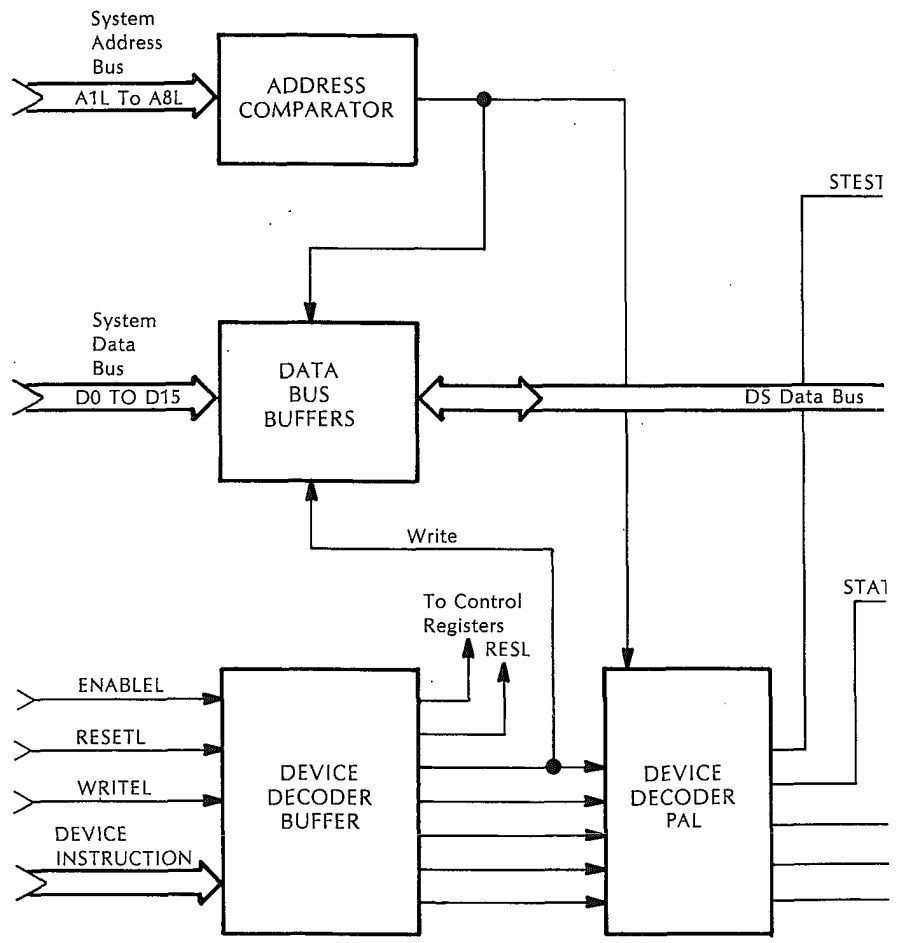
TLOLD TEST LOCAL OSCILLATOR LOAD
This signal is used in testing the LO input receiver.

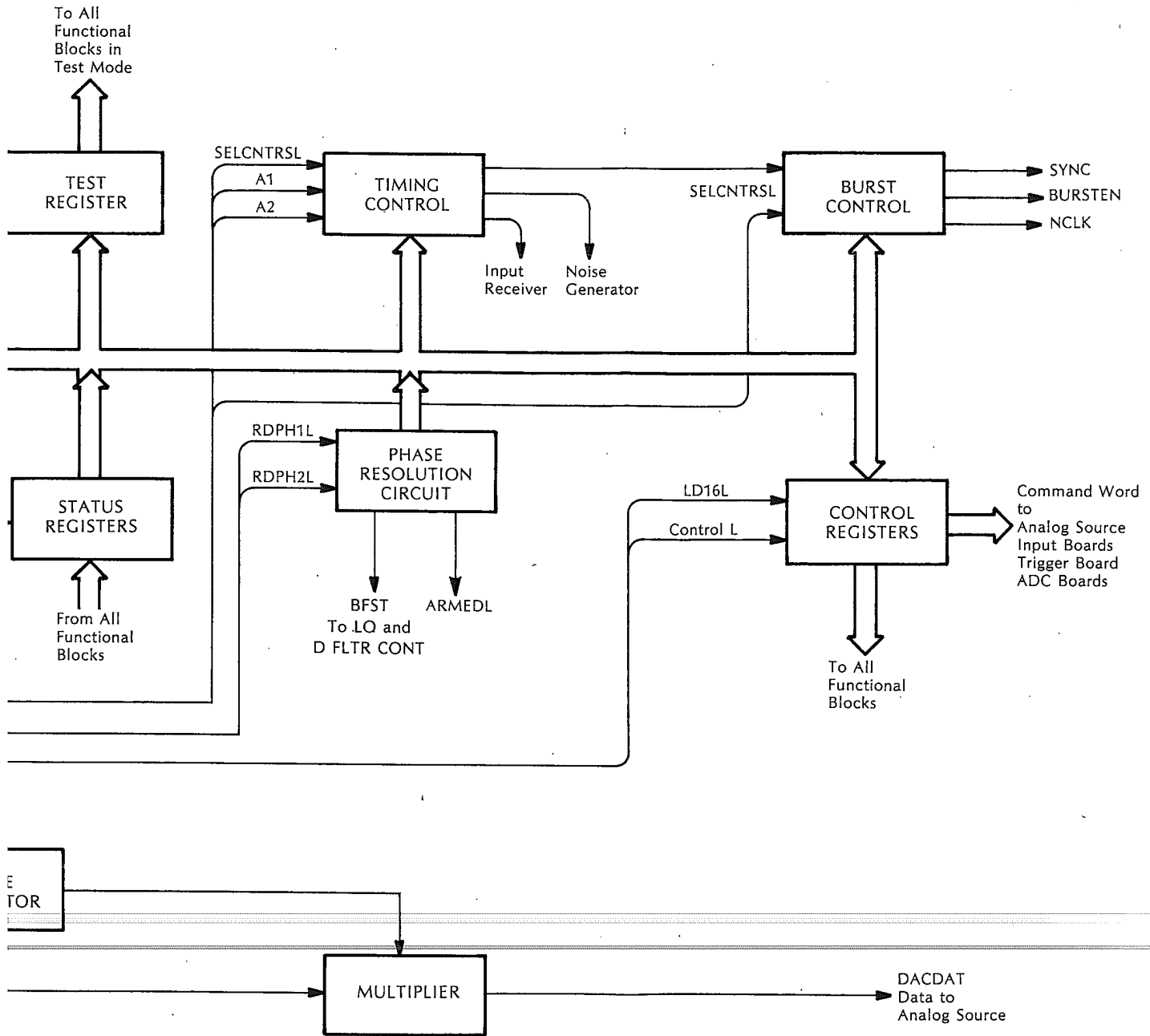
TRIG TRIGGER
When TRIG goes high, the phase state machine strobes the current count of the phase counters into the counters' output registers.

TRIGGERED TRIGGERED
Signal from the phase resolution circuit to the status registers. When the ARML signal is received, TRIGGERED goes low. When a trigger is received, TRIGGERED go high. This indicates the trigger has occurred.

TTH TEST TRACK/HOLD
In the self-test mode this signal becomes the sample clock.







6-A1e Digital Source Block Diagram

6-4 A2 SYSTEM CPU/HPIB

Refer to Figure 6-A2 for this discussion. The processing unit of the A2 System CPU (Central Processing Unit) is a MC68000 16-bit microprocessor. The function of the system CPU is to tell each assembly which process to execute and monitor the overall functioning and data processing of the instrument. The programs stored in memory (monitor memory) on the A2 System CPU and some of the programs on the A3 program ROM help the system CPU perform this function. The monitor memory is made up of ROM, RAM, and nonvolatile RAM (which is maintained by a battery backup).

The HP-IB interface is included on the A2 CPU assembly. This allows for direct memory access and a HP-IB device to talk directly with the system processor.

The system CPU is the system address and data bus master of all communications on the system bus. Interactions between the assemblies are maintained by using 16 bidirectional data lines (D0L to D15L), 23 address lines (A1L to A23L), and 17 system control lines. An assembly attracts the attention of the A2 System CPU by using interrupt lines IRQT2L to IRQT6L. The priority interrupt encoder determines when an assembly can interrupt the system processor. When interrupted, the system CPU processes the interrupt and sends the next command to the assembly. After receiving the information, the assembly handshakes with the system CPU. Most assemblies use the asynchronous signal Data Transfer Acknowledge (DTACKL) to handshake with the system CPU. The exception is the A4 Local Oscillator. It uses the synchronous signal Valid Peripheral Address (VPAL) to handshake with the system CPU.

Off-Board Operations

The system processor uses the system bus control, system address drivers, system data buffers, and handshake circuits to get programs stored in the A3 Program ROM and to command assemblies to perform operations. When the system CPU needs to load an instruction, it asserts the read/write line (WRITEL) low and puts the address for the A3 ROM assembly and the address of the needed instruction on the system address bus. The A3 ROM decodes the address lines, returns the DTACKL to the system CPU, and puts the requested instruction on the system data bus. The system CPU then loads the instruction from the system data bus.

The following happens when the system CPU commands an assembly to perform an operation:

1. The system processor puts the address for the assembly on the system address bus and the address decoder activates the proper control lines.
2. The address decoder selects the appropriate monitor memory location where the command is stored and the command is put on the system data bus:

(To command the A7 Floating Point Processor, the system CPU loads a command stack into the A8 Global RAM before addressing the assembly. The data transferred on the system data bus is the starting address of the command stack in global RAM.)

3. The assembly recognizes it has been addressed and returns a handshake signal (DTACKL or VPAL).

4. The system processor asserts upper data strobe (UDSL) and/or lower data strobe (LDSL) signals to transfer byte data (8 bits) or word data (16 bits). The assembly being addressed determines whether UDSL or LDSL are used.
5. The assembly reads the system data bus and performs the operation.
6. When the assembly has finished the operation, it sends the system CPU an interrupt (IRQT).

On-Board Memory Operations

The system processor controls the monitor memory by asserting the address lines to the memory and the address decoder. The address decoder decodes these lines to select the ROM or RAM memory pair to be accessed. Next, the system processor asserts the upper data strobe (UDSL) or lower data strobe (LDSL). UDSL selects the upper memory and LDSL selects the lower memory. Both UDSL and LDSL are asserted at the same time if a 16 bit word is used. The read/write (R/WL) signal is also decoded and determines whether a read or write operation to memory is to occur. For the monitor memory to communicate with another assembly on the system data bus, the address decoder must activate SBUSENL, placing the system data bus in the input/output mode.

Interaction Between the A2 System CPU and the A8 Global RAM

The system CPU shares the global bus with all other devices to access the global RAM. For this operation, the system CPU has 16 address lines, 16 data lines, and 4 control lines connected to the global bus. The system CPU's global address bus connection (GA1L to GA16L) is an extension of the lower 16 bits of the CPU address bus. When the system CPU addresses a global RAM memory location, the system CPU's address decoder asserts the global request (GLRQTL) line to the handshake circuit. The handshake circuit sends the memory request (MR68L) to global RAM. The global RAM returns a memory grant (MG68L) when it gives bus control to the system CPU. This memory grant signal clears the memory request signal (MR68L) and enables the assertion of the global read/write signal (GR/GWL). When the system CPU has a write request, the assertion of GR/GWL causes memory data to be written onto the global data bus. For a read request, the global bus receivers latch the incoming data when the global data strobe (GDSL) signal is received.

Interrupt Circuit

An interrupt is sent when an assembly has information for the system CPU, finishes a process, or requests service. For example, the keyboard sends the system CPU the IRQT2L signal when a front panel key is pressed. When an assembly needs to communicate with the system CPU, the assembly asserts its interrupt request line (IRQT2L to IRQT6L). The priority interrupt encoder informs the system processor which assembly has interrupted it. For a description of the interrupt request lines, refer to paragraph 6-8, "Signal Descriptions".

Programmable Timer Module

The programmable timer module is an internal time base generator, clocked by the ENBL clock from the system processor. This timer is used for function time outs and to maintain relative time intervals. This module contains three clocks which get addressed by signals A1 to A3. The clocks are loaded and read by the system processor using the CPU data lines D0 to D7. A clock is enabled by the program timer module signal PTML. When the program timer module clock finishes counting, the interrupt request IRQ7L is generated.

Bus Time Out

When a system processor bus cycle is initiated, the bus time out ripple counter is started and runs until either the handshake is completed (DTACKL or VPAL is received) or the counter reaches its terminal count. If the timer reaches the terminal count of 32 μ s before the handshake is completed, the bus error line (BERRL) to the system processor is asserted to abort the current bus cycle. The system processor then begins processing for the bus error. Bus errors are entered in the fault log along with the name of the assembly that failed to send the handshake signal.

Status Decoder

When the system processor is performing an operation, the status decoder lights one of the status LEDs (DS2). The status operations and corresponding LEDs are as follows:

| LED | Label | Description |
|-------|-------|---|
| DS2-5 | UD | User Data, CPU in user state and accessing data |
| DS2-4 | UP | User Program, CPU in user state and accessing program |
| DS2-3 | SD | Supervisor Data, CPU in supervisor state and accessing data |
| DS2-2 | SP | Supervisor Program, CPU in supervisor state and accessing program |

| | | |
|-------|------|--|
| DS2-1 | JACK | Interrupt Acknowledge, CPU is getting interrupt vector numbers |
|-------|------|--|

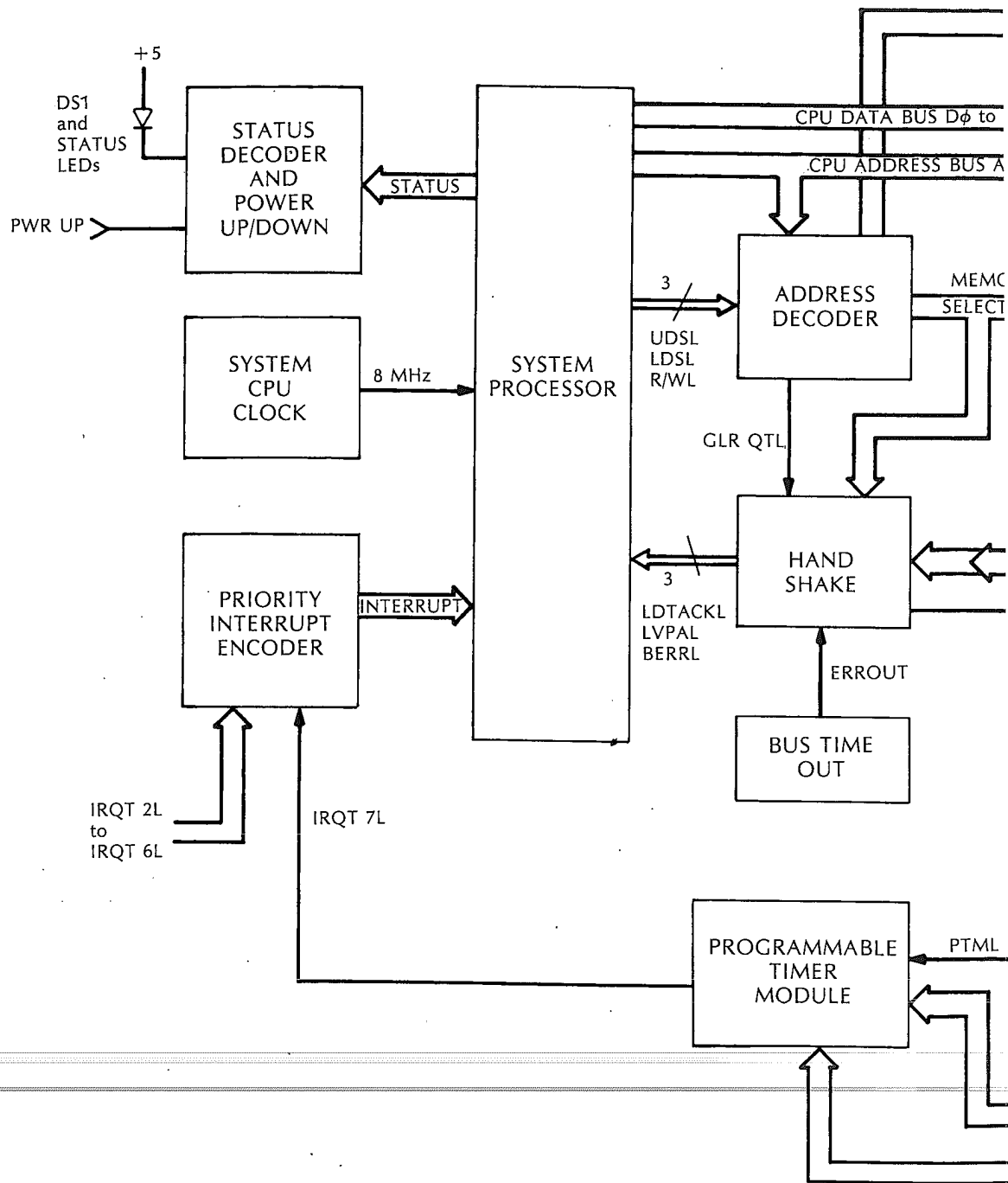
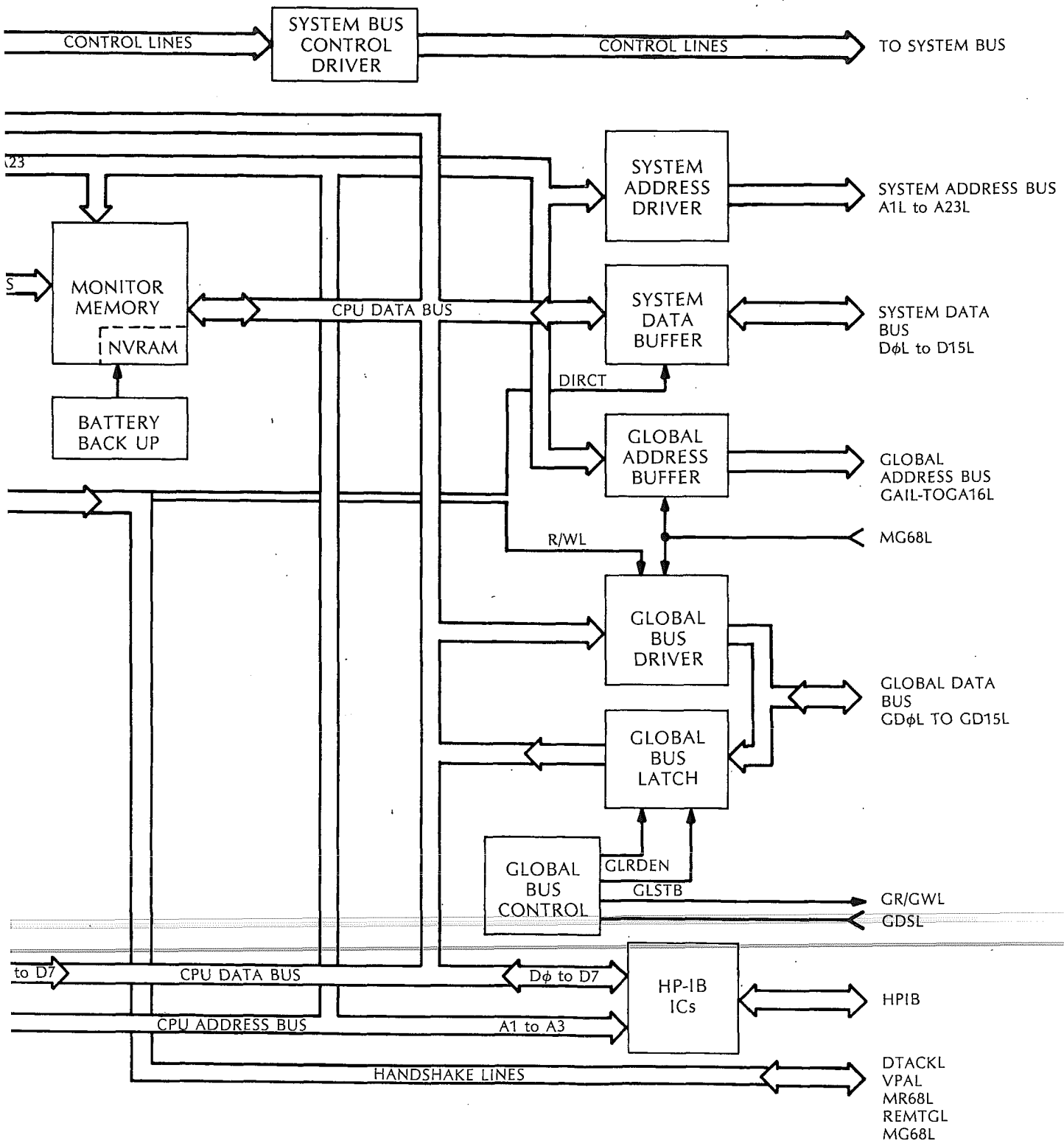


Figure 6-1



System CPU/HPIB Block Diagram

6-5 A3, ROM

The A3 ROM board functions as an extension of read only memory for the system CPU board. The ROM board stores most programs for the HP 3562A except initial start-up routines. All communications between the system CPU board and the ROM board occur over the system bus. Refer to the timing diagram (figure 6-A3a), block diagram (figure 6-A3b), and the schematic (figure 9-A3) as referenced in the following circuit descriptions.

The following descriptions apply to the current ROM board. This board allows flexibility in the number and type of ROM chips used. ROM density (size) is selected by placement of jumpers in the OEL line to the ROM chips, the address comparator section, the delay section, and the ROM decoder section.

Address Comparator

The address comparator verifies that the ROM board is addressed and asserts the ROM select (ROMSELL) line low. The ROMSELL signal does the following:

1. Returns DTACKL to the system CPU to acknowledge that the ROM board was addressed.
2. Enables the ROM Decoder.
3. Enables the Data Bus Driver.

ROM Decoder

The ROM decoders (U21, U22, and U23) are 1-of-8 decoders. They generate the chip enable (CE1L through CE20L) signals by decoding system address lines A16 through A21. The chip enable signal causes the selected ROM pair to put data on the data bus.

Delay

U13 and U14 are used to delay the DTACKL signal based on the speed of the slowest component on the ROM board. The placement of R50 determines the length of the delay (from 0 to 4 clock cycles).

Memory

The memory section of the A3 ROM board consists of 32k by 8 bit read-only-memory chips. The chips are addressed by system address lines A1 through A16 and enabled by CE1L through CE20L. The inverting drivers pass the system address lines from the system bus to all ROMs. The memory is arranged as a lower byte (D0 through D7, stored in U101 through U120) and an upper byte (D8 through D15; stored in U201 through U220). Each CE line enables a lower byte chip and an upper byte chip to put all sixteen data bits on the bus simultaneously.

Data Bus Driver

When enabled by the ROMSELL signal, the data bus drivers transfer data from the ROM data bus to the system data bus.

Theory of Operation

Refer to figure 6-A3a for the following theory of operation. When the system CPU wants to load data from the ROM board, it unasserts the WRITEL line, puts a valid address on system bus lines A1 through A23, then asserts the address strobe (ASL). The address comparator verifies that the ROM board is addressed and asserts the ROM select (ROMSELL) line low. The ROM decoder samples A16 through A21. When gated by the ROMSELL signal, the ROM decoder issues a chip enable (CE) signal to the appropriate ROM pair. The CE signal enables the ROM pair to put data on the ROM data bus. The ROMSELL signal gates the data through the data bus drivers onto the system data bus and returns DTACKL (data acknowledge) to the system CPU.

Internal Signal Descriptions

| | |
|---------------------------|--|
| CE1L through CE20L | Chip enable 1-20, active low. Enable the output from the selected ROM pair. |
| CLK | Inversion of the 8MHz system CPU clock, used in the delay circuit block. |
| ROMSELL | ROM select, active low. Indicates that the ROM board has been addressed, enables the ROM decoder, enables the data bus driver, and returns DTACKL to the system CPU. |

6-5 A3, ROM

The A3 ROM board functions as an extension of read only memory for the system CPU board. The ROM board stores most programs for the HP 3562A except initial start-up routines. All communications between the system CPU board and the ROM board occur over the system bus. Refer to the timing diagram (figure 6-A3a), block diagram (figure 6-A3b), and the schematic (figure 9-A3) as referenced in the following circuit descriptions.

The following descriptions apply to the current ROM board. This board allows flexibility in the number and type of ROM chips used. ROM density (size) is selected by placement of jumpers in the OEL line to the ROM chips, the address comparator section, the delay section, and the ROM decoder section.

Address Comparator

The address comparator verifies that the ROM board is addressed and asserts the ROM select (ROMSELL) line low. The ROMSELL signal does the following:

1. Returns DTACKL to the system CPU to acknowledge that the ROM board was addressed.
2. Enables the ROM Decoder.
3. Enables the Data Bus Driver.

ROM Decoder

The ROM decoders (U21, U22, and U23) are 1-of-8 decoders. They generate the chip enable (CE1L through CE20L) signals by decoding system address lines A16 through A21. The chip enable signal causes the selected ROM pair to put data on the data bus.

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Data Bus Driver

When enabled by the ROMSELL signal, the data bus drivers transfer data from the ROM data bus to the system data bus.

Theory of Operation

Refer to figure 6-A3a for the following theory of operation. When the system CPU wants to load data from the ROM board, it unasserts the WRITEL line, puts a valid address on system bus lines A1 through A23, then asserts the address strobe (ASL). The address comparator verifies that the ROM board is addressed and asserts the ROM select (ROMSELL) line low. The ROM decoder samples A16 through A21. When gated by the ROMSELL signal, the ROM decoder issues a chip enable (CE) signal to the appropriate ROM pair. The CE signal enables the ROM pair to put data on the ROM data bus. The ROMSELL signal gates the data through the data bus drivers onto the system data bus and returns DTACKL (data acknowledge) to the system CPU.

Internal Signal Descriptions

| | |
|---------------------------|--|
| CE1L through CE20L | Chip enable 1-20, active low. Enable the output from the selected ROM pair. |
| CLK | Inversion of the 8MHz system CPU clock, used in the delay circuit block. |
| ROMSELL | ROM select, active low. Indicates that the ROM board has been addressed, enables the ROM decoder, enables the data bus driver, and returns DTACKL to the system CPU. |

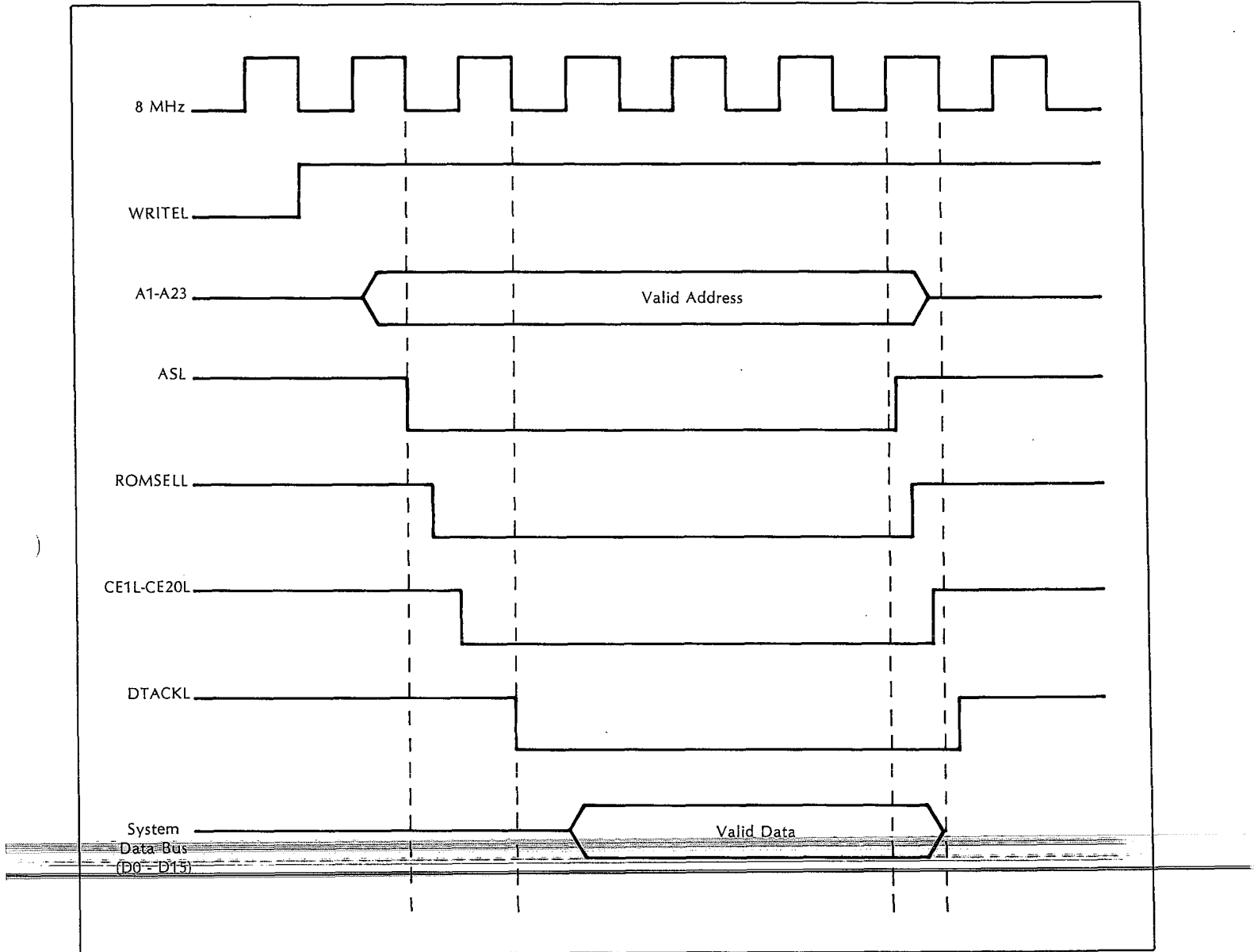
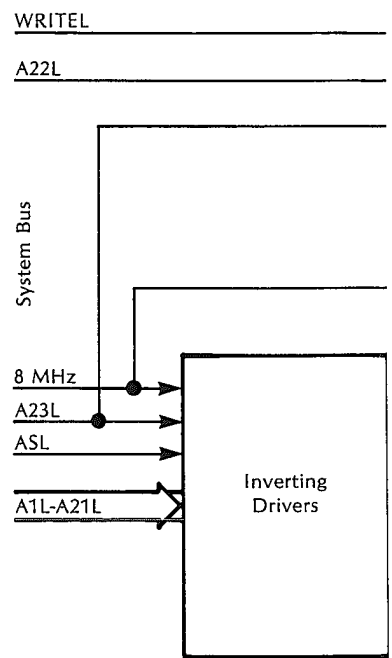


Figure 6-A3a ROM Timing Diagram



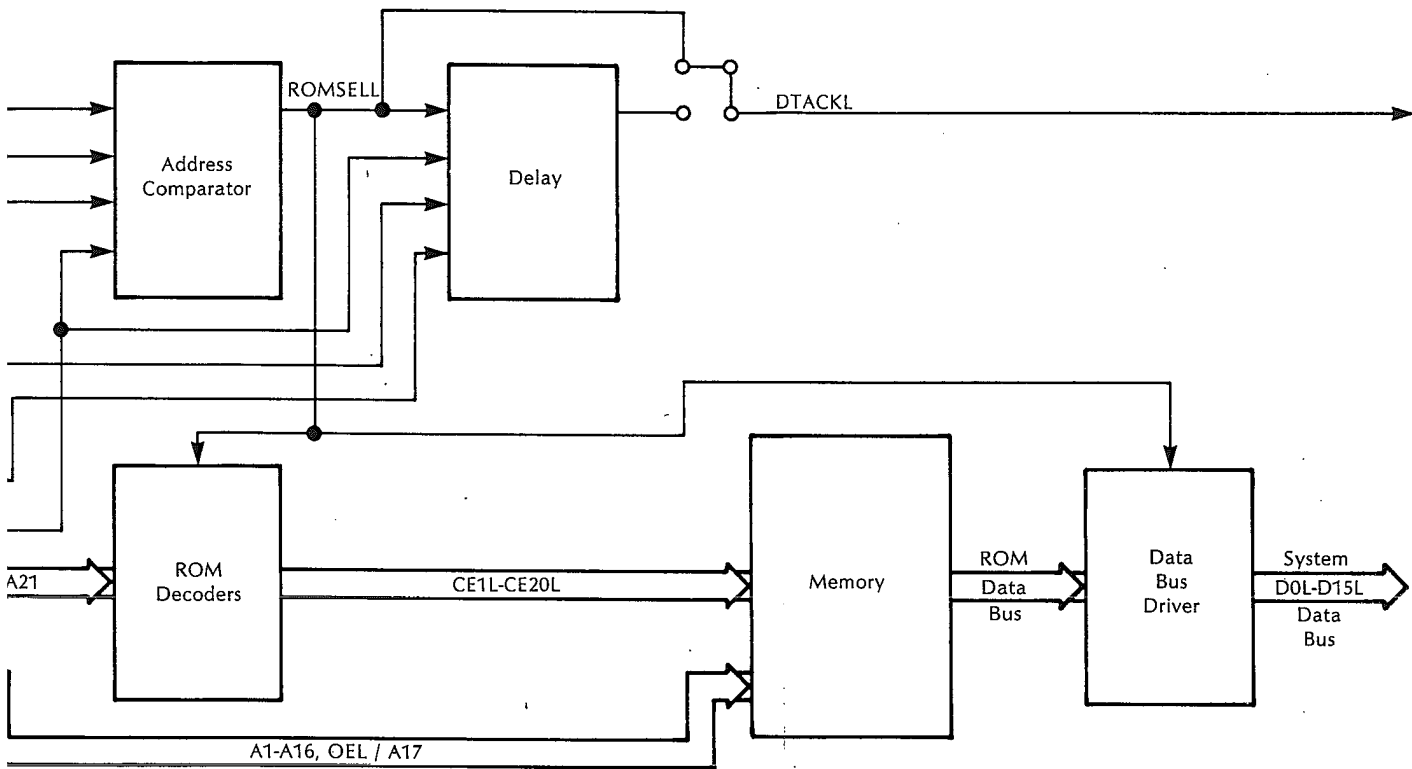


Figure 6-A3b ROM Block Diagram

6-6 A4 LOCAL OSCILLATOR

Introduction

(Refer to figure 6-A4) The A4 Local Oscillator (LO) produces digital sine and cosine signals which are synchronized with the sample rate. The LO outputs digital sine and cosine signals to the A5 Digital Filter. The digital filter uses these signals for the mixing operation when the instrument is in the 'zoom mode' (frequency span <100 kHz). The LO also outputs a cosine signal (NDAT) to the A1 Digital Source. The digital source uses the digital data from the LO to create band-limited noise and interfaces the LO output with the analog source. The analog source is basically a digital-to-analog converter for the LO digital sine wave. The LO output to the digital source is determined by the operation mode of the instrument as follows:

| Mode | LO output to A1 (NDAT) |
|----------------------|--|
| Baseband measurement | Constant output |
| Zoom | Cosine to digital filter |
| Swept sine | Cosine to digital filter |
| Periodic Chirp | Linear swept sine starting at trigger point |
| Burst chirp | Linear swept sine starting at trigger point and ending in accordance with the percent of span setting. |
| Fixed Sine | Sinusoidal wave of specified frequency. |

Theory of Operation

The A2 System CPU starts the sine wave generation process by setting up the LO. When the LO recognizes it has been addressed, data from the system CPU is transferred into the LO's system bus interface. This data contains a command byte to put the LO in the desired mode of operation (the mode is determined by the instrument setup). Once the LO is initialized with the mode of operation and desired frequency values, the system CPU is no longer needed for the sine wave generation process.

After receiving the data from the system CPU, the parallel interface adapter (PIA) sets up the phase accumulator with the frequencies of the sine wave to be generated. The frequency is set by 32 bits of data from the CPU. The address determines which phase accumulator registers are loaded and thus what the frequency represents (source, chirp start, chirp increment, digital filter frequency, etc.) The phase accumulator sends an address that represents the phase value to the sine and interpolator ROMs. For example, an address of 00000000 corresponds to a phase value of 0 degrees, and an address of FFFFFFFF corresponds to a phase value of just under 360 degrees. The sine ROM is a look-up table containing the positive half of a sine wave. The interpolator ROM contains a set of data points used for linear interpolation between the sine ROM data points.

Outputs from the sine (16 bits) and interpolator ROMs (4 bits) are added four bits at a time to determine the sine, cosine, or NDAT data point. The 16-bit sum is sent to the LO output buffers in 4-bit nibbles which are converted to 16 bit words. The word is latched into the proper output buffer to be clocked out in series at the next SYNC2 pulse.

The A5 Digital Filter sends the SYNC2 signal to the LO when it is ready for the next sine and cosine wave data points. The data points are synchronized with SYNC2 and shifted out to the digital filter and digital source. Each serial data stream represents one point (amplitude value) on a sine or cosine wave.

Each sample period corresponds to an LO 'super-cycle'. Each super-cycle is composed of four cycles defined by the state variables S0 and S1. The phase accumulator generates a phase value for sine, cosine, or source during each cycle except for one which is used for general housekeeping. This is shown below:

| S1 (U46-5) | S0 (U46-9) | Output of Phase Accumulator |
|--------------|------------|--|
| 0 | 0 | Cosine data point |
| 0 | 1 | No output, set up for next super-cycle |
| 1 | 1 | Sine data point |
| SYNC2 occurs | | |
| 1 | 0 | NDAT data point |

While the present phase values are being generated in the phase accumulator, the previous set of data points are being processed in the interpolator and adder, and the set of data points before that are being sent to the digital filter and digital source. So, at any given time, there are a couple of sets of data points in process. The process repeats until the LO operation is changed by the system CPU.

When a trigger occurs, the phase value of the cosine is latched into the phase output latches. The system CPU reads this value through the system bus interface and uses this information for an input correction factor. The self-test shift registers are used to test the assembly. During self-test, the system CPU reads and verifies the values from the self-test shift registers and the phase latches.

System Bus Interface

All communications between the A2 System CPU and the LO is through the system bus interface. The main components of the interface are the system bus PAL (U32) and the parallel interface adapter (PIA, U36). The system bus PAL controls all the signals to and from the system CPU. To send a command or data to the LO, the system CPU puts the command or data on the system data bus (D0 to D7) and addresses the LO. A comparator (U37) checks A4L to A8L, LDSL, ASL, and VIOL for a valid address. When the address is valid, the comparator asserts the Valid Address line (VADDR) which enables the system bus PAL. The PAL sets the Valid Peripheral Address line (VPAL) low to enable the system data bus buffers (U24, U28) and to handshake with the system CPU. When the system CPU receives VPAL, it synchronizes the Valid Memory Address line (VMAL) with the Enable Clock (ENBLL). The data is transferred while VMAL is low. System bus lines are only valid as long as VMAL is low.

Phase Accumulator

The phase accumulator uses six internal registers with adders and latches to produce phase values (addresses). One or two registers (depending on mode) contain the phase values which are used to generate the desired sine and cosine values. The other registers contain phase increments, increments of phase increments (chirp mode), or are not being used. These phase increments determine the sine wave frequency (frequency = $\Delta\theta/\Delta T$, where ΔT is the sample period). The only mode in which all registers are used is the chirp mode. The registers are 64 bits, but only the chirp sweep rate uses 64 bits. All other values use the 32 MSB. The data is handled in four, 8-bit chunks each cycle.

Sine ROM (U29, U20)

The sine ROM (U29, U20) takes the phase value from the phase accumulator and uses it to output a digital sinusoidal wave. The sine ROM contains the positive half of a sine wave in a lookup table. The sine ROM takes in 13 phase bits (an address) and outputs 16 amplitude bits (data).

Interpolator and Adder

The interpolator is used to increase the phase resolution of the sine ROM output and produce the data needed for a complete sine wave. The interpolator ROM (U13) uses the output from the phase accumulator to produce an interpolate value. This value is added to or subtracted from the sine ROM output to produce the high resolution output (parallel, 16-bit word) in four, 4-bit chunks.

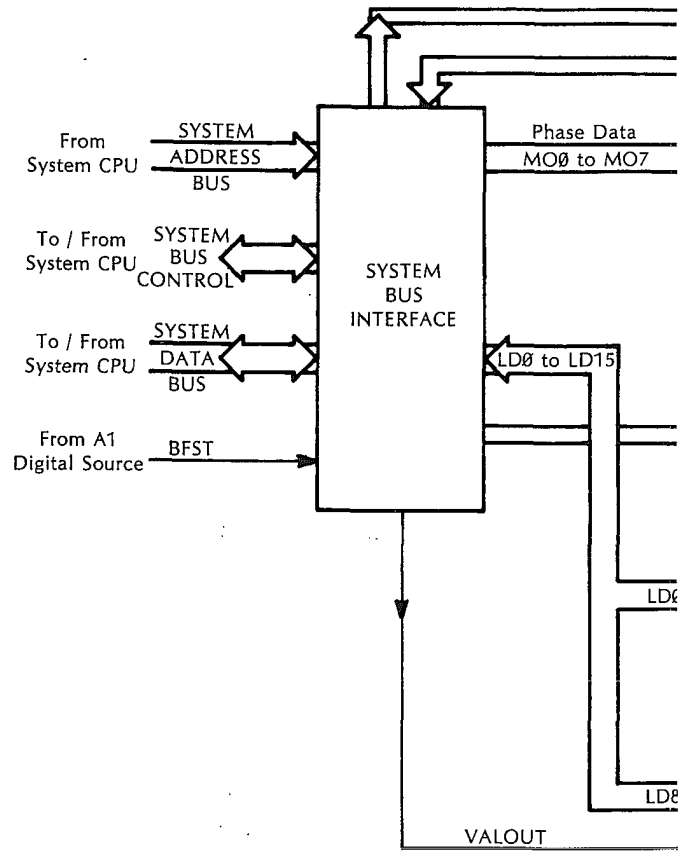
Output Buffers

The output buffers consist primarily of three, 16-bit parallel-in, serial-out shift registers and an output timing PAL (A4 U58). The timing PAL controls the shift registers and the self-test shift registers.

Control Circuits

The control circuits consist of two PALs, one PLA, and some related circuitry. The function of these circuits are as follows:

| | |
|-----------------------------|--|
| Phase Accumulator PAL (U56) | This PAL controls the input, output, and shifting of the data in the phase accumulator. |
| Interpolator PAL (U55) | This PLA controls the addition, subtraction, and slope functions for the interpolator output and other random logic functions. |
| Timing PAL (U68) | This PAL produces the basic timing signals of the LO. |



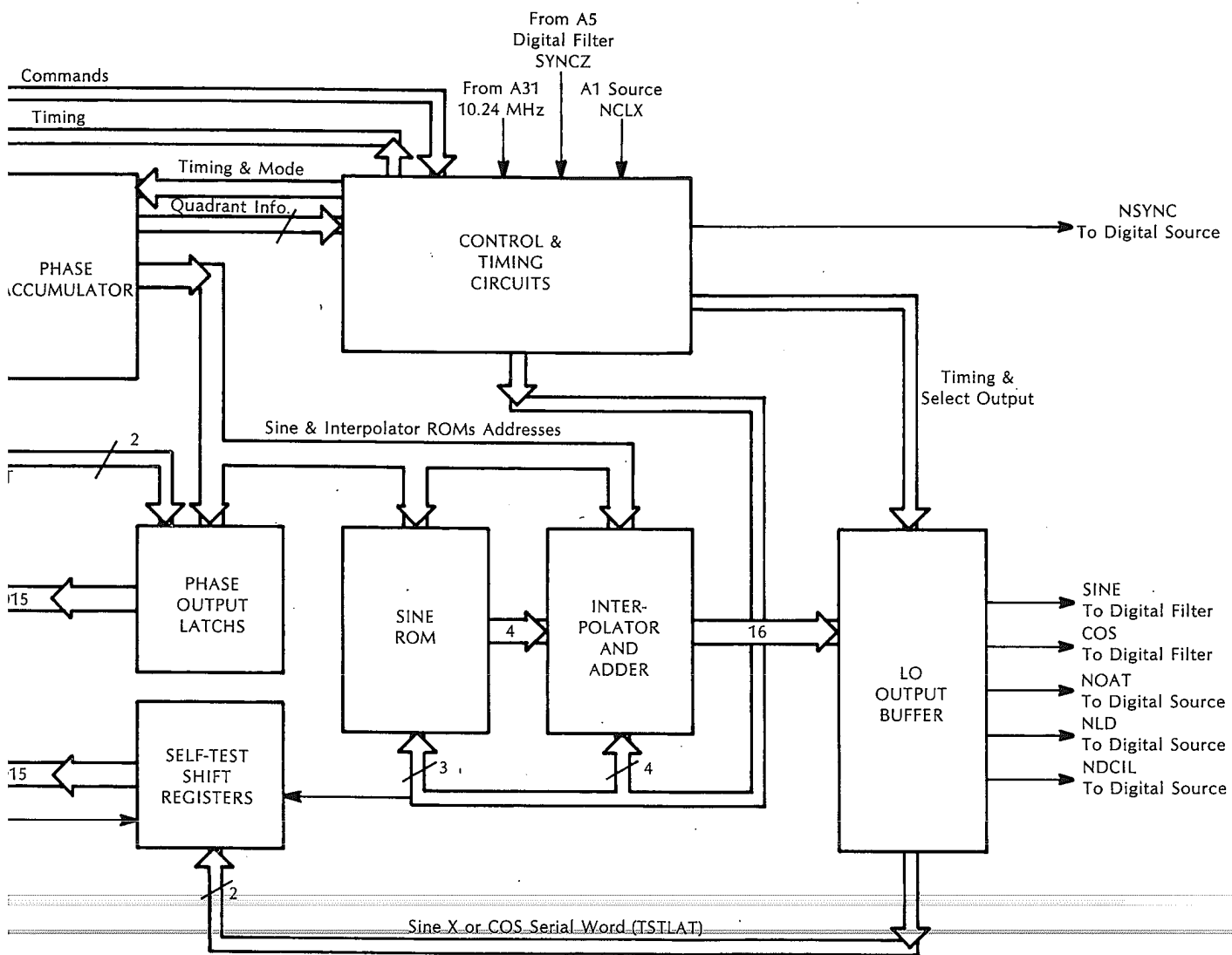


Figure 6-A4 Local Oscillator Block Diagram

6-7 A5, DIGITAL FILTER A6, DIGITAL FILTER CONTROLLER

The digital filter assembly (DFA) consists of the digital filter board (A5) and the digital filter controller board (A6). The digital filter processes two channels of serial data from the instrument front end (ADC boards) and stores the results in global RAM. Processing consists of conversion from a serial format to a parallel format and, if required, digital filtering or zoom (a combination of frequency shifting and filtering). The processed data is transferred on the global data bus to Global RAM (A8).

Data Flow

Refer to the block diagram in figure 6-A5a. Two data signals, one from each input, come onto the A5 board in a serial format from the A32 and A34 ADC boards. These signals enter the digital filter blocks where they are processed.

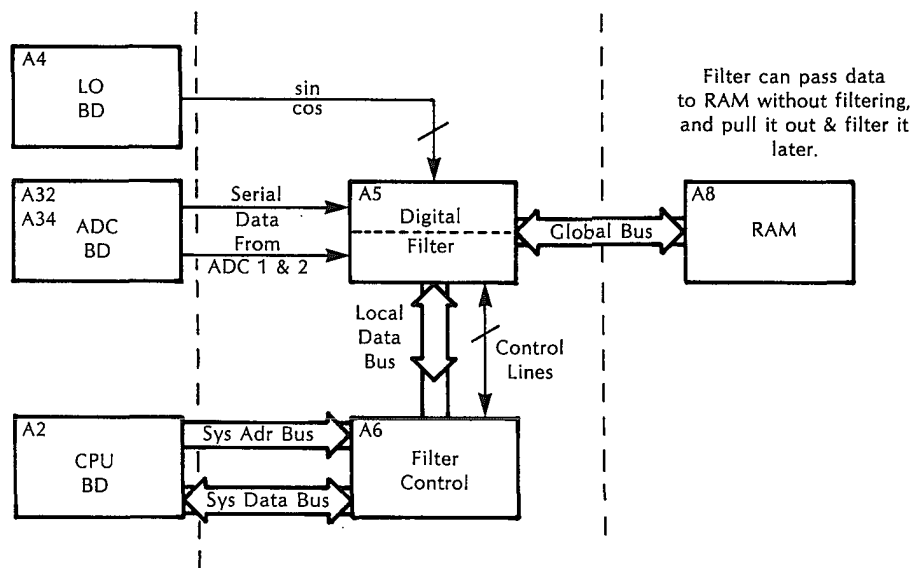


Figure 6-A5a System Block Diagram Referenced to the Digital Filter Boards

When the digital filter is ready for data, it sends DREQ (data request) to the ADC boards.

In response, the ADC boards send data to the digital filter at a 10.24 MHz rate. The data is reclocked by A5 U512. The filter accepts one input data word and sends the SYNC2 pulse to the A4 Local Oscillator and A6 Digital Filter Control boards.

Measurement data is input serially to a filter controller. Incoming data is processed in one of three ways:

Streaming

If VIEW TIME is selected with a span of 100 kHz or VIEW INPUT is active, processing consists only of conversion to a parallel format for storage in Global RAM.

Baseband

If filtering is required and the frequency span is 100 kHz, the filter controller passes the incoming data to the filter ICs in serial format. The filter ICs multiply the incoming data by the LO data signal. This signal is a constant when not in zoom. The filter ICs filter the data and return it to the controller IC. Depending on the processing required, this may be a multipass operation. The controller IC converts the filtered data to a parallel format.

Zoom

Zoom is used when the selected span is less than 100 kHz. The filter controller passes the data to the filter ICs in a serial format. The filters down-convert the input data by mixing it with a digital representation of the span center frequency from the LO board. The resultant sum and difference are filtered to remove the sum component and yield a reduced frequency span. See figure 6-A5b. The filters return the processed data to the controller IC, which converts the data to a parallel format.

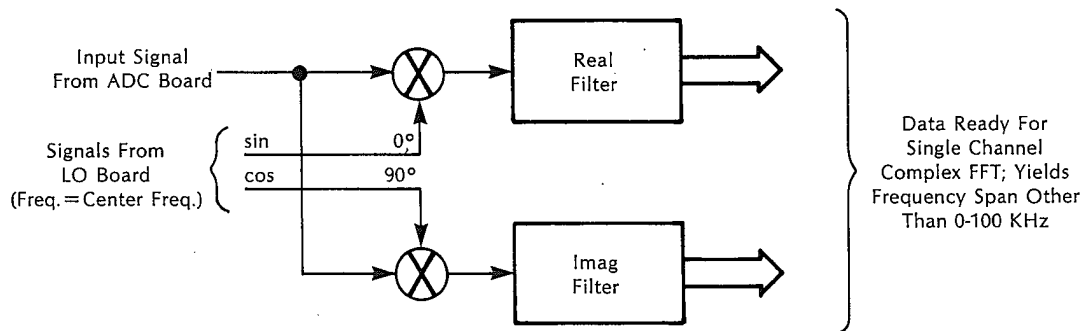


Figure 6-A5b Zoom Implementation

When the processed data is ready for storage, the controller ICs request the digital filter local data bus. When granted use of the bus, the controller ICs transfer the data to the global data bus interface. The global bus DMA controller sends a memory request to Global RAM. When Global RAM returns a memory grant, the data flows on the global data bus to Global RAM.

~~When data in global RAM requires filtering (as if the data were stored without filtering) the data comes into the filter controllers via the global data bus interface and the digital filter data busses. The remainder of the process is the same as described previously.~~

A5, Digital Filter Block Descriptions

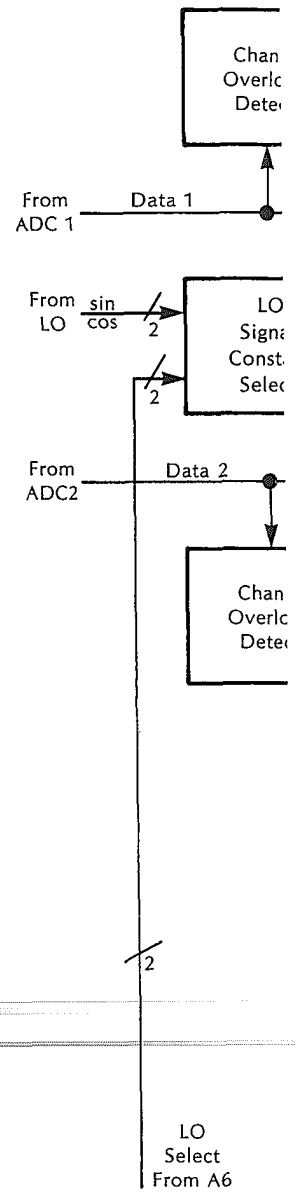
Refer to figure 6-A5c, A5 Block Diagram, for the following circuit block descriptions.

DIGITAL FILTER

Each digital filter consists of a control IC and two filter ICs, one for real data and one for imaginary data. When in the zoom mode, the filters multiply the input data by a digital sine (real) and cosine (imaginary) function from the LO assembly.

The digital filters have three modes of operation, controlled by three DIS lines from the filter control block. The measurement data out of the filters corresponds to these lines as follows:

- DIS1 In baseband (non-zoom) mode, the control IC outputs filtered data from the real filter. In zoom mode the control IC outputs the real data first, followed by the imaginary data.
- DIS2 The control IC outputs the data from the imaginary filter (third octave).
- DIS3 The control IC outputs unfiltered data.



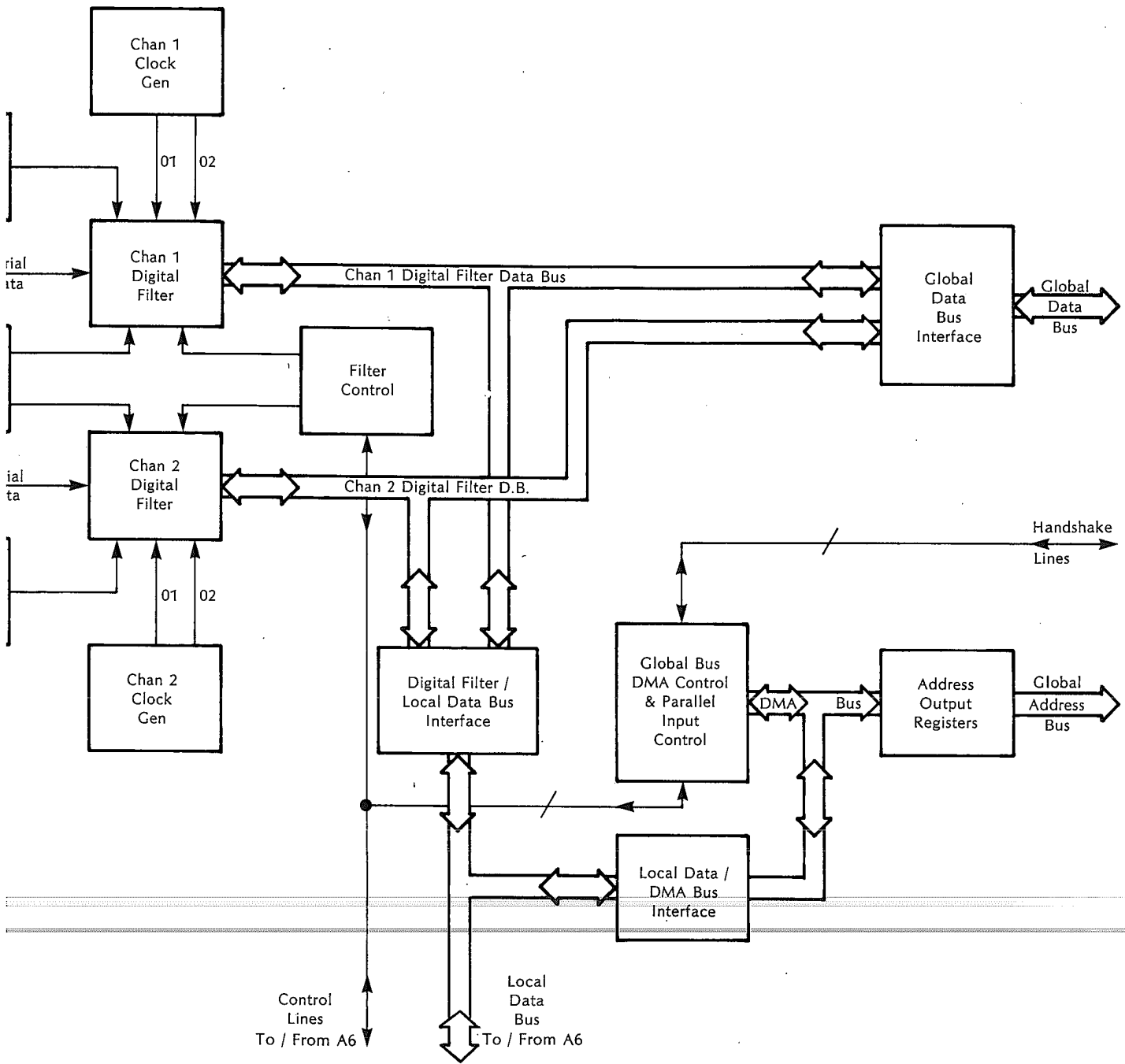


Figure 6-A5c A5 Block Diagram

CLOCK GENERATOR

The clock generator creates two complementary clock pulses from the 10.24 MHz system clock. This circuit produces an eight volt peak pulse signal for use in the digital filter ICs. This pulse must drive a high capacitance and still reach approximately eight volts.

OVERLOAD DETECT

The first three bits in the ADC serial data stream contain overrange information from the ADC converters. This information is stripped off the serial data stream by the digital filter control IC and processed by the ADC overload detect IC. The overload information is then sent to the digital filter control IC and included in the status information given to the system CPU.

LO SIGNAL/CONSTANT SELECT

The local oscillator/constant select circuit multiplexes the SINE and COSINE signals from the LO board to the CH1 and CH2 digital filter functional blocks. In baseband operation, a constant is output by activating CH1LOSEL and CH2LOSEL signals.

DIGITAL FILTER/LOCAL DATA BUS INTERFACE

The digital filter/local data bus interface isolates the digital filter bus from the local data bus. The information passing through these ICs consists of configuration commands from the system data bus to the digital filters and status information from the digital filters to the system data bus.

FILTER CONTROL

The filter control block controls data flow for the three digital filter modes. When a filter controller IC has data ready to store in global RAM, it requests the global bus by activating the CHxBRy signal, where x corresponds to input channel number (1 or 2) and y corresponds to the channel mode number (1, 2, or 3; see DIGITAL FILTER description). A5U205 and A6U206 enable only the channel and mode for which access to the global bus has been requested and granted.

GLOBAL BUS DMA CONTROL

The global bus DMA control and parallel input control block is composed of several smaller blocks. The function of these blocks is explained in the following discussion.

The **DMA address decoder** (A5U505) receives addresses from the system address decoder on the A6 Digital Filter Controller board. These addresses and the MYADDR control line are decoded to generate filter channel write control, channel output strobe, and read status signals.

The **DMA pointer register** (A5U311) latches into the DMA controller ICs (A5U307, A5U309) the address of an internal DMA Controller register that is to be loaded with information.

The **local data/DMA bus interface** (A5U406 and A5U411) latches start and stop addresses onto the DMA bus. This information is used by the DMA controller(s) to partition the global RAM on A8 for the different output modes of the DMA controller.

The **global data bus interface** (A5U304 and A5U404 for the channel one digital filter and A5U313, A5U413 for the channel two digital filter) latches data from the digital filter data busses to the global data bus.

The **global bus DMA control** circuit takes the decoded address information from the DMA address decoding functional block. The decoded information programs this block into the correct state machine mode for the output from the digital filters. The control line outputs from this functional block control the timing and synchronization of the output buffers and A8 global RAM addressing.

The **parallel input control** circuit controls the transfer of parallel data from the global RAM into the digital filters through the global data bus interface.

A6, Digital Filter Controller Block Descriptions

Refer to figure 6-A5d, A6 Block Diagram, for the following circuit block descriptions.

SYSTEM DATA BUS INTERFACE

The system data bus interface consists of tristate transceivers connecting the system data bus and the local data bus. The system CPU configures and reads status from various registers in the digital filter assembly through this interface and the local data bus.

SYSTEM ADDRESS DECODER

The system address decoder is divided between the A5 and A6 boards with some of the circuitry appearing on each. The system address bus is connected to the A6 control board. Part of the address (A5L-A8L and VIOL) is decoded by the system address decoder (A6U404). This IC is an eight-bit identity comparator configured to activate the signal MYADDRSL when the filter assembly is addressed by the system CPU.

~~The lower four bits of the system address and the signals UDSL, LDSL, WRITEL, and RESETL are buffered into the digital filter assembly by A6U403. These buffered signals go to address decoders on the control (A6) and filter boards A(5).~~

The address decoder on the control board (A6U304) decodes address information into measurement commands, counting instructions, and interrupt masks.

DATA POINT COUNTER

The data point counter monitors the information required to synchronize the actions of the various components of the filter assembly. A6U109 contains five 16-bit counters used to count the number of data points (samples) stored in Global RAM. Configuration information from the system CPU is written into this counter and status information read from it via the local data bus. Each of the five counters has an output (OUT1 through OUT5) to signal when the counter has reached its terminal count.

The **counter read/write control** (A6U107) controls timing for data transfer between the U109 counter and the local data bus. U107 is held in a clear state until the system CPU activates the counter select signal (COUNTERSELH). Operating as a shift register, U107 drives the chip select (CS) counter input and the NAND gates driving the read and write inputs to the counter. After four clock cycles of delay, the proper configuration signals cause the counter to write to or read from the local data bus.

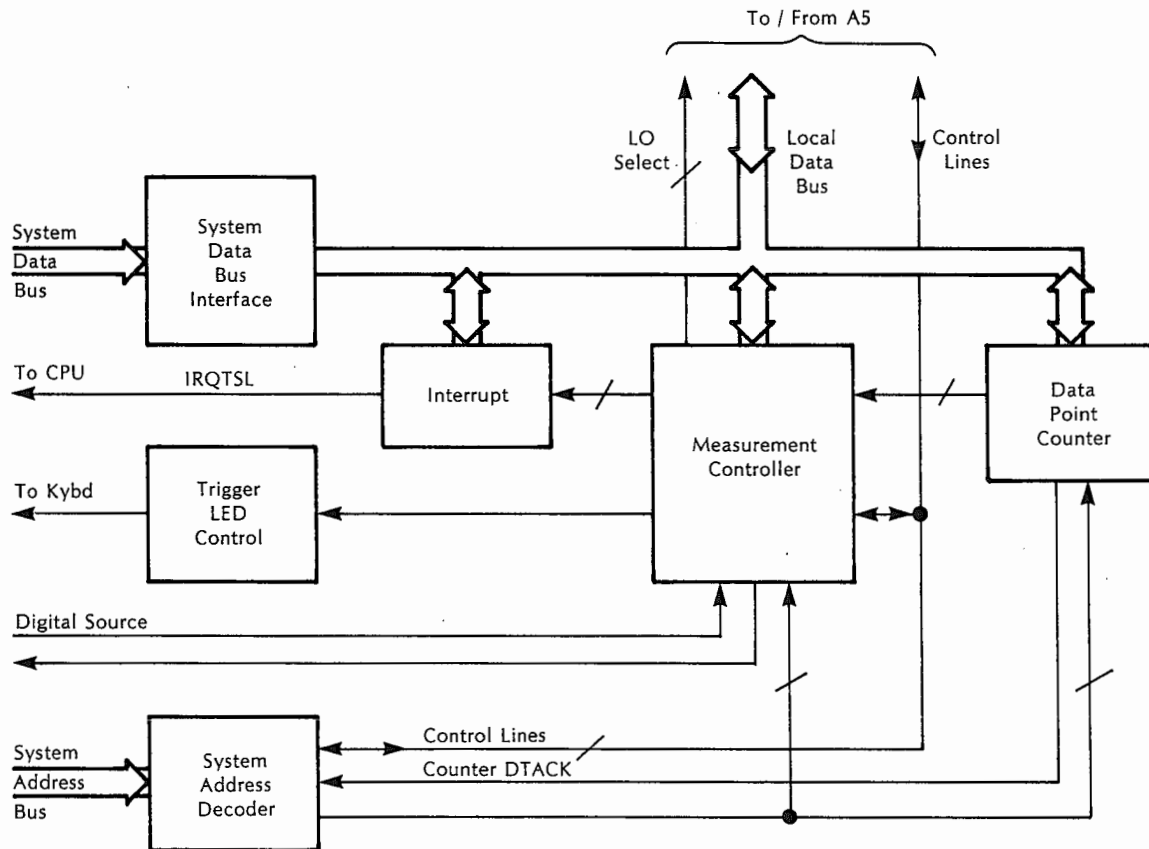


Figure 6-A5d A6 Block Diagram

MEASUREMENT STATE MACHINE

This block consists of five parts:

- Command Register
- Measurement Control Machine
- Status Register
- Start/Stop Control
- Trigger Control

This block, configured by the system CPU, controls how the digital filter assembly works in the various modes.

The **command register** (flip-flops A6U307 and A6U109) is used to read data lines from the local data bus into the measurement state machine. The command is clocked into the register by the signal WRIBCCMDL (write IBC command) from the address decoder. (The digital filter assembly is sometimes called the input buffer control.) The commands configure the measurement state machine, control the LO selection on the digital filter board, and provide information to the trigger LED control block.

The **measurement control machine** senses configuration and status signals and controls the measurement. When it is configured for the type of measurement and receives a start signal, the measurement control machine enables the measurement to start. A measurement is complete when OUT4 is activated. OUT4 is reclocked, called BLKFULLH, and connected to an input of the measurement control machine. The measurement is terminated by activating the SETBLKREADYL signal, causing a CPU interrupt. The CPU decides when the transfer to RAM may be executed and grants the global bus appropriately.

The **status register** is an eight-line latch which allows the A1CPU to read the status of the digital filter assembly. The status word is latched onto the local data bus when the RDIBCSTATL signal is activated. Bit 0 is a signal called NOTREALTIMEFLG. This signal activates when data can not be moved through the DFA fast enough to prevent delay of further measurements. In this case, the data in global RAM is not updated fast enough to be real time. This flag is reset every time the status word is read. If the condition is still not real time, the reset does not change the status of the NOTREALTIMEFLG signal (CLR overrides a SET command).

The **start/stop control** (A6U309) and the **trigger control** (A6U409) are used to control triggered measurements. In a triggered measurement the digital filter begins processing data and storing it in RAM when the trigger board senses the trigger signal. There is also some interaction with the source. Here is an example sequence of events for a triggered measurement:

- If pretrigger delay is active, data is taken before a trigger signal is received. If pretrigger delay is 100 samples, the counter keeps track of the number of samples and the trigger signal is ignored until at least this many samples are taken. OUT1 is active when pretrigger delay is complete. The trigger control IC recognizes this and arms the trigger by activating the ARML signal. This signal goes to the digital source which is waiting for a trigger.
- When the digital source receives the trigger it activates the signal BFST (buffer start) going back to the trigger controller on A6.

- The trigger controller activates TRIGATEL, signaling the counters to continue counting input samples, and the measurement runs to completion.
- The start/stop controller controls the A5 Digital Filter outputs. CH1STOP1 controls DF1 main output and CH2STOP1 controls DF2 main output.
- When a triggered measurement is complete the output of the start/stop controller (BLKDONE) is sent to the measurement control state machine.

INTERRUPTS

There are six interrupt flags:

| | |
|--------------|--|
| TRIGGERED | Set if a valid trigger event has occurred after ARML is activated |
| MARKER | Set if a marker count has finished during a freerun measurement |
| BLOCK3FULL | Set when the measurement mode data blocks are complete for both channels |
| BLOCK2FULL | Set when auxiliary data block 2 is filled |
| BLOCK1FULL | Set when the filtered auxiliary data block is filled |
| INBLOCKEMPTY | Set when the parallel input data blocks have been emptied |

When one of these interrupt flags is set, the digital filter controller sends an interrupt (IRQ5L) to the A2 System CPU. After receiving the interrupt, the system CPU reads the Interrupt Register Latch (U302) to determine which signal caused the interrupt.

Any combination of flags may be cleared through the CLRINTL signal and the local data bus. These two signals are ANDed together into the CLR inputs of each of the interrupt flag flip-flop registers. Typically, the interrupt routine clears only the flag it deals with. The CPU uses addressing to activate CLRINTL.

The interrupt mask register (A6 U301) is a write only register that allows selective enabling of the interrupting events. The corresponding bit in the mask register must be set to enable an interrupting event to cause a system interrupt.

TRIGGER LED CONTROL

This circuit is composed of a dual monostable multivibrator (A6U310) and a one-of-eight multiplexer (A6U410). This circuitry causes the front panel TRIGGERING LED to flash once each time a trigger is received.

Internal Signal Descriptions, A6

| | |
|--------------------------|--|
| ABORT | Used to stop Digital Filter Assembly activity |
| BLKDONE | Signal from start/stop controller to measurement control state machine to indicate that a triggered measurement is complete |
| BLKFULL | Block full. Input to measurement control machine which indicates that a measurement is complete |
| BLKREADYFLG | Set when the measurement mode data blocks are complete for both channels |
| BLK2FULLFLG | Set when the auxiliary data block 2 is filled |
| BLK3FULLFLG | Set when the unfiltered auxiliary data block is filled |
| CLRINTL | Clear interrupt. Clears the addressed interrupt flag flip-flop |
| COUNTERSEL | Counter select, enables U107 |
| COUNTERDTACKL | Data point counter data transmit acknowledge |
| DMEANABLEL | Timing signal from measurement control machine to start/stop control and trigger control |
| FLASH | Signal activated in the trigger LED control block each time a trigger occurs |
| FREERUN | Used with TRIGGERED to select the measurement mode. If TRIGGERED is set and FREERUN is clear, triggered mode is selected. If FREERUN is set and TRIGGERED is clear, freerun mode is selected. If both bits are clear, stream mode is selected. |
| GATE2L | Signal to data point counter indicating that a trigger has occurred |
| INBLKEMPTYFLG | Set when the parallel input data blocks have been emptied |
| MARKER, MARKERFLG | Set if a marker count has finished |
| MASK0-2, 13-15 | Outputs from the interrupt mask register |
| MEASURING | Set when the measurement is active. Used for control of the front panel TRIGGERING LED |
| NOTREALTIMEL | Signal to trigger LED control indicating that measurement is not real time |
| NOTREALTIMEFLG | Indicates that data cannot be moved through the DFA fast enough to prevent delaying further measurements. |

| | |
|---------------------|---|
| RDIBCINTL | Read input buffer control interrupts |
| RDIBCSTATL | Read input buffer control status. Latches status word from status register onto the local data bus |
| SETBLKREADYL | Terminates a measurement by generating a CPU interrupt |
| SFLTRST | Set filter reset |
| STOPENL | Stop enable |
| TPULSE | Test pulse, replaces system clock signal when A6J2 is in test position |
| TRIGATEL | Signal from trigger controller to counters to continue counting input samples |
| TRIGGERED | See FREERUN |
| TRIGGERFLG | Set if a valid trigger event has occurred after being armed |
| WRIBCCMDL | Write input buffer control command. Clocks commands from the local data bus into the command register |
| WRINTMSKL | Write interrupt mask. Used to mask interrupt flags |

Internal Signal Descriptions, A5

| | |
|---|---|
| 2XCLKL | The buffered on-board 10.24 MHz clock |
| CH1A/DDATA | Serial data inputs from the ADC assembly which have CH2A/DDATA been reclocked by U512 |
| CH1AEN, CH2AEN | Channel 1 and channel 2 address enable |
| CH1BG1, CH2BG1 | Bus grants for DMA channels 1, 2, and 3 |
| CH1BG2, CH2BG2 | |
| CH1BG3, CH2BG3 | |
| CH1BR1, CH2BR1 CH1BR2, CH2BR2 CH1BR3, CH2BR3 | Bus requests for DMA channels 1, 2, and 3 |
| CH1DACK3L, CH2DACK3L | Data acknowledge, channel 1 and channel 2 |
| CH1DIS1, CH2DIS1 CH1DIS2, CH2DIS2 CH1DIS3, CH2DIS2 | Disable DMA modes 1, 2, and 3 |
| CH1DMACS, CH2DMACS | Enable channel 1 or channel 2 of the DMA Pointer Register and DMA Controller |

| | |
|---|---|
| CH1DMAL, CH2DMAL | Channel 1 and Channel 2 direct memory access |
| CH1DREQ3, CH2DREQ3 | Data request, channel 1 and channel 2 |
| CH1EOPL, CH2EOPL | Timing signal from DMA controller to filter control block |
| CH1HACK, CH2HACK CH1HREQ, CH2HREQ | Timing signals between DMA controllers and global bus DMA controller |
| CH1HLFSCALE, CH2HLFSCALE | Status signal from the ADC assembly asserted whenever the analog input exceeds half-range in amplitude |
| CH1IORL, CH2IORL CH1IOWL, CH2IOWL | Read/write signals in global bus DMA control block |
| CH1IS1L, CH2IS1L | Strobe from Global Bus DMA Control to Filter Controller for polling status word |
| CH1LO1 CH1LO2 | Signals from the Digital Filter Controller assembly used to select the input to the digital filters. The input can be either the sine/cosine data from the local oscillator or a locally generated constant |
| CH1MEMRL, CH2MEMRL CH1MEMWL, CH2MEMWL | Clock data through global data bus interface |
| CH1OVLD, CH2OVLD CH1 + OVLDL, CH2 + OVLDL CH1 - OVLD, CH2 - OVLD | Status lines to Filter Controller to indicate overload condition on ADC assembly |
| CH1RDFLTSTATL, CH2RDFLTSTATL | Read filter status channel 1 and channel 2 |
| CH1SHIFT1 | Signal from the channel 1 filter control to request data from the ADC assemblies |
| CH1SYNC2 | Serial data accepted. Signal to A6 board that the digital filter accepts an input data word |
| CH1XCVREN, CH2XCVREN | Channel 1 and Channel 2 transceiver enable |
| CH1*PHI*1 CH1*PHI*2 | 5.12 MHz non-overlapping clocks |
| CH1ϕ1FBL CH1ϕ2FBL | 5.12 MHz clock signals |
| DIR1, DIR2 | Control direction of data flow through global data bus interface |
| DMADTACKL | DMA data acknowledge |

| | |
|--|---|
| DMAPOINTER | Clock for DMA Pointer Register |
| DMARST | DMA reset |
| FCLK, FCLKL | 5.12 MHz clock signals |
| MRST | Master reset signal |
| OS1L, OS2L, OS3L | Data valid strobes for mode words 1 and 2 and external parallel A/D data on the data bus |
| OS3ENL | Data valid strobe for external parallel A/D data on the data bus |
| PLGR1L, PLGR2L PLGRANT PLRQL PXGO | Signals from the parallel input control block which control the input of data from Global RAM to the digital filters. |
| TEST1L | A/D self test input to filter ICs |
| TEST2L | LO self test input to filter ICs |
| WRIBCCMDL | Write input buffer control command. Clocks data into the command register |

6-8 A7 FLOATING POINT PROCESSOR

(Refer to figure 6-A7) The Floating Point Processor (FPP) is a fast arithmetic unit which carries out real and complex arithmetic operations on blocks of data stored in the A8 Global RAM. The processing units (ALUs) of the FPP are six AM2903 bit-slice microprocessor ICs. Instructions are provided to the ALUs by an address sequencer and seven microcode PROMs.

The FPP can perform 85 unique operations including addition, subtraction, multiplication, and division. Operations are performed on data blocks which have been normalized and stored in the A8 Global RAM. The data can have one of three formats:

- 2's complement integer (16 bit)
- Single precision floating point (32 bit)
- Double precision floating point (64 bit)

The operation the FPP performs on a data block is dictated by the A2 System CPU. The system CPU sets up a command stack in the global RAM to tell the FPP which operation to perform. A command stack consists of the following:

- 32 bit command word (add, sub, etc.)
- Number of entries in the data block which are to be operated on.
- Constants to indicate if the data block is real or complex.
- The beginning address of the data block in global RAM.
- The destination address of the results.

Commands may be executed individually or in groups. Commands in groups are executed in series and can include multiple looping.

To perform an operation, the FPP interfaces with the A2 System CPU and the A8 Global RAM. ~~The programs stored in the microcode memory control the timing and interactions between the three assemblies.~~ The following is an overview of an FPP operation:

1. The system CPU puts a command stack or series of command stacks in the global RAM.
2. The system CPU addresses the FPP using the system address bus and puts the starting address of the command stack on the system data bus.
3. The FPP recognizes that it has been addressed (ADDFLG) by the CPU.
4. The ALUs read the command stack's address that is now in the command pointer registers and on the B bus. The address of the command stack is stored in the internal registers of the ALUs.

5. The FPP fetches a 32 bit command using the Y bus and corresponding global bus registers.
6. The ALUs read and store the address of the data block to be operated on.
7. The instruction mapping PROM interprets the command data on the Y bus and tells the sequencer where to start its address sequence.
8. The sequencer addresses the microcode memory using the pipeline address bus.
9. The microcode memory sends the appropriate instruction to the ALUs using the A and B port address and ALUs instruction bus.
10. The designated instruction is performed.
11. When finished with a command (or an error is detected), the FPP sends an interrupt (IRQT3L) to the system CPU.
12. Steps 8 through 11 are repeated until the computation is completed. This process includes instructions for fetching data blocks from global RAM.
13. The result of the computation is stored in global RAM at an address previously specified in the command stack.
14. The FPP fetches the next command stack.
15. Steps 5 through 13 are repeated until all the command stacks are done (unless the FPP is reset or an error is detected by the condition code multiplexor).
16. The sequencer addresses the microcode memory for the 'wait' command.
17. The wait command is executed using the constant pipeline interface. The FPP remains in a wait loop until the next command address flag (ADDFLG) is sensed.

System Address Decoder and Handshake

~~After the command stacks have been set up in global RAM, the system CPU asserts the system address and control lines to start FPP operations. The address comparator asserts the My Address signal (MYADDRSL) to activate the address PAL. The address PAL activates the following signals:~~

1. Address Flag (ADDFLG)
This signal latches the system data bus into the command pointer registers. (This data is the starting address of the command stack in global RAM.)
2. Data Acknowledge (DTACK)
DTACK is returned to the system CPU to indicate the completion of the FPP handshake.
3. Condition Code (CCODE)
CCODE is sent to the sequencer. When the sequencer receives CCODE, it branches out of wait loop and starts the FPP process.

Sequencer (U103)

The sequencer is an 'address sequencer' used to control the execution of microinstructions stored in the microcode memory. The sequencer has the capability of sequential access and conditional branching to any microinstruction in the microcode memory. During each microinstruction, the sequencer provides a 12-bit address to the microcode memory from one of four sources:

1. The incremented present address.
2. A jump address from the microcode memory or instruction mapping PROM.
3. A jump address from a previous microinstruction that stored an address in an internal register of the ALUs.
4. A subroutine return address from the sequencer's internal stack register.

The sequencer's next address is determined by the test and jump PROM, the conditional code multiplexor, and the instruction mapping PROM.

Global Bus Interface

The FPP has the ability to read and write 16 and 32 bit words to and from the global RAM. When doing a 32 bit operation, the FPP uses two consecutive 16 bit word operations. This is accomplished by addressing the first 16 bit word followed by inverting GA1L for the address of the second 16 bit word. For 32 bit floating point data, the first data word contains the most significant bits of a mantissa and the second data word contains the least significant bits of the mantissa and the exponent. This results in a 24 bit mantissa, 8 bit exponent, floating point data word.

To start the global bus transfer, the ALUs write the global RAM address for the data word on the B bus. The bus control PROM uses control lines PLSA, PLSB, and PLSC to command control PAL 1 and control PAL 2 to set up the FPP assembly for a data transfer. If the FPP is to read a 32 bit data word from global RAM, the following operations occur:

1. Control PAL 1 asserts the Memory Request Flag (MRFLG) signal which causes the following:
 - a. The address on the B bus is latched into the global address registers.
 - b. Bit 0 of the B bus is clocked through the test even flip-flop (U215) to determine if the address is an even or odd number.
 - c. Control line PLSA is clocked through the read/write flip-flop (U215) to control PAL 2 to set up for a data read operation.
2. Control PAL 1 asserts the Memory Request FPP signal (MRFPP) to the global RAM.
3. The global RAM responds by sending the Memory Grant FPP signal (MGFP) to the FPP. This causes the following to occur:
 - a. The global address registers are enabled.
 - b. Control PAL 2 asserts the Global Read/Write signal (GR/GWL) for a read operation.
 - c. Control PAL 2 tests its Q1 input to determine if this is the first half or second half of the 32 bit word.

4. The global RAM assembly places the data on the global data bus and activates the Global Data Strobe signal (GDSL) which latches the data into the global bus registers.
5. The global RAM assembly sets the MGFPPPL line low to inform control PAL 1 that the first half of the 32 bit data word has been loaded into the FPP assembly.
6. Control PAL 1 sets global address line 1 (GA1L) high which increments the address to global RAM by one for the second half of the data word.
7. The second half of the data word is now loaded into the global bus registers.

Arithmetic Logic Units (ALUs)

The Arithmetic Logic Units (ALUs) subblock consists of six 4-bit sliced arithmetic-oriented microprocessors (AM2903) cascaded for up to 24-bit mathematic operations. The ALUs can do complete arithmetic and logic instructions including multiplication, division, and normalization. Arithmetic and logic instructions are read from the ALUs instruction bus by the ALUs internal instruction decoder.

The ALUs have a 16 x 24 bit RAM for storing data. To load the ALUs RAM, the data in the global bus registers is placed on the Y bus when MANL is active and on the B bus when EXPL is active. The A Port Address from the microcode memory determines the storage location of the data block address (upper Y bus) and the B Port Address determines the location of the B bus data and the location of the data coming in and going out on the Y bus.

The ALUs perform operations using two operands. Multiplexors in the ALUs provide selection of various pairs for the operands which can be data from the ALUs RAM or data from the external buses.

After the ALUs have completed an operation, several status bits are sent to the condition code multiplexor for testing. The status bits are as follows:

ZERO

Indicates the ALUs Y bus output is zero (all 24 bits)

NEG

From the most significant ALU (U310) indicating a negative result.

OVR

From the most significant ALU (U310) indicating an operation has resulted in an overflow.

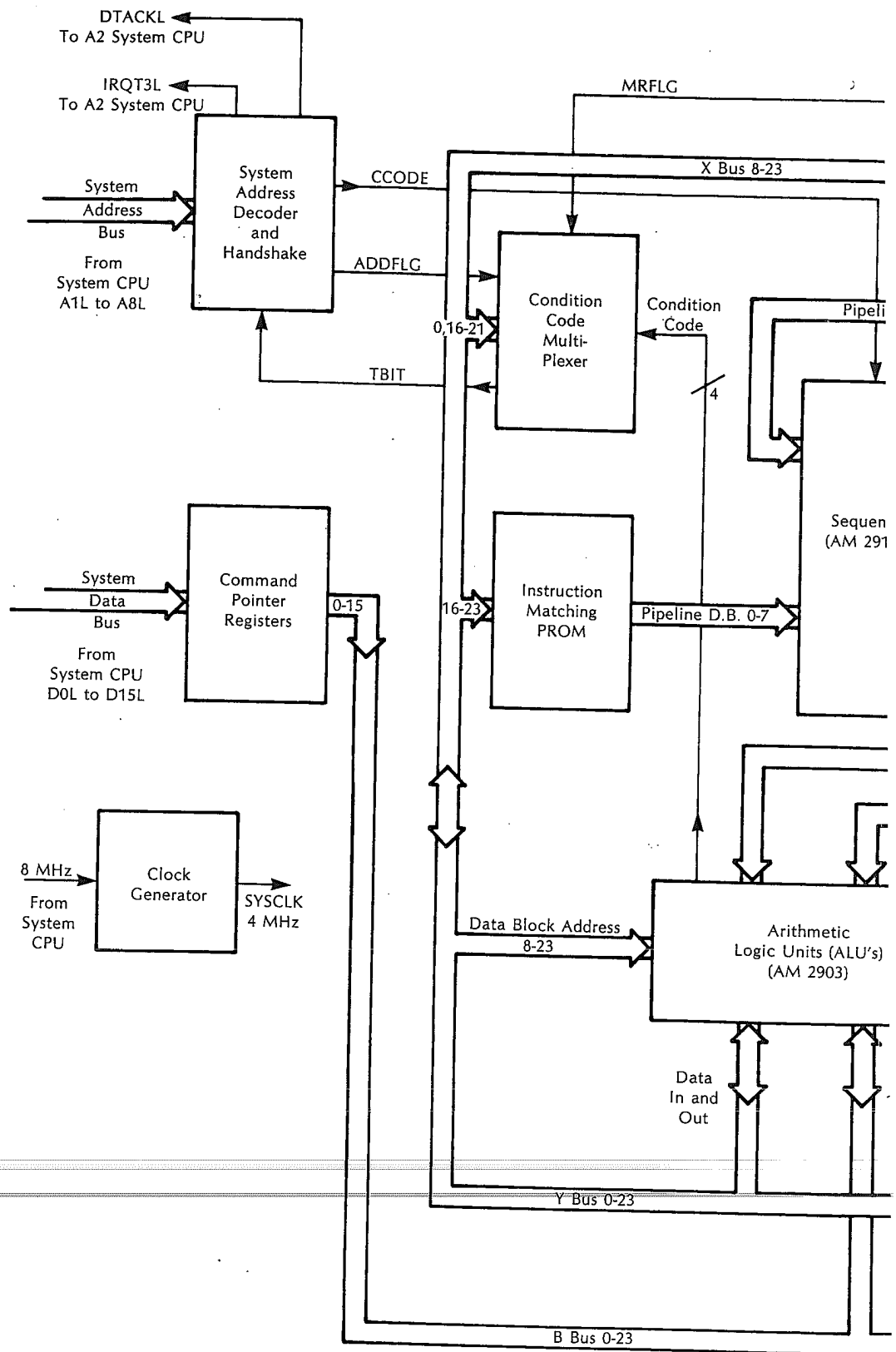
CN+4

From the most significant ALU (U310) indicating a carry-out of the ALU.

Internal Signal Descriptions

| | |
|------------------------------|---|
| CCA | CONDITION CODING |
| CCB | Output lines of the test and jump PROM which controls the |
| CCC | input selection of the condition code multiplexor. |
| CCEN | CONDITION CODE ENABLE Enables the condition code multiplexor. |
| CCODE | CONDITION CODE When the sequencer receives CCODE, it branches out of the wait loop and starts the FPP process. |
| CLKINHIY | CLOCK IN HIGH Y BUS Signal from control PAL 2 which clocks the global data bus into the Y8 to Y23 global bus registers. |
| CLKINLOWY | CLOCK IN LOWER Y BUS Signal from control PAL 2 which clocks the global data bus into the Y0 to Y7 and B17 to B23 global bus registers. |
| CLRIRQ | CLEAR INTERRUPT REQUEST Clears the Interrupt Request (IRQT3L). |
| CPDL | CONSTANT PIPELINE DATA Output signal of the B bus, Y bus control register which enables the pipeline data bus onto the Y bus. |
| EA | ENABLE A This signal from the bus control PROM selects the input to the ALUs (ALUs internal RAM or Y bus). |
| ENHIYOUTL | ENABLE HIGH Y BUS OUT Signal from control PAL 2 which enables the global bus registers output from Y8 to Y23 onto the global data bus. |
| ENLOWYOUTL | ENABLE LOW Y BUS OUT Signal from control PAL 2 which enables the global bus registers output from Y0 to Y7 and B16 to B23 onto the global data bus. |
| EXPL | EXPONENT This signal enables the global bus registers output onto the B17 to B23 bus lines. |
| I0 to I3 | SEQUENCER INSTRUCTION In test mode, these lines become the sequencer's instruction. |
| LDHIY | LOAD HIGH Y BUS Signal from control PAL 2 which latches the Y8 to Y23 into the global bus registers. |

| | |
|----------------|---|
| LDLOWY | LOAD LOW Y BUS Signal from control PAL 2 which latches the upper B16 to B23 into a global bus register and Y0 to Y7 into a global bus register. |
| MANL | MANTISSA This signal enables the global bus registers output onto the Y bus. |
| MYADDRL | MY ADDRESS Output signal of the address comparator to indicate the FPP assembly has been addressed by the A2 System CPU. |
| OPCLK | OPTION CLOCK This signal clocks the condition code of the FPP assembly into the condition code multiplexor. |
| QB0 | Q BIT 0 This input to control PAL 1 determines whether GA1L is low or high. |
| Q1 | OUTPUT 1 The output of control PAL 1 to control PAL 2 to indicate which half of a 32 bit global RAM transfer is to occur next. |
| SSADL | SET ADD Forces an add operation. |



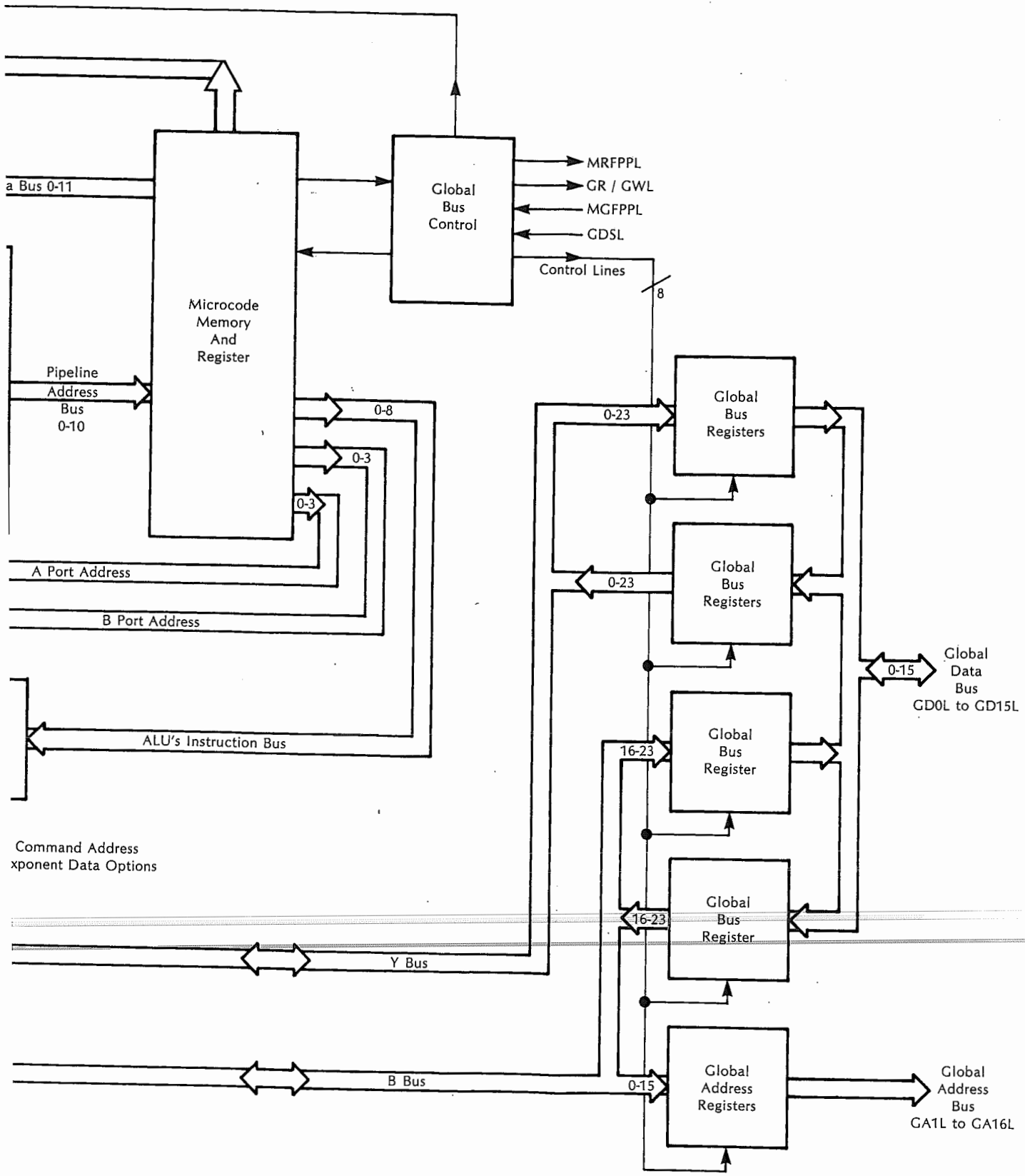


Figure 6-A7 FPP Block Diagram

6-9 A8, GLOBAL RAM/DISPLAY CONTROL A17, DISPLAY INTERFACE

The global RAM board stores data and arbitrates access to memory. It also works with the display interface board to control the transfer of data from memory to the display. Refer to the block diagrams in figures 6-A8a and 6-A8b and the schematic in figures 9-A8a and 9-A8b as referenced in the following circuit descriptions.

Arbiter

The arbiter section controls access to global RAM. Seven devices send memory request signals to the arbiter. The synchronizing register (U507) synchronizes the signals coming onto the board with respect to the global RAM. The priority decoder (U506) samples the memory requests periodically and allocates memory cycles based on the following priority list:

1. FFT, A9
2. DF1 (Digital Filter Channel 1), A5
3. DF2 (Digital Filter Channel 2), A5
4. RFSH (Memory Refresh), A8
5. B2D2 (Display Interface), A17
6. FPP, A7
7. 68 (System CPU), A2
8. Idle (If no device has asserted a memory request, the memory/global bus transceivers are disabled to prevent memory access.)

The feedback network (U405, U407, U408, and U508) prevents any device from receiving two consecutive memory cycles. The only exception is the FPP, which is allowed two consecutive memory cycles if no higher priority device is requesting memory.

A two-wire handshake coordinates memory requests and grants. When a device wants memory access, it first sets up valid global address and data at its output bus drivers. The device then initiates handshaking by asserting its memory request line low. When the device is allocated a memory cycle, its memory grant line goes low. This signal enables the device's address and data bus drivers. The address flows to the global RAM address multiplexer and is multiplexed into the memory. Data then flows into or out of memory through the bi-directional bus drivers. The global data strobe (CDSL) signal goes high to indicate valid data is on the bus. The memory grant unasserts and the handshake is ended.

Global Timing

The global timing section consists of a delay line oscillator and gating logic. Three delay lines (U311, U312, and U411) each have ten taps, each tap delayed 10 ns from the previous tap. The output from the third tap of the third delay line feeds back through an inverter to the input of the first delay line. The polarity of the signal changes every 235 nsec (230 nsec through the delay lines plus 5 nsec through the inverter). The result is a 2.13 MHz square wave. This signal is tapped at several intervals along the delay lines and passed through combinations of logic gates to generate timing signals.

Dynamic Memory Array

The RAM itself is a 64k by 16 bit dynamic memory array constructed from 16 64k by 1 bit dynamic RAM chips. The 16-pin RAM chips have 8 address input lines and require address multiplexing to receive 16 address bits.

Address Multiplexer and Address Drivers

The address multiplexer (U611 and U612) multiplexes the 16 global address lines and transfers the address 8 bits at a time to memory through the memory address drivers (U111 and U211).

Memory Control Drivers

The memory control circuit generates the row address strobe (RASLL and RASUL) and column address strobe (CASLL and CASUL) signals. These are clock signals which strobe the multiplexed address into the RAM.

Memory Refresh Timer and Refresh Address Counter

The dynamic global memory must be refreshed to prevent loss of data. Every 8.5 μ s the memory refresh timer (U404) sends a memory refresh request (MRRFSL) to the arbiter. When the arbiter issues a memory refresh grant (MGRFSL), the output of the address multiplexer is disabled. The refresh address counter (U511 and U512) is enabled. The output is applied to the memory address drivers to set up the memory row to be refreshed. The row address strobe signals (RASUL and RASLL) are enabled and a read memory operation refreshes the RAM memory row.

Global Bus Transceivers

The global bus transceivers (U609 and U610) are bi-directional, inverting buffers which transfer data between the global data bus and memory locations. The RAMGR/GWL signal determines the direction of flow (if high, the transaction is a read cycle; if low, it is a write cycle).

Display Control/Interface

The display is presented to the viewer in the form of a frame. A frame consists of from 3 to 20 buffers (e.g. data, grid, scales). Each of these buffers has a predefined size and location in global memory. The display control/interface section monitors and directs the flow of this data to the 1345A display in response to control commands from the A2 System CPU.

DISPLAY CONTROLLER (A8)

The display controller (U303) is a field programmable logic sequencer or state machine. Among the inputs to the display controller are address and control lines from the system bus. The synchronizing register (U302) synchronizes the control inputs with the 8 MHz clock from the system CPU.

DISPLAY DMA WORD/ADDRESS COUNTERS (A8)

The system CPU puts the beginning address and the length of each buffer on the system data bus. They are clocked into the display DMA word (U400, U401, U500) and address (U600, U601, U602, U603) counters by the ALOADL and WLOADL signals from the display controller. Each time a display memory grant is asserted, the address from the address counters flows through the display address drivers (U604, U605) to the memory address multiplexer. After the display data has been transferred to the display interface board (A17), the count enable line (COUNT ENL) is asserted low. The address counters increment and the word counters decrement by one. This process continues until the entire buffer has been transmitted to the display interface. The word counters have gone to zero, asserting the TCL (terminate count) line low. This signal generates an interrupt to inform the system CPU that the buffer transmission is complete.

DISPLAY REFRESH TIMER (A8)

The display must be refreshed at a rate of 60 Hz or greater. U101 divides down the 8 MHz clock to 61 Hz. U201 is clocked by this 61 Hz signal and puts out a SYNC pulse every 16.4 msec. Each time the system CPU starts a new display frame it sets D15 on the system bus. This signal is used to reset the display refresh timer to coordinate the sync pulses with the new frame information.

DISPLAY INTERFACE (A17)

One section of the display interface board buffers information and control signals from the global bus to the 1345A display. This circuitry consists of two inverting registers (U1, U2) for the data lines and a non-inverting bus driver (U3) for the control lines.

The other section of the interface board is the output protection circuitry between the display X, Y, and Z outputs and their respective rear panel connectors.

Internal Signal Descriptions

ALOADL Address load, active low. Allows the contents of the system address bus to be loaded into the display address counter.

~~**ARML** Arm, active low. Clears the display refresh timer to synchronize the beginning of the frame with the negative to positive assertion of the SYNC signal.~~

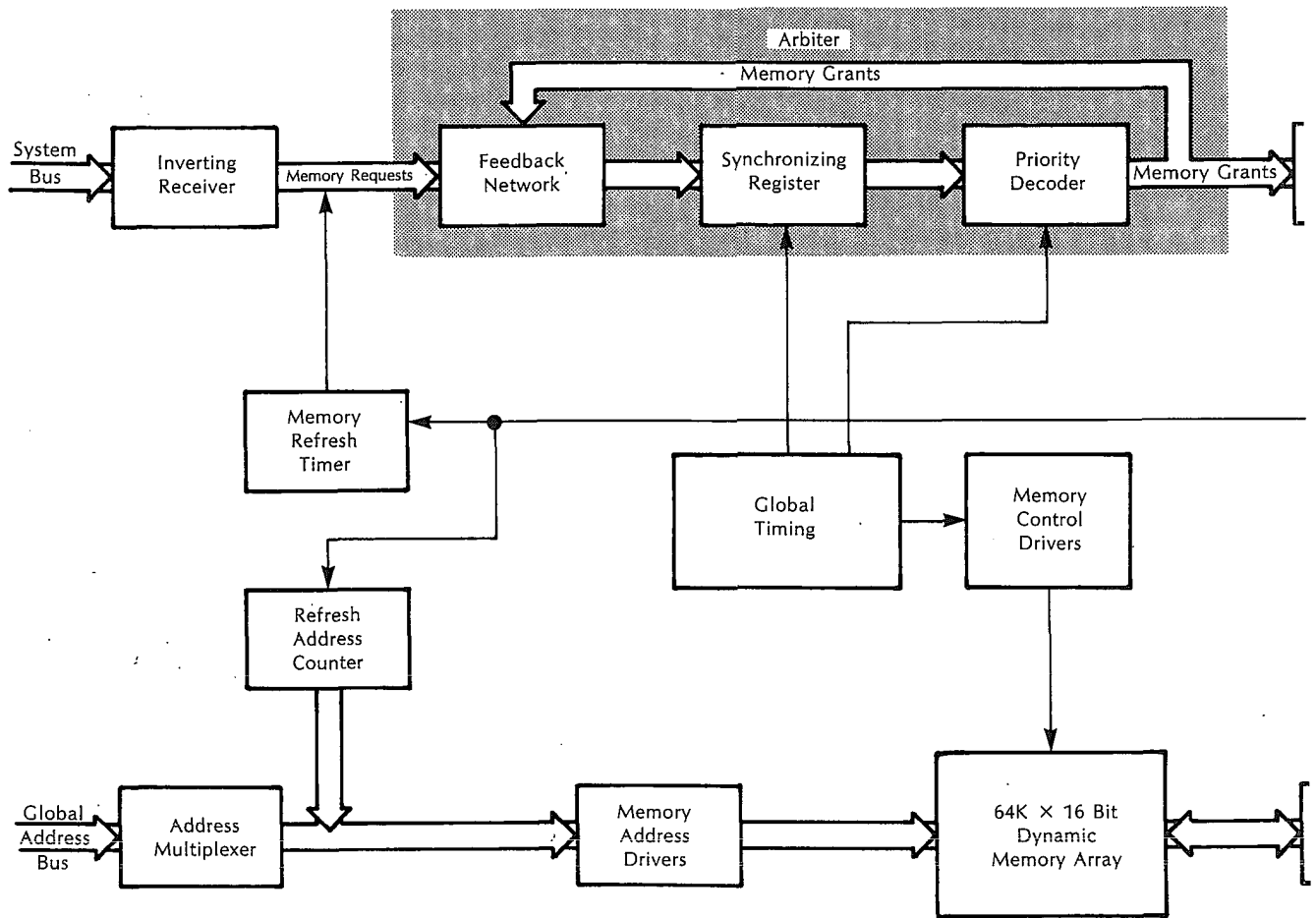
BRSTL Board reset, active low. Software reset for the global RAM board, originates from the system CPU.

BUS EN1 Timing signals which enable the global bus to perform a transaction.
BUS EN2

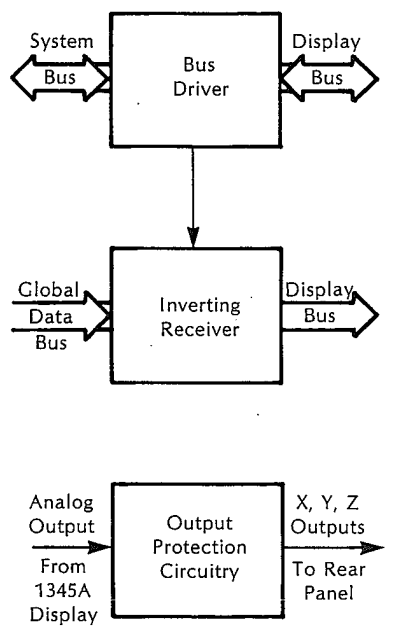
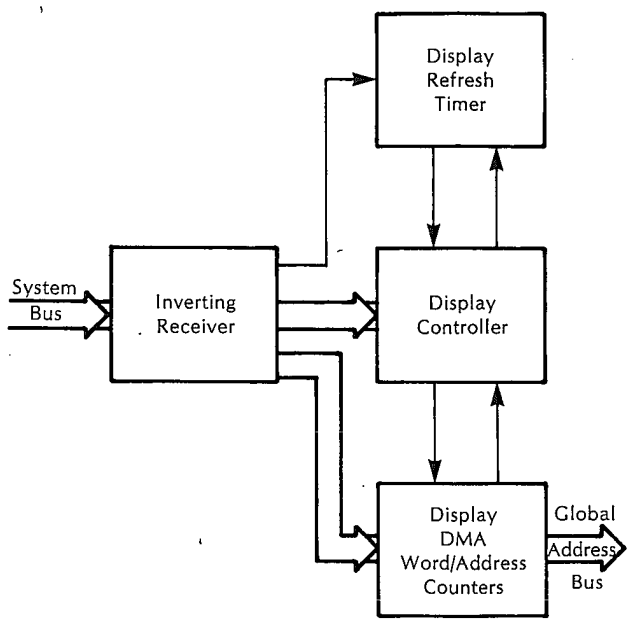
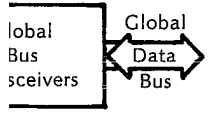
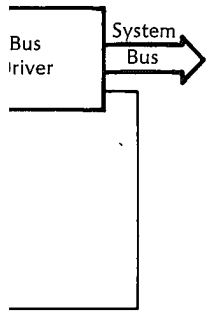
C0 Counter address bus lines 0 through 7.
through
C7

| | |
|---------------------------------|--|
| CASLL CASUL | Column address strobes. Clock the multiplexed address into the dynamic RAMs. |
| CLK | 8 MHz clock. The 8 MHz system clock used to synchronize the global RAM board to the system CPU. |
| CD | Chip disable. Turns the global bus transceivers on (low) and off (high). |
| COUNT ENL | Count enable, active low. Increments the memory address counter and decrements the memory word counter for each word transfer to the display. |
| D15 | Set data bit 15. Set by the system CPU at the start of a new frame. Sets the ARML signal to clear the display refresh timer. |
| DAMUXL | Disable address multiplexer, active low. Opens the output of the address multiplexer so that the refresh address counter can be used for setting the global address lines. This is the inverse of the arbiter circuit signal YD, which indicates a memory refresh grant. |
| GD0 through GD15 | Global data lines between dynamic memory and global bus transceivers. |
| GSMP | Global sample. A 4.26 MHz clock produced by the delay line timer and used as the clock for the synchronizing register. |
| IDLEL | Idle, active low. Ensures that global RAM does not change when there is no memory grant asserted. |
| MA0 through MA7 | Memory address bus lines 0 through 7. |
| MCAS MRAS | Master column (row) address strobe. Timing signals to the memory control drivers when the address is valid. |
| MGB2D2L | Memory grant, display, active low. |
| MGRFSHL | Memory grant, memory refresh, active low. |
| MRB2D2 | Memory request, display. |
| MRRFSH | Memory request, memory refresh. |
| PWRON | Power on. Signal from system CPU to global timing circuit to ensure global timing is initialized at correct frequency. |
| RAM GR/GWL | RAM global read/global write, active low. Triggers the global bus transceivers. When low, the transfer is a write cycle. When high, the transfer is a read cycle. |

| | |
|------------------------------|--|
| RAM GRL/GW | RAM global read (active low)/global write. Used to generate the WEL signal to allow a write transfer into memory. |
| RASLL RASUL | Row address strobes. Clock the multiplexed address into the dynamic RAMs. |
| RFDL | Ready for data, active low. Signal from display to inform controller that previous data point has been processed and a new data point is required. |
| ROW EN | Row enable. Switches the output of the address multiplexer. |
| RSTL | Rest. Software reset for the global RAM board, originates from the system CPU. |
| STROBE | Signal from global timing circuit used to generate global data strobe (GDSDL). |
| SYNC | Output of the display refresh timer, used to synchronize frame refresh (approximately 61Hz). |
| TCL | Terminate count, active low. Indicates that the display word count has gone to zero. |
| WEL | Write enable, active low. Allows a write transfer into memory. |
| WLOADL | Word load, active low. Allows the word count from the system CPU to be loaded into the display word counters. |
| YA through YH | Memory grant lines from the priority decoder to the bus driver. |



6-A8a Global RAM



A8 Display Controller

A17 Display Interface

6-A8b Display Controller / Interface

6-10 A9, FAST FOURIER TRANSFORM (FFT) PROCESSOR

The Fast Fourier Transform (FFT) processor board performs windowing, Fast Fourier Transform, and inverse Fast Fourier Transforms as specified by the System CPU (A2). Input and output data are stored in memory blocks in the global RAM. The FFT board performs the memory access (controls the global bus) to move these blocks to and from global memory (on the global bus). Input data may be real or complex, for one channel or two.

The description of how the FFT works covers operation at the system level (between the FFT board and the system CPU) and at the board level. Refer to the block diagrams in figures 6-A9a and 6-A9b and the schematic in figure 8-A9 for the following discussion of the theory of operation.

FFT Interaction with the CPU

The FFT board is controlled by the system CPU (A2) through the system bus. The FFT board appears to the main CPU board as a set of registers. These registers (sometimes called pseudo-registers) exist as RAM inside the FFT microprocessor chip.

FFT I/O is not synchronized with other activity on the global bus. The FFT requests control of the global bus for direct memory access (DMA) whenever it is necessary to get input data or store output data. The FFT has the highest priority interrupt status in the DMA chain. Memory access is provided within 500 ns of the FFT memory request.

FFT Microprocessor System

The FFT microprocessor (U103) is a TMS320 running at 5 MHz. The crystal oscillates at 20 MHz but the TMS320 divides that by four. The TMS320 and its ROM (U301 and U303) form a complete microprocessor system. The data bus between the TMS320 and its ROM is connected to the FFT internal data bus through a transceiver. The rest of the circuitry on the board appears to this system as individual I/O ports. The ports are activated by addressing combinations which activate the port decoder. The circuits that are not directly controlled by the TMS320 through the port decoder are indirectly controlled through the hardware control register.

Port Decoder

The port decoder (U216 and U217) is used by the TMS320 system to control the circuitry on the FFT board. This circuitry appears to the TMS320 as I/O ports on the internal data bus. The TMS320 enables ports through address and control lines which are input lines for the port decoder. When an address corresponding to a port appears on the address bus and the control lines are enabled, the port decoder selects one of thirteen lines to activate. These lines are described in the first part of the internal signal descriptions at the end of the FFT circuit description.

Hardware Control Register

The hardware control register (U405 and U406) is used to control circuits that are not directly connected to the internal data bus. It appears to the TMS320 as a write-only register on the internal data bus and is activated through the port decoder. It allows the TMS320 to control the global bus I/O sequencer, control the type of transform done, keep track of the level and scale factor during the transform, and monitor scale factors and execution status.

Address Generation

The FFT board must create addresses for the data input from and output to RAM when it has control of the global bus. This function is a major portion of the activity on the FFT board. The block entitled Address Generation on the main block diagram has its own block diagram made up of the blocks listed as follows. Refer to figure 6-A9b for the following discussion.

- I/O Sequencer
- Sequence Decoder
- Counters One and Two
- Address Translator
- Page Register
- Coefficient ROM

I/O SEQUENCER

The I/O sequencer (U117) controls the I/O process when the FFT board has control of the global bus. It manages the timing for global bus I/O and directs the generation of addresses used to transfer data to and from global RAM. The TMS320 system controls the I/O sequencer through the hardware control register. The sequencer is synchronized to the TMS320 operations through the port decoder to tell the sequencer when the TMS320 has accessed or provided data for the next I/O operation. The sequencer also initiates handshaking when the FFT needs memory access.

SEQUENCE DECODER

The sequence decoder (U115) decodes the outputs of the I/O sequencer. When the TMS320 begins a new level (the Fast Fourier Transform is performed in "levels", five of which are called "butterfly routines") it initializes the sequencer by activating LDHWCRL (load hardware control register). This signal from the port decoder also presets the sequencer (U117), starting the sequencer process. The memory access process is as follows:

- The sequencer asserts REQGBL (request global bus) to the global bus handshaking circuitry which produces a memory request (MRFFTL) to global RAM.
- When the memory grant (MGFFTL) comes back from global RAM the bus request is deactivated.
- If it's a read operation the read registers get loaded by GDSL (global data strobe). If it's a write operation, the write registers on the global data bus are enabled and the GR/GWL (global read/global write) signal is set low.
- When global RAM removes the memory grant signal (signaling that the cycle is complete) the address, data, and global write lines are all deactivated.

COUNTERS ONE AND TWO

Address generation begins with two counters. Counter One (U209 & U210) is an up-counter. Counter Two (U409-U411) is a loadable, count-up or count-down counter on the internal data bus. Counter Two appears as a write-only port to the TMS320 system. Typically, one counter is used to keep track of input addresses while the other is used to keep track of output addresses. The output of one of the two counters is selected by the counter multiplexer (U309-U311) to drive the address count bus.

ADDRESS TRANSLATOR

The address translator (U313 & U314) consists of 2 PAL ICs used to convert addresses on the address count bus to addresses on the FFT address bus depending on the FFT level and whether a read or a write operation is required. Several bits from the hardware control register are used to determine how the data on the address count bus is changed to FFT address bus data. PASSBIT0 is a control line (see schematic) used to mask off the least significant bit of the address during a complex transform requiring access to only even (real) window coefficient addresses.

PAGE REGISTER

The upper bits of the FFT address bus come from the Page Register (U312). This register on the internal data bus is a read-only register activated by the port decoder. It selects the RAM location for input and output blocks. The TMS320 sets the inputs which are written to (once) at the beginning of the transform. The page register specifies the four most significant bits of the FFT address bus dependent on whether the memory access is a read or a write (state of the FFTWR signal) and whether the information being accessed is window data or FFT data (state of the WINDPGL signal). (User defined windows are stored in RAM.)

COEFFICIENT ROM

The coefficient ROM (U315 and U317) appears on the internal data bus as a read-only register activated by the port decoder. The FFT address bus drives the ROM inputs. The purpose of this circuit is to convert FFT address information into coefficients used by the TMS320 system for the transform process.

Bus Interface

There are two busses connected to the FFT board; the system bus and the global bus. Each is composed of address lines and data lines. The system bus allows communication between the system CPU and the TMS320 system. The global bus allows the TMS320 system access to the global RAM which holds user defined window information and data for the Fourier transformation. The FFT board handles all memory access directly by requesting memory and controlling the global bus. The interface hardware consists of the following blocks:

System bus interface:

- System address bus buffer
- System data bus interface
- FFT interrupt circuit
- CPU interrupt circuit

Global bus interface:

- Global address bus interface
- Global data bus interface
- Global bus handshaking circuit

SYSTEM ADDRESS BUS BUFFER

The system address bus buffer (U505) appears as a read-only port to the TMS320 system. This register is used to tell the TMS320 processor which port the system CPU wants to access on the FFT board. These ports exist as RAM registers inside the TMS320.

SYSTEM DATA BUS INTERFACE

The system data interface (U506-U509) appears as one read-only register and one write-only register to the TMS320 system. Each is activated by the FF port decoder. These registers are used to transfer data between the FFT board and the system CPU (A2).

FFT INTERRUPT

The FFT board is controlled and monitored by the system CPU through the use of pseudo-registers inside the TMS320 integrated circuit. When the system CPU executes a write or read to one of these ports, the interrupt circuit on the FFT board generates an interrupt signal which is sent to the TMS320.

The FFT interrupt circuit consists of an identity comparator connected directly to the incoming system address bus. When the system CPU addresses the FFT board, the identity comparator (U510) in the interrupt block activates the BRDSELH (board select, active high) which generates an interrupt for the TMS320.

To determine which (pseudo) register the system CPU is requesting access to, the FFT interrupt service routine reads the address bus (through the address bus buffer, U505) onto the internal data bus. When the address is read, the interrupt is cleared and the data is transferred in the appropriate direction through the system data bus.

If the CPU is writing to the FFT board, the TMS320 reads the data registers by asserting the SDBUSINL (system data bus in) signal which activates DTACKL (data acknowledge). When the system CPU receives the DTACKL signal, it removes (or changes) the address, which deactivates BRDSELH, which deactivates DTACKL. If the FFT is writing to the CPU, the FFT puts the data on the output data registers (a write operation) and performs a (dummy) read to activate DTACKL, telling the CPU that the data on the bus is valid. When the CPU finishes reading the data it removes the FFT address, which deactivates BRDSELH, which deactivates DTACKL.

CPU INTERRUPT

The CPU interrupt circuit consists of an R-S flip-flop with two Reset inputs and one Set input. Inverters are used in pairs to ensure a single TTL load on the system bus. The RESETL signal from the system resets the CPU interrupt circuit to ensure that the FFT board does not have an impending interrupt request after a reset.

The FFT performs a CPU interrupt by activating the SIRQSYSL (set interrupt request, system) line which activates IRQ4L on the system bus. When the system CPU runs its interrupt service routine, it reads the status register on the FFT board and the TMS320 resets the interrupt.

GLOBAL ADDRESS BUS INTERFACE

The global address bus interface (U511 and U512) is a latch circuit which exists between the FFT address bus and the global address bus. These latches are clocked when the FFT board requests control of the global bus and are enabled when the FFT board is granted control of the bus.

GLOBAL DATA BUS INTERFACE

The global data bus interface appears as one read-only register and one write-only register to the TMS320. They are enabled by signals GDBINL and GDBOUTL from the port decoder.

GLOBAL BUS HANDSHAKING

This block is used to coordinate data transfers between the FFT board and global RAM. When the FFT board needs access to memory, it requests control of the global bus by activating REQGBL (request global bus) signal to the handshake block. This activates the MRFFTL (memory request from FFT) signal going off the FFT board. When the MGFFTL (memory grant to the FFT) signal becomes active, the memory request is removed and the read or write is performed through the global data bus interface. If the operation is a read, the GDSL (global data strobe) signal is used to indicate when the data on the bus is valid. If the operation is a write, the data is loaded into the write register at the same time the GR/GWL (global read/global write) signal is set low to indicate to the memory that the data on the bus is valid.

Pseudo-Scale ROM

All data operations are done in the TMS320 microprocessor. The only hardware doing math operations outside the TMS320 is the pseudo-scale ROM (U305). It looks at the internal data bus on each data write cycle and compares the upper eight bits to values stored in memory. The two output lines are reclocked by flip-flops in U208. The TMS320 clocks them when it puts something on the global data bus. The flip-flops store the largest value output for that particular pass of the FFT. Before beginning the next pass, the TMS320 examines (and clears) the DIVBY4 and DIVBY2 lines (from the flip-flops) to see how big the data was on the last pass; it then can select a scale for the next pass.

Butterfly Subroutine Address ROM

The TMS320 keeps track of the address process via the Butterfly Type PLA (U207) and the Butterfly Subroutine Address ROM (U502)-hereafter referred to as the Butterfly ROM. The Butterfly ROM is a read-only port on the internal data bus which is activated by the port decoder. The TMS320 uses information from this logic to keep track of execution status of the transform to guide its math operations (help select subroutines). Depending on where execution is in the pass, the TYPE2BF line from U207 tells the ROM which of two types of butterfly routines to execute.

Test Bit Mux

The test bit multiplexer (U206) selects the the TMS320 test bit (BIO320). This allows the TMS320 to examine the scale-compare flip-flops in U208 and examine the PASSDONE bit which comes from the sequencer telling the processor when execution has finished a level. It can also examine the PRN bit from U105.

Pseudorandom Number Generator

This circuit provides a bit that is randomly high or low. The FFT processor uses this information to do a math routine called dithered rounding.

LED Register

LED register (U202) is a write-only register on the FFT internal data bus. It drives the LED arrays CR101 and CR102. One line is used as the start/stop signal for digital signature analysis (DSA). Another line is used to clear the pseudorandom generator.

Internal Signal Descriptions

PORT DECODER OUTPUTS

| | |
|------------------|--|
| SIRQSYSL | Set interrupt request to system, active low. |
| RIRQSYSL | Reset interrupt request to system, active low. |
| GDBINL | Global data bus in, active low. |
| GDBOUTL | Global data bus out, active low. |
| SDBUSINL | System data bus in, active low. |
| SDBUSOUTL | System data bus out, active low. |
| SABUSINL | System address bus in, active low. |
| PROMINL | Coefficient-ROM read, active low. |
| LDPGSL | Load page register, active low. |
| LDHWCRL | Load hardware control register, active low. |
| LDCTR2L | Load counter two, active low. |
| CLRSCALEL | Clears the scale data in the pseudo-scale ROM output flip-flops, active low. |
| BFSUBADL | Butterfly subroutine address, active low. |

HARDWARE CONTROL REGISTER OUTPUTS

| | |
|---|--|
| WINLOC | Window location. The data for the standard windows is on the FFT board; the data for user defined windows are kept in global RAM. |
| BNKSELH | Bank select, active high. Selects upper or lower 32k of memory. |
| SWAP | Swap two halves of the time buffer. |
| CTR2DNL | Set counter two to count down, active low. |
| TWOCH | Measurement is two-channel as opposed to single channel. |
| REALDATA | Data is real as opposed to complex. |
| SEQSEL0 SEQSEL1 | These two lines select one of three sequences for the I/O sequencer; this tells it how to control the counters and page register depending on whether the execution is processing a window, an FFT, or a deinterlace (terms associated with FFT). |
| LEV2 LEV1 LEV0 | These three lines select one of seven levels within the FFT process. The seven levels are: window, five butterfly passes, and (if necessary) deinterlace. Each level processes an entire block of data in memory. The LEV signals help keep track of addressing. |
| TBSEL2 TBSEL1 TBSEL0 | These three lines are used to choose one of four signals used by the test bit mux. |
| SCALE1 SCALE0 | These lines are used to select one of three signals to convey information about the math results on the previous level to the page register. |

OTHER SIGNALS

| | |
|--|--|
| IDB0 through IDB15 | Internal data bus lines 0 through 15. |
| SDOUTENL | System data bus output enable, active low. |
| DIVBY4 DIVBY2 | Two lines conveying information from the pseudo-scale ROM to the TMS320 test bit mux concerning data size. |
| PASSDONE | Signals the end of a level! (see LEV). |
| DIDONE | Same as PASSDONE for the deinterlace pass. |
| IRQ320 | Interrupt request to the TMS320 microprocessor. |
| LDCAL | Load coefficient address, active low. Signal from the I/O sequencer which loads data on the internal data bus into the coefficient ROM address inputs. |

| | |
|------------------|---|
| CTR2B11 | Counter two, bit 11. Bit 11 on the FFT address bus (FA11) originates in one of two places: counter two or the page register. The signal from the page register is W11. The sequence decoder picks one of these two, depending on some other addressing criteria, and puts out FA11. |
| W11 | See CTR2B11. |
| FA11 | See CTR2B11. |
| CTR1ENL | Counter select, counter one is selected when low. |
| DEC2L | Decrement counter two, active low. |
| INC2L | Increment counter two, active low. |
| INC1L | Increment counter one, active low. |
| FFTWR | FFT write. Command from the I/O sequencer to the global bus handshake circuit to write. Also used in conjunction with the WINDPGL signal as input to the page register to determine address page to use depending on whether the operation is a read or a write and the data is window information or coefficient information. (It is not possible to write coefficient information). |
| WINDPGL | Window page, active low. Used in conjunction with FFTWR as input to the page register. See FFTWR. |
| PASSBIT0 | A signal ANDed with bit 0 on the FFT address bus so that it passes bit 0 when high and holds bit 0 low when low. See the discussion on the address translator. |
| GDINEMPTY | Global data input register empty. Indicates that there is no data waiting to be read from the global data bus registers. |
| CLREMPYTL | Clears the GDINEMPTY flip-flop. |
| GDOUTRDY | Global data output register ready. Indicates that data in the global data output register is ready to be read (valid). |
| CLRRDYL | Clears the GDOUTRDY flip-flop. |
| FFTMR | FFT memory request. This signal is active high between the time that the FFT board requests the global bus and the time that it is granted control of the bus. It is an input to the I/O sequencer. |
| FFTMG | FFT memory grant. This signal is a direct result of the FFT board being granted control of the global bus. It is an input to the I/O sequencer. |
| POSTINCL | Post increment, active low. Controls whether counters are incremented after a read or write. |

- REQGBL** Request global bus, active low. A signal from the I/O sequencer to the sequence decoder and the global bus handshake circuit requesting control of the global bus.
- LDGDBRL** Load global data bus register, active low. This signal loads data from the global data bus into the read registers. It is activated when the FFT is granted memory access and GDSL (global data strobe) becomes active (low).
- BIO320L** Branch on I/O, active low. A signal from the test bit mux to the TMS320 microprocessor.
- IRQ320L** Interrupt request to the TMS320 microprocessor, active low.
- BRDSELH** Board select, active high. Signal created by the identity comparator in the FFT interrupt circuit. This signal indicates that the system CPU is addressing the FFT board.

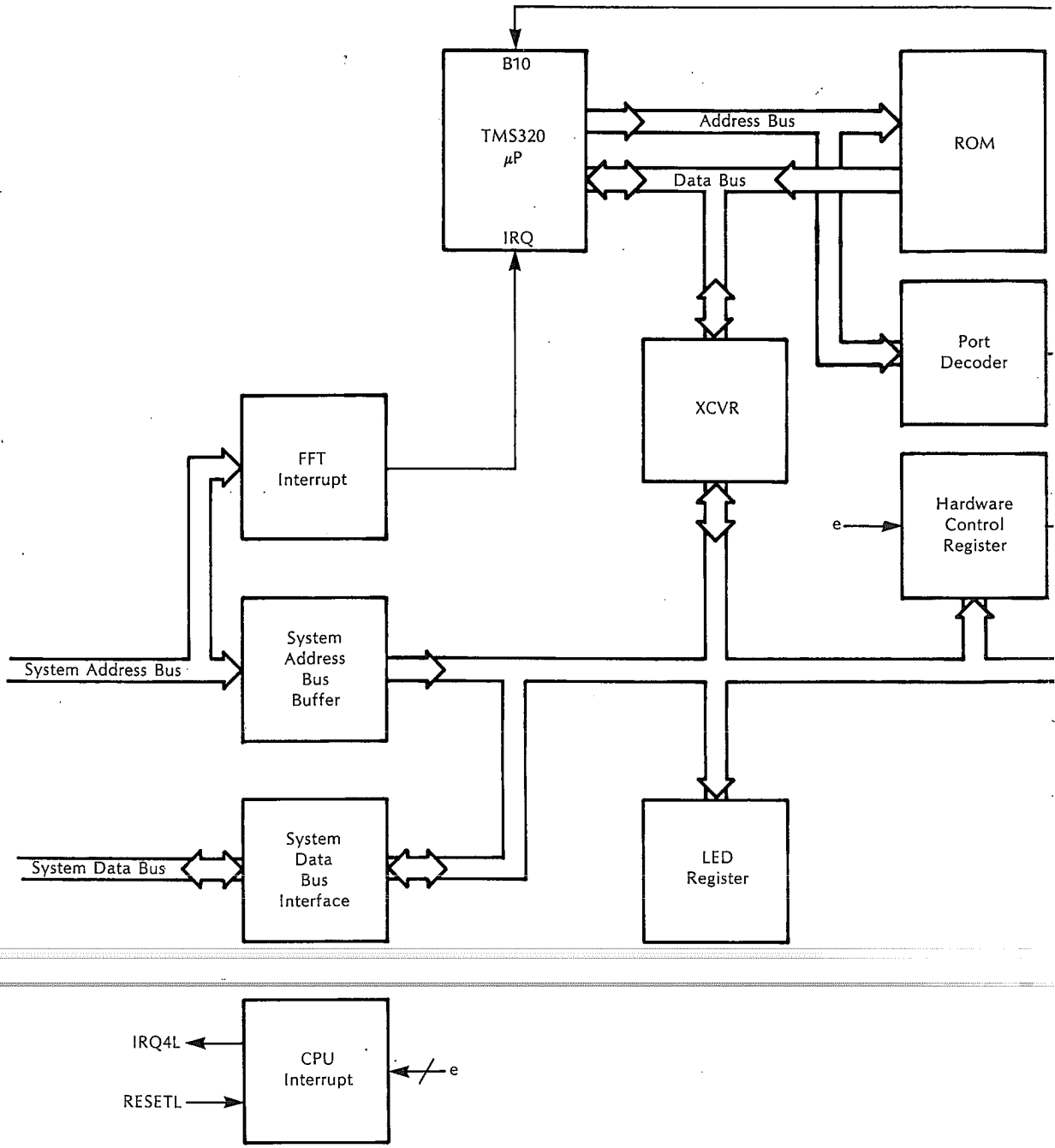
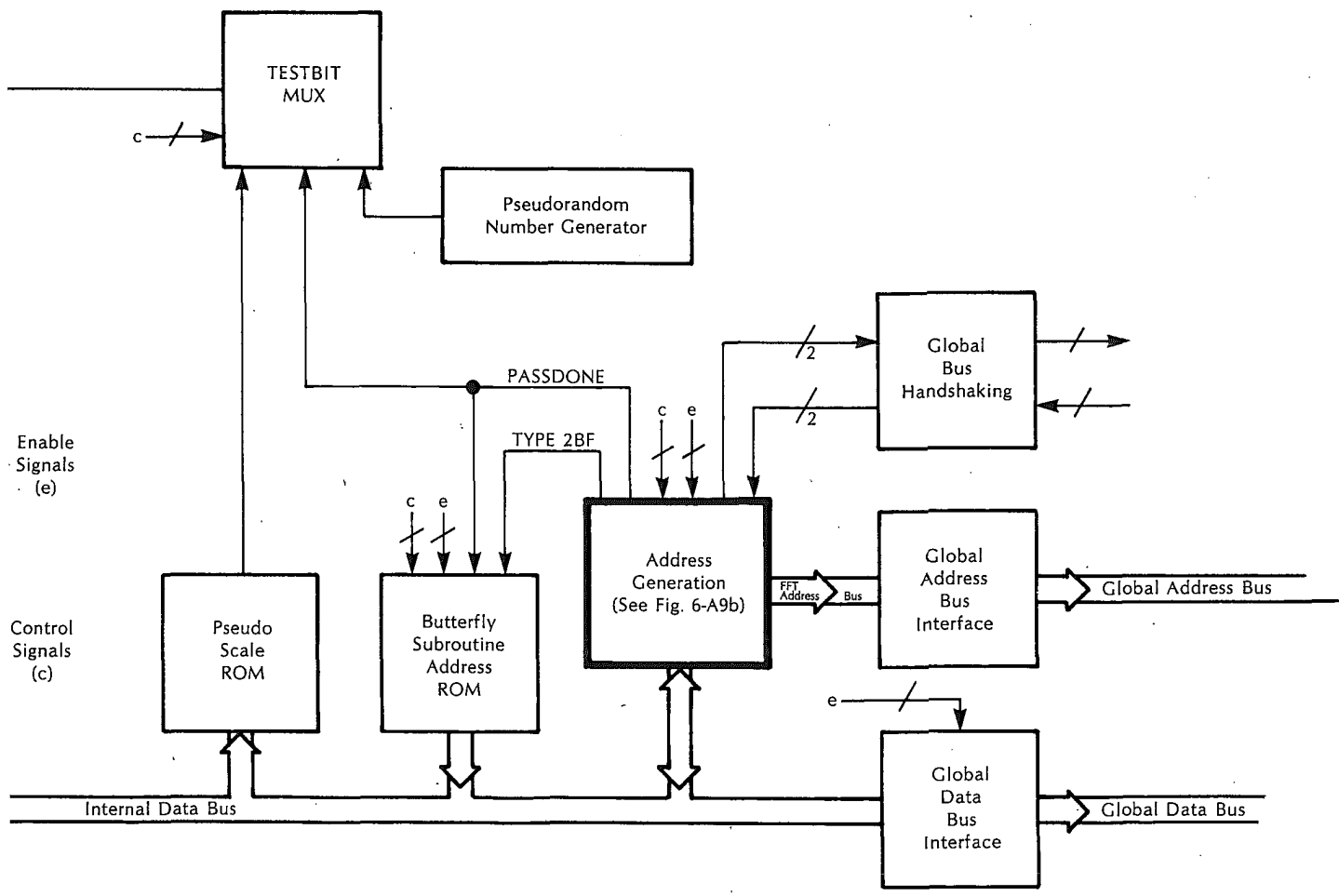
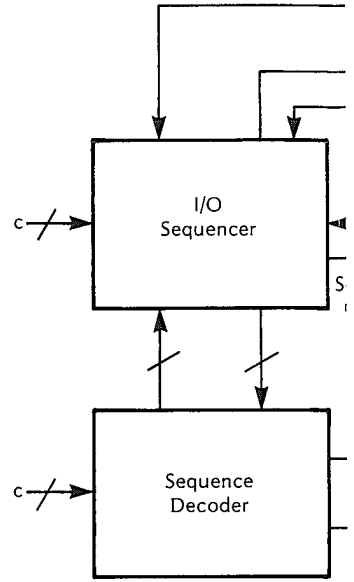
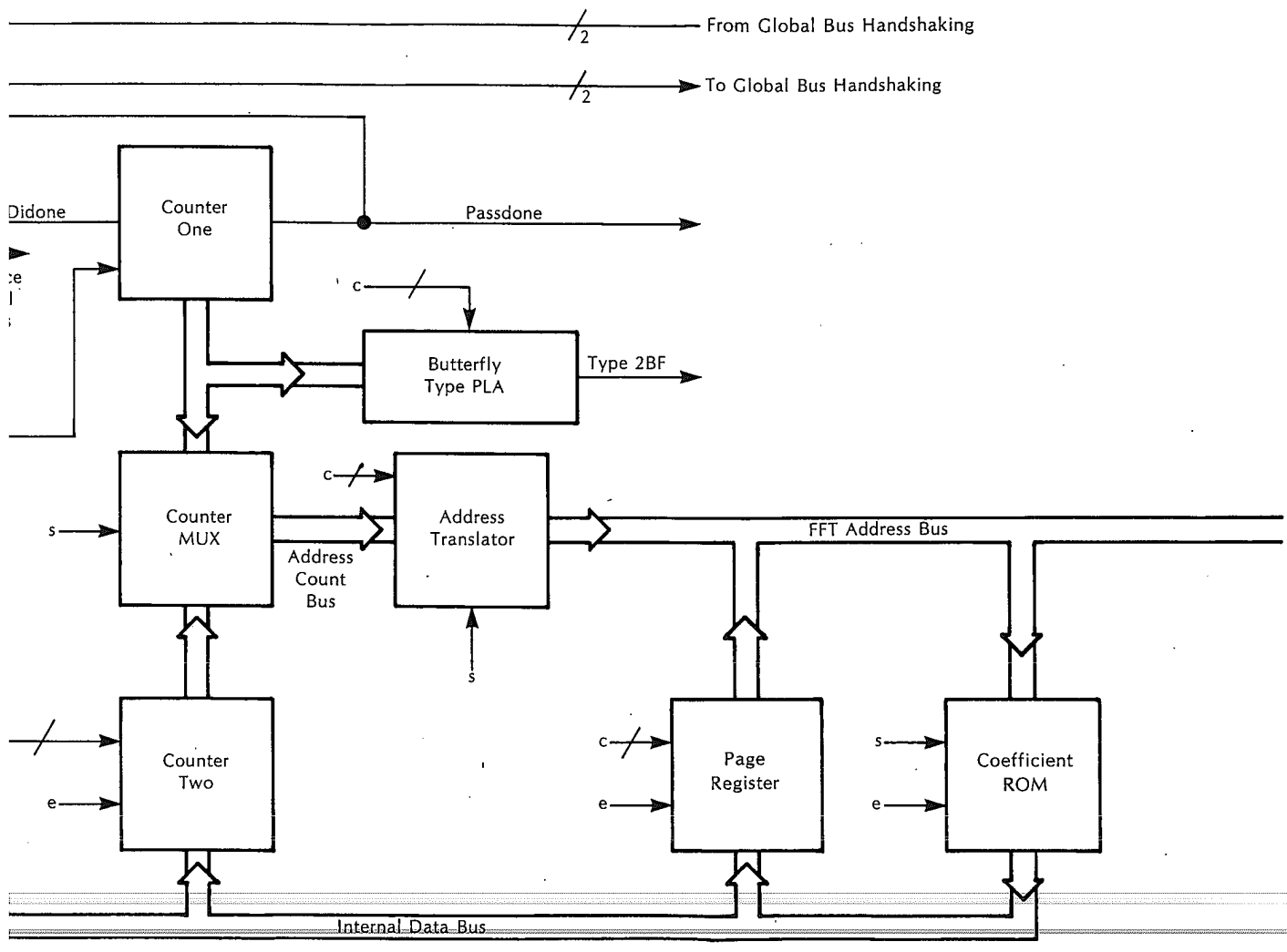


Figure 6-A5



562A FFT Board Block Diagram





6-A9b Address Generation Block

6-11 A15 KEYBOARD

Refer to figure 6-A15 for this discussion. The keyboard provides operator inputs to the HP 3562A as well as operation feedback in the form of status LEDs. The three major functions of this assembly are:

1. To send the code of any key pressed to the A2 System CPU.
2. To indicate operational status with LEDs.
3. To inform the A2 System CPU when the rotational pulse generators (RPG1, RPG2) have been enabled.

LED Indicators

The A2 System CPU sets the appropriate system data line (D0L to D7L) for the LED which is to be turned on. Next, the system processor asserts the instruction lines for the keyboard (A1L, A2L, WRITEL, KYBRDL). After these lines are set up, the address strobe (ASL) line is asserted which causes the keyboard processor to be interrupted by the keyboard select (Kysel) signal. When interrupted, the keyboard processor reads the instruction lines and causes LED1L or LED2L to latch the system data to the LEDs.

Front Panel Key Pressed

The keyboard processor continuously increments its output port except when it is interfacing with the system CPU. The output port controls a BCD-to-decimal decoder and multiplexer. When a key is pressed by the operator, an input line to the multiplexer is grounded and the KEY line is asserted. When the keyboard processor senses the asserted KEY line, it reads the matrix counter, and stores the value internally. At the same time, the keyboard processor asserts IRQ causing the interrupt request (IRQT2L) signal to be sent to the system processor.

The system processor always responds to a keyboard interrupt request by first sending a status request instruction to the keyboard. This instruction causes the following to happen:

1. The output register enabled (OREGENL) signal is asserted.
- ~~2. The keyboard status is put on the keyboard bus.~~
3. The status is stored in the data output register when OREGL is asserted.
4. The CLRPGl line is asserted to clear the IRQT2L line.
5. The DTACKL signal is sent to the A2 System CPU to indicate the data was transferred.
6. The A2 System CPU reads the status word to determine what has occurred on the keyboard.
7. The A2 System CPU sends an instruction to the keyboard processor to output the value stored in the keyboard matrix counter. This value is the key code.
8. The Key Code is read by the system processor to determine what key has been pressed.

In addition to reading the front panel keys the system processor can also sound the beeper when an error occurs. To sound the beeper, the A2 System CPU sends the beeper instruction to the keyboard. The keyboard processor sets the decoder output lines to activate the beeper.

Rotational Pulse Generators

The RPGs must be activated before they can be used. The signal lines XL and YL activate the marker RPG (RPG1) and the X and Y front panel LEDs. The ENABLED signal line activates the parameter RPG (RPG2). Since both RPGs operate in the same manner, only RPG1 is described.

After the A2 System Processor instructs the keyboard to turn on the X or Y LED, the input lines XL and YL activate the marker RPG; the output of the turn latch (RPG1) is set to a logic 1. When the RPG is turned, the clock of the turn latch toggles between TTL level high and TTL level low. The output of the turn latch (RPG1) toggles the clock of the direction latch. The output of the direction latch (DIR1) depends on the direction the RPG is turned. After the RPG1 and DIR1 signals are sent to the keyboard processor the following occurs:

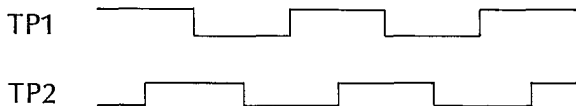
1. The keyboard processor polls the RPG1 and DIR1 lines and IRQT2L is sent to the A2 System CPU.
2. The system processor instructs the keyboard to send its status. The status word tells the system processor which RPG was moved and in what direction.
3. The keyboard processor asserts the Clear RPG (CLRPGL) line, clearing the turn and interrupt latches.

The system processor uses the information from the keyboard in the display routines. These routines increment the marker one location in the direction as indicated by DIR1 and DIR2.

As the RPG moves, the above steps are repeated until no further movement of the RPG is detected.

The outputs of the RPG appears as follows:

Clockwise:



Counterclockwise:

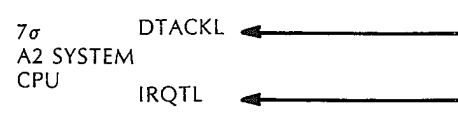
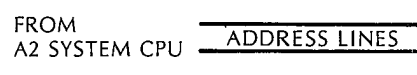
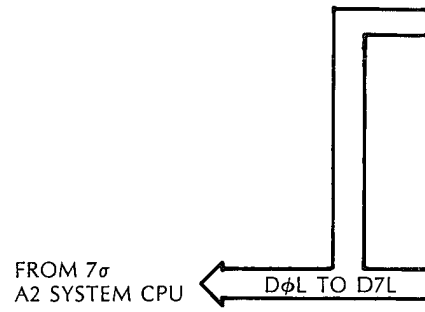


When the RPG latches are enabled, turning of the RPG causes the RPG1 line to go high. This clocks the direction latch.

Internal Signal Descriptions

| | |
|-------------------|---|
| CLRPGL | CLEAR ROTATION PULSE GENERATOR (RPG) Active Low Output of the keyboard device decoder. This signal clears the turn and interrupt latches. |
| DIR1 | DIRECTION of ROTATION of RPG1 Direction latch 1 send DIR1 to the keyboard processor to indicate which direction the marker RPG has been rotated. |
| DIR2 | DIRECTION of ROTATION of RPG2 Direction latch 2 sends DIR2 to the keyboard processor to indicate which direction the parameter RPG has been rotated. |
| ENABLEDL | ENABLED PARAMETER Active Low The LEDs latch 1 sets ENABLEDL low to light the Enable LED and activate Turn Latch 2. |
| EP0 to EP7 | EPROM0 to EPROM7 The keyboard EPROM sends instructions to the keyboard processor using these lines. |
| KACKL | KEYBOARD ACKNOWLEDGE Active Low Signal from the keyboard device decoder to clock DTACKL out to the A2 System CPU. |
| KAS | KEYBOARD ADDRESS STROBE Signal from the keyboard processor indicating addresses KA8 to KA12 are valid. |
| KB0 to KB7 | KEYBOARD BUS LINES 0 through 7 Keyboard data lines the keyboard processor uses for input and output. |
| KDS | KEYBOARD DATA STROBE The keyboard processor send KDS to the control circuit when there is valid data on KB0 to KB7. |
| KRD | KEYBOARD READ/WRITE This signal determines whether the keyboard processor is reading or writing on data lines KB0 to KB7. The keyboard control circuitry also uses KRD to set up input and output operations for the keyboard. |
| KROML | KEYBOARD ROM Active Low This signal from the keyboard device decoder enables the instruction ROM lines EP0 to EP7. |

| | |
|-------------------|---|
| KYSEL | <p>KEYBOARD SELECT Active Low The keyboard command register uses KYSEL to interrupt the keyboard processor when the keyboard has been addressed by the system processor.</p> |
| LED1L | <p>LED 1 ENABLE Active Low This signal clocks the system data bus through the LED's Input Register into the keyboard LED's Latch 1.</p> |
| LED2L | <p>LED 2 ENABLE Active Low This signal clocks the system data bus through the LED's Input Register into the keyboard LED's Latch 2.</p> |
| OREGENL | <p>OUTPUT REGISTER ENABLE Active Low When this signal is low, keyboard data from the data output register is put on the system bus.</p> |
| OREGL | <p>OUTPUT REGISTER Active Low This signal clocks keyboard data into the data output register.</p> |
| PA0 to PA7 | <p>PORT A0 to PORT A7 Port A lines are output lines of the keyboard processor. The keyboard processor uses PA0 to PA6 to set up the key matrix and uses PA7 to clock IRQT2L to the A2 System CPU.</p> |
| RPG1 | <p>ROTATION PULSE GENERATOR 1 When the marker RPG is moved, Turn Latch 1 sends RPG1 to the keyboard processor.</p> |
| RPG2 | <p>ROTATION PULSE GENERATOR 2 When the parameter RPG is moved, Turn Latch 2 sends RPG2 to the keyboard processor.</p> |
| XL | <p>X CURSOR Active Low Output signal of LED's Latch 1. It enables the X cursor LED and Turn Latch 1.</p> |
| YL | <p>Y CURSOR Active Low Output signal of LEDs Latch 1. It enables the Y cursor LED and Turn Latch 1.</p> |



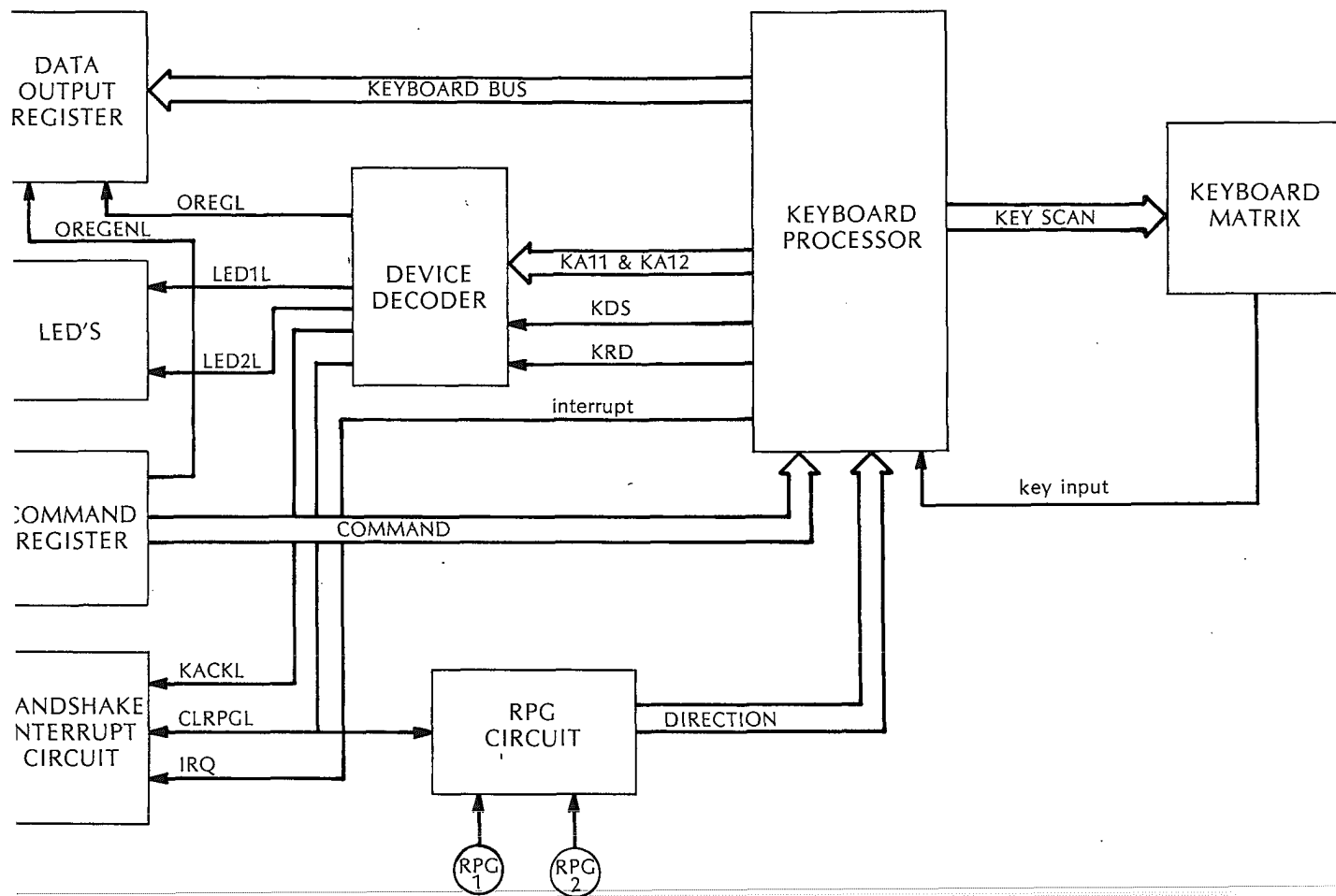


Figure 6-A15 Keyboard Block Diagram

6-12 A18 POWER SUPPLY

The HP 3562A power supply is a half-bridge switching power supply. It supplies 5 volts dc at 30 amps regulated power. It also supplies low power, linear regulated ± 30 Vdc, ± 15 Vdc, +8 Vdc, and +2.6 Vdc. The power supply operates with a line voltage from 84 Vac to 129 Vac and from 187 Vac to 255 Vac. The line frequency can vary from 47 Hz to 66 Hz.

Refer to figure 6-A18 for this discussion. The primary rectifier converts the ac line voltage to a high dc voltage with ripple. This dc voltage is fed into FET chopper switches to produce positive and negative pulses. The power output of the power supply increases and decreases with the pulse width. The pulse width is controlled by the pulse width modulator (PWM) compensating for line voltage and load variations. The control voltage used by the PWM to determine the pulse width is derived from the 5V supply. As the 5V supply deviates from the 5V reference voltage, the PWM reduces or increases the duty cycle of the FET chopper switches changing the output voltage. The output of the primary transformer is a square wave at 128 kHz which is rectified and filtered to make a dc output with ripple. The 5V supply and the secondary supplies then regulate the output to produce the dc voltages needed by the HP 3562A.

Turn On

At the moment the power supply is turned on, the primary capacitors and the bias power supply capacitors begin charging. The supply is not switching and the entire instrument is in the reset mode. The power down circuit monitors the bias supply's transformer to determine when the line voltage is at the correct level. When the voltage reaches the correct level, the power down circuit signals the PWM and the power supply starts switching. The slow start circuit is then triggered and the pulse width of the FET chopper switches increases slowly (0.1s) to its normal width. The slow start circuit is then triggered and the PWM slowly (0.1s) increases the pulse width to the correct level. As soon as the 5 volt output comes up to 4.75 volts, the PWRUP signal goes high and unlocks the A2 System CPU.

Primary Rectifier and RC Filter

This full-wave bridge rectifier and R-C filter network converts the ac power input to a high dc voltage between 236 Vdc and 364 Vdc with a 10V to 15V ripple. When switch S1 is set to the 115V position, the primary rectifier and filter functions as a voltage doubling circuit. When S1 is set to the 220V position, the primary rectifier and filter functions as a full-wave bridge circuit.

Bias Power Supply

The bias power supply is a linear, low power supply that provides power for the PWM, control circuits, and protection circuits. This supply takes its input directly from the ac line through its own transformer. The bias power supply provides ± 12 Vdc which rises and falls with the line voltage.

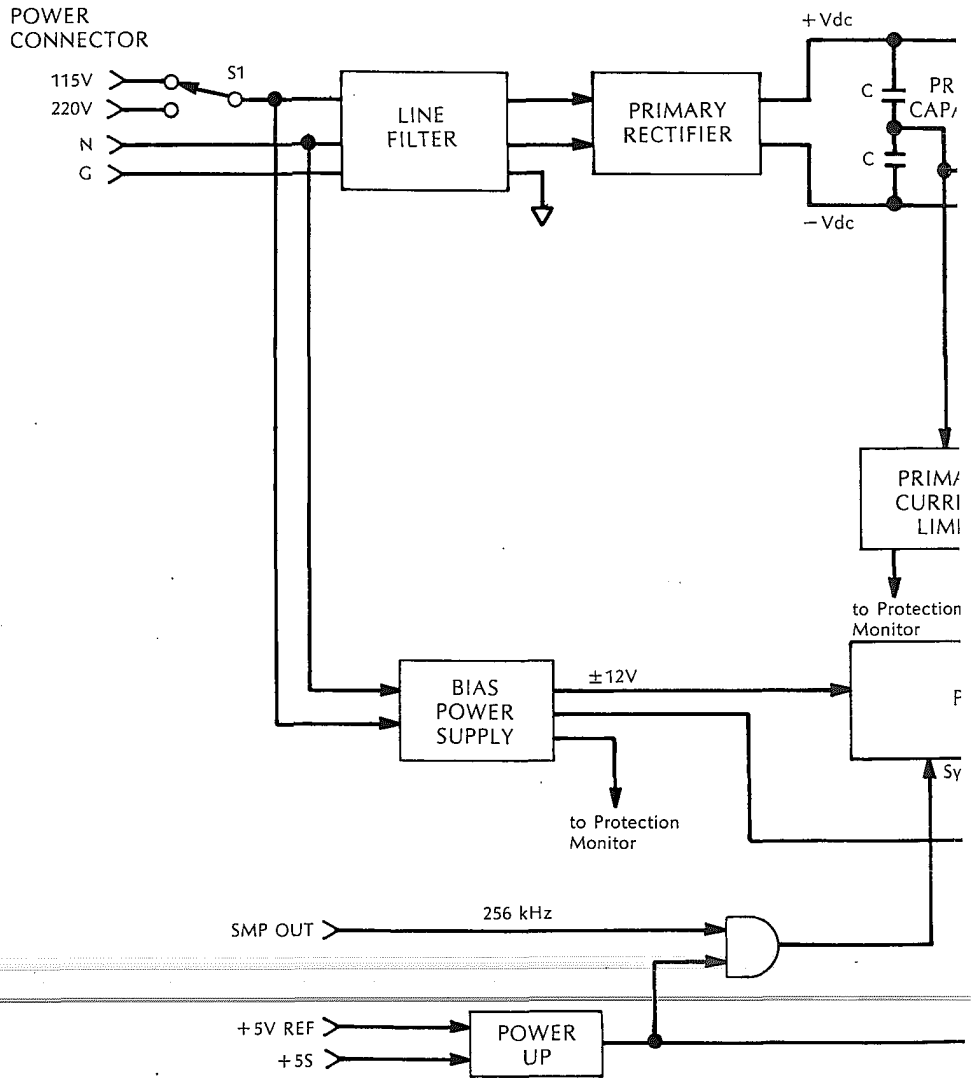
Pulse Width Modulator

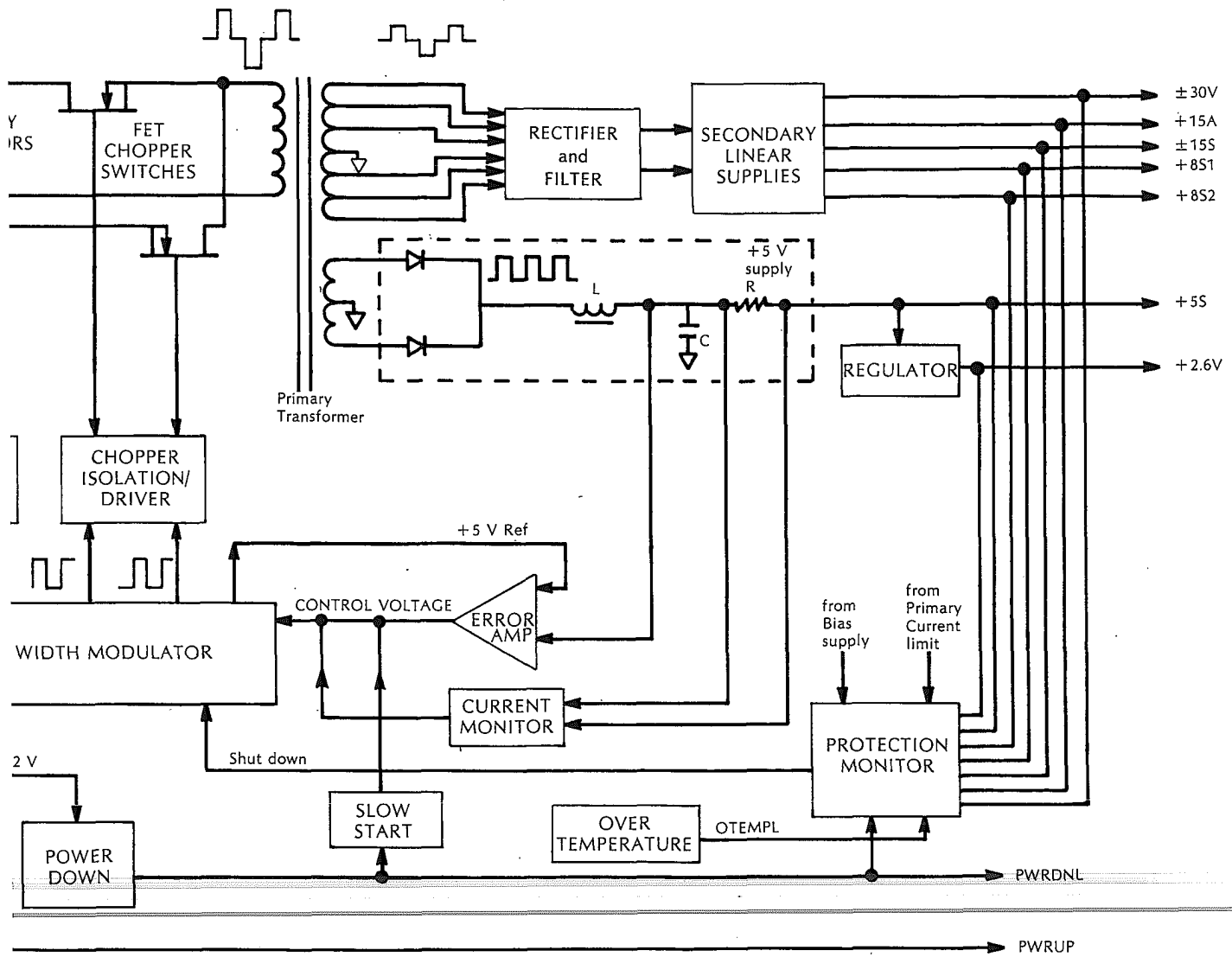
The voltage output of the power supply is controlled by the pulse width modulator (PWM). It drives the chopper switches in a manner which maintains a constant voltage output. The PWM compares the 5 Vdc voltage to its own internal reference using the error amplifier. This comparison determines the duty cycle of the FET chopper switches. The PWM contains its own internal oscillator and +5V reference. The PWM can be turned off by the protection monitor, power down, and current limit circuits.

Protection Circuits

There are five sections of protection circuits: the primary current limit, the power down, the current monitor, the over temperature circuit, and the protection monitor. The primary current limit circuit quickly shuts down the power supply when the current in the primary exceeds about 8A by shutting off the voltage supply of the PWM. If this fault occurs, the power must be cycled for the instrument to operate. When switch S1 is in the 115V position and the line voltage drops to less than 84 Vrms, the power fail sign (PWRDNL) becomes active. If the line voltage drops to less than 160 Vrms, PWRDNL becomes active (when switch S1 is in the 220V switch position). This signal goes to the protection and current monitors and the PWM is shut off. The power down signal also goes to the A30 Analog Source and the A2 System CPU to signal a power down is occurring.

The current monitor senses an over-current condition in the 5V supply. When this fault occurs, it reduces the control voltage to the PWM, which results in a reduction of the output power of the primary transformer. The protection monitor senses two things: over voltage in the positive supplies and if the voltages from the negative supplies rise above ground. When a voltage fault, current fault, power failure, or over temperature (OTEMP) occurs the protection monitor shuts off the PWM and lights the corresponding fault LED. The LED indicates which fault-detecting circuit was activated. All the LEDs are off during normal operation.





re 6-A18 Power Supply Block Diagram

6-13 A30, ANALOG SOURCE

The descriptions in this chapter are written to help you understand the operation of the circuits of the analog source board. The circuit functions are discussed beyond the block level but not to the component level. Refer to the A30 schematic for part and pin numbers while reading this circuit description.

The analog source board performs two functions: 1) converts digital information from the digital source board (for sinusoidal signals) into an analog signal available at the front panel, and 2) generates pseudo random noise (PRN) and square wave signals which are used to calibrate the input and ADC boards. Refer to the block diagram and schematic drawings for the following discussion.

Sine Wave Interface

The digital source board provides the source signal in digital form to the analog source board which converts it into the selected analog signal. The digital information enters the analog source board in a serial format as a signal called DACDAT at pin 39 and is shifted into serial-to-parallel shift registers U553 and U552. The clock used to shift in the data is on pin 40 and the enable signal is on pin 27. The parallel output is latched by U551 and U550 into the D/A converter (DAC) U551.

Source Signal DAC

U551 changes the digital information originating on the digital source board into an analog signal. The output is a current signal which is converted to a voltage signal by U350 and buffered by U352.

100 kHz LPF

The filter consists of passive components followed by an amplifier stage (U50) which buffers the filter and has enough gain to make up for losses in the filter and losses in U251 (next stage).

Attenuator

U251 is a multiplying D/A converter used to control the amplitude of the source. The analog source signal from the 100 kHz LPF is connected to pin 15 which is the reference voltage input for the DAC. In this configuration the circuit performs as a step attenuator such that its output is 0 V when all control lines are low and it increases 5 mV for consecutively larger binary numbers. The digital information which sets the output level of the attenuator comes onto the board as a serial bit stream through the front end interface circuit as described for that block later in this section. The output of U251 is a current signal which is converted to a voltage signal by U250.

Summer/driver

U400 is an operational amplifier used to sum together the source signal and the user-selected dc offset coming from U301. U401 is the current driver for U400 and final amplifier for the analog source. K201 is used for protection of the source circuits from outside signals and for disconnecting the source from the front panel during the time that it is used for calibration. During calibration K201 opens and K202 or K200 is selected (closed) for calibration. The calibration signal is fed to the input boards via the mother board from pin 9 of the analog source board.

Front End Interface

Information for the dc offset, control data, and attenuator output level comes onto the board as serial data on pin 30 (CNTLD). The CNTCLK $\frac{1}{2}$ signal (pin 28) shifts the serial bit stream into the serial-to-parallel shift registers U501 and U502 and LDSRCL loads the data into latches U500 and U502. U500 holds dc offset information for the DAC U301. U502 holds information on the attenuation of the source signal and control information for: 1) selection of signal types (controls U452), 2) operation of the relays on the board, and 3) disconnecting the dc offset DAC output from U150 when a zero dc offset is selected.

dc Offset DAC

U301 receives offset information in digital format from U500 and converts it to an analog current signal. The current signal is changed to a voltage signal by U300. The output of U300 is connected to the switch U151. This signal is opposite in polarity and half the final amplitude of the dc offset. The switch is required because the DAC output signal is not exactly zero when zero offset is selected.

Offset Switch

The offset switch, U151, either connects the dc offset signal to amplifier U150 or terminates the line by connecting it to ground through R153. Control of the switching operation comes from the digital source board through U502 as described for the front end interface. One and only one of the switches in U152 is closed at any given time.

The amplifier circuit around U150 has a gain of two, adjustable with R9, which sets the dc offset level. The gain between the output of U150 and the front panel output is 1.

Overload Protection

U600 is two comparators configured to sense voltage on the source output line and signal an overload condition (source output fault) when the signal appearing on the output exceeds 12 V_{pp}.

Calibrator Introduction

The calibrator is driven by either square wave signals (64 kHz or 4 kHz) or pseudo random noise. These signals are generated on the analog source board, selected according to the needs of the current instrument process, and relocked to assure synchronization.

Square Wave Source

The DAC load signal (DACLD) on pin 36 is used for a number of things in this part of the analog source. This 256 kHz square wave is divided by U450 (a dual 4-bit counter) which yields square waves whose frequencies are 64 kHz and a 4 kHz. Both signals are connected to the signal selection circuit.

Pseudo Random Source

DACLD clocks U455 (serial shift register with 8-bit parallel output) which drives a group of gates, the end result of which is a pseudo random bit stream which repeats itself every 256 clock cycles. This signal and its inverse is connected to the signal selection circuit.

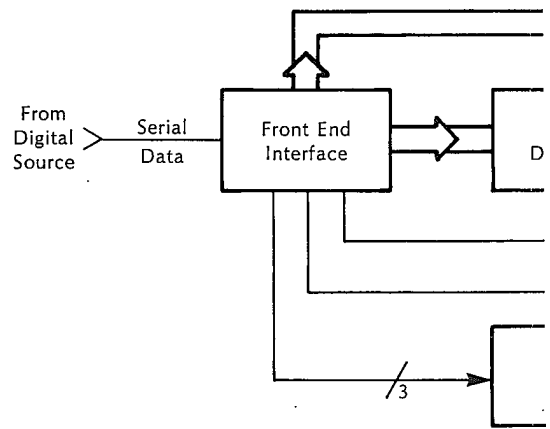
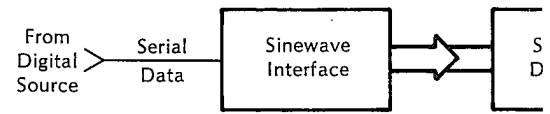
Signal Selection

Signal selection is done by U452 (a dual 1-of-4 selector/mux) and reclocking is done by U451. Inputs to this block consist of two square waves (64 kHz and 4 kHz) from U450 and the pseudo random noise (PRN) signal and its inverse. The control lines SELCAL and INVCAL from U502 select one of the four signals to pass to the calibrator circuit and to send to the trigger board as the signal CALTRIG. Pseudo random noise is not used for a CALTRIG signal, but a signal from the PRN source is connected to both C2 and C3 of the CALTRIG selector, U452A. See table A30-2 in section VIII for specific control information.

Calibrator

The 6.2 volt reference is divided by R5 and R6 such that 0.2 volts appears on the inverting input of U1. A feedback loop through Q1, Q2/Q3, and R7 forces the voltage across R8 to be the same as across R5. This makes Q1 a stable current source for Q2 and Q3. The bases of this transistor pair are driven by the TTL signal from the signal selection block such that one of the pair is on and the other is off at any given time. When Q3 is off there is no voltage drop across R16 and R10; when Q3 is on there is a voltage drop. Since the current through Q2 and Q3 is very well regulated, the voltage appearing on its collector is very stable.





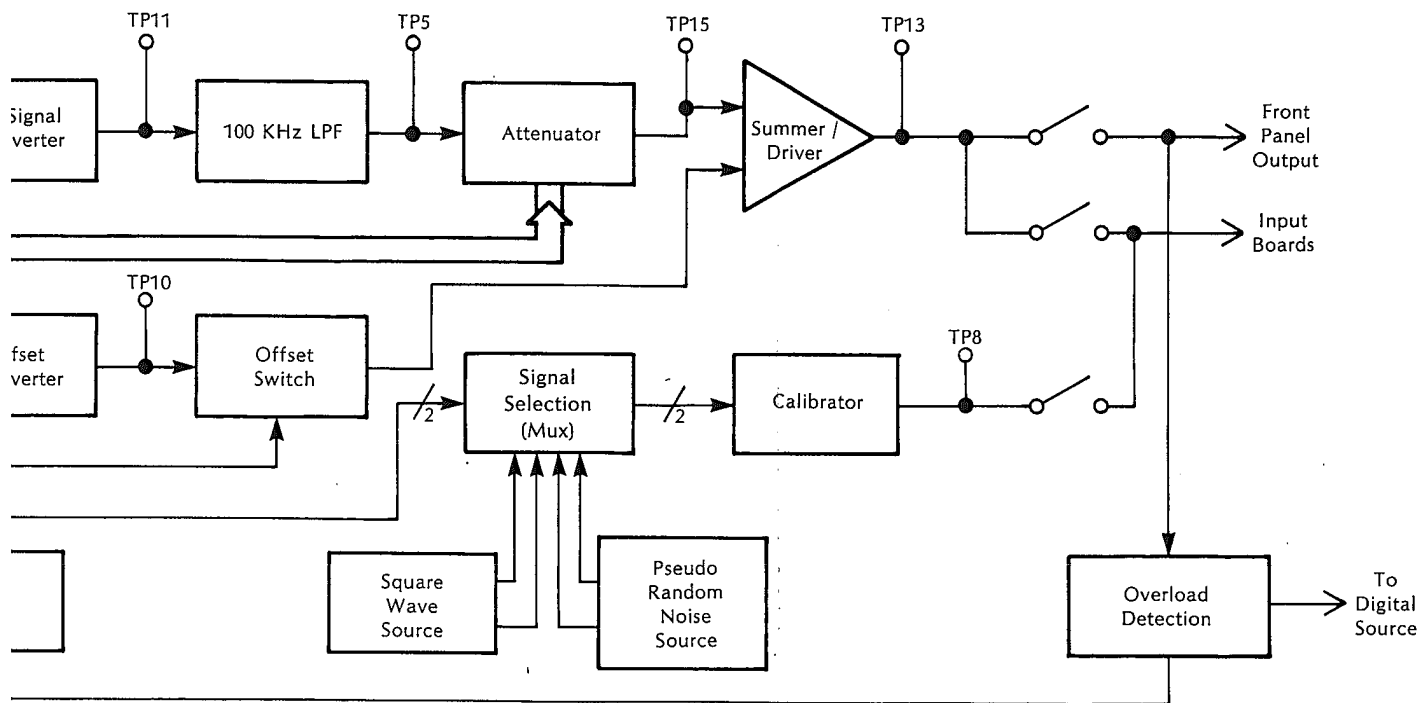


Figure 6-A30 Analog Source Block Diagram

6-14 A31 TRIGGER

The trigger assembly produces the trigger signal (TRIGRO) for the A1 Digital Source and the A5 Digital Filter and the sample signal (CONV) that is sent to the A32, A34 ADCs. The trigger assembly also generates the 10.24 MHz clock used by the A1 Digital Source, the A4 Local oscillator, the A5 Digital Filter, the A6 Digital Filter Controller, the A30 Analog Source, and the A32, A34 ADCs assemblies. The 10.14 MHz clock can be locked to an external reference signal by using the rear panel REF IN input.

Trigger Level Circuit

(Refer to figure 6-A31a) To produce the trigger level, the trigger assembly uses one of four analog inputs; external trigger (EXT TRIGGER), channel 1 (TRIG1@), channel 2 (TRIG2@), or trigger calibration (CALTRIG). The trigger select switch selects one of the input signals and passes it to a comparator. The selected analog input is compared to a dc voltage from the trigger's DAC. The output of the comparator is low as long as the analog signal is below this dc value and is high if the analog signal is above the dc value. The output of the comparator is then sent through an exclusive OR gate which inverts the signal if the slope select line is high.

Trigger Control

The operations of the trigger assembly are controlled through the trigger's shift register. The shift register shifts in a command word from the A1 Digital Source assembly. The command word sets the input trigger selection, the trigger level, the trigger slope, and whether an internal or external sample is used (SELXS).

EXT TRIGGER >
TRIG 1 @ >
TRIG 2 @ >
CALTRIG >

CNTLD > COMA
CNTCLK > WC
LDTRGL >
RESETL >

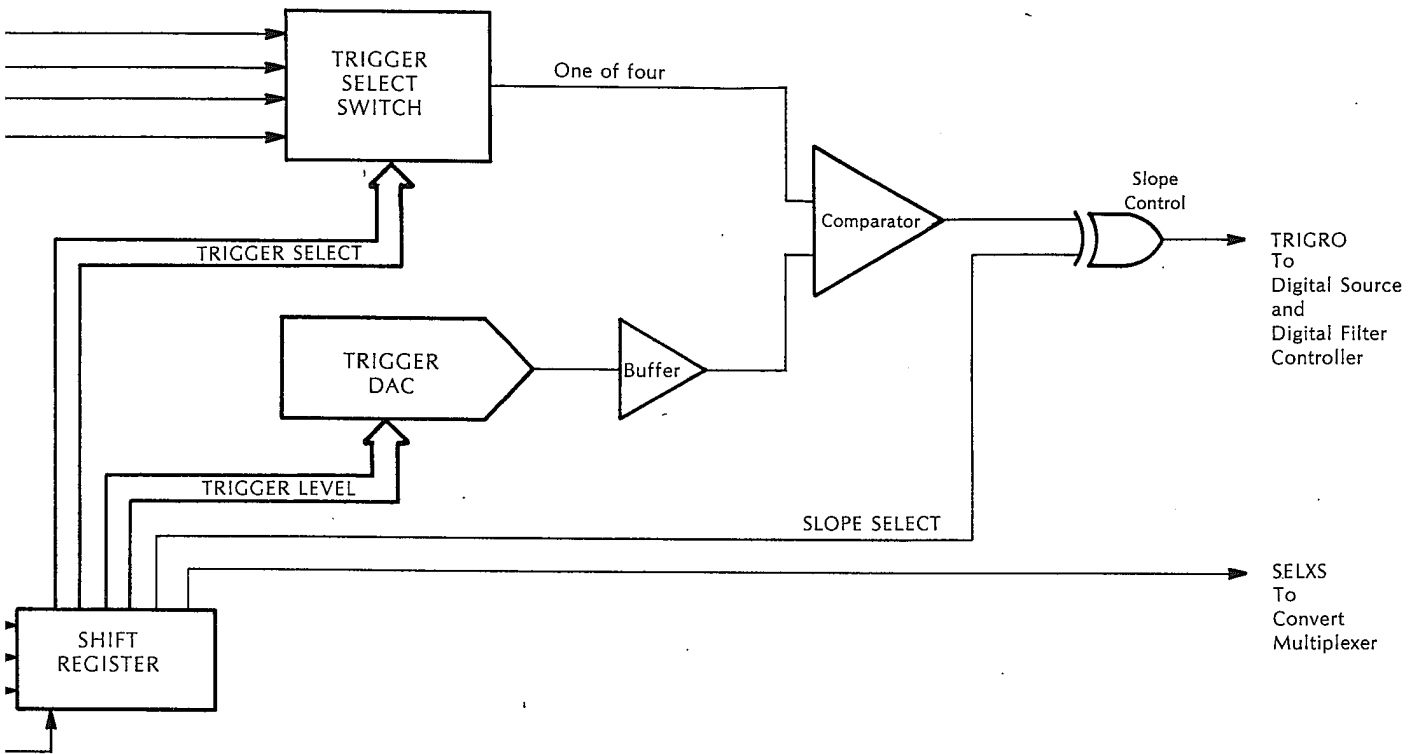


Figure 6-A31a Trigger Level Block Diagram

Trigger Clock Circuit

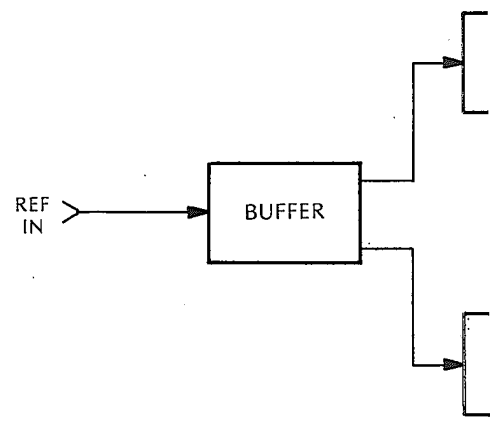
(Refer to figure 6-A31b) The trigger clock circuit produces the 10.24 MHz clock using a voltage controlled crystal oscillator (VCXO). When there is no external reference signal (REF IN) the phase lock loop is not used. The error voltage into the PLL gain and shaping subblock is zero. The frequency adjustment is used to adjust the frequency out of the VCXO to precisely 20.48 MHz. This signal is divided by two to form the 10.24 MHz clock. The 10.24 MHz signal is divided by forty to produce the internal sample signal (CONV, 256 kHz). The convert multiplexer selects the internal sample signal or an external sample signal. The signal SELXS from the shift register determines which is selected.

The phase lock loop is used when there is an external reference signal. The external reference signal can be 1,2,5, or 10 MHz. The difference in frequency between the 3.413 MHz harmonic of the external reference and the 3.413 MHz output of the VCXO are used for the phase comparison. The sampler subblock samples the 3.413 MHz clock from the VCXO with $\text{REF IN} \div 3$ to produce the sum and difference frequencies of the clock and the reference signal's harmonics. These frequencies are then put through a bandpass filter to produce an 80 kHz signal.

At the same time the 80 kHz signal is being produced, the REF IN is divided by 125. The phase detector samples the 80 kHz signal with the $\text{REF IN} \div 125$ signal to produce an error voltage. The error voltage is amplified and passed through a switchable low pass filter to generate the control signal for the VCXO. When the phase lock loop is in lock this control voltage is a dc value. If the phase lock loop is not locked, the control voltage deviates high and low until the phase lock loop locks.

Switchable Low Pass Filter (Q201, R214, C207, C208)

During normal operation the low pass filter has a very narrow bandwidth ($\cong 16$ Hz). This bandwidth can change to a wide bandwidth ($\cong 4$ kHz) to allow for a faster phase loop lock up. When the phase loop is in lock the output of the lock detect subblock is a negative dc voltage and a FET switch (Q201) in the PLL gain and shaping subblock is turned off. If the phase loop is not in lock the output of the lock detect subblock goes positive turning the FET switch on. This switches out the low pass filter and the UNLOCK signal is sent out to indicate the phase lock is unlocked. When the output of the lock detect returns to a steady positive dc voltage, the FET switch turns off and the low pass filter changes to a narrow bandwidth.



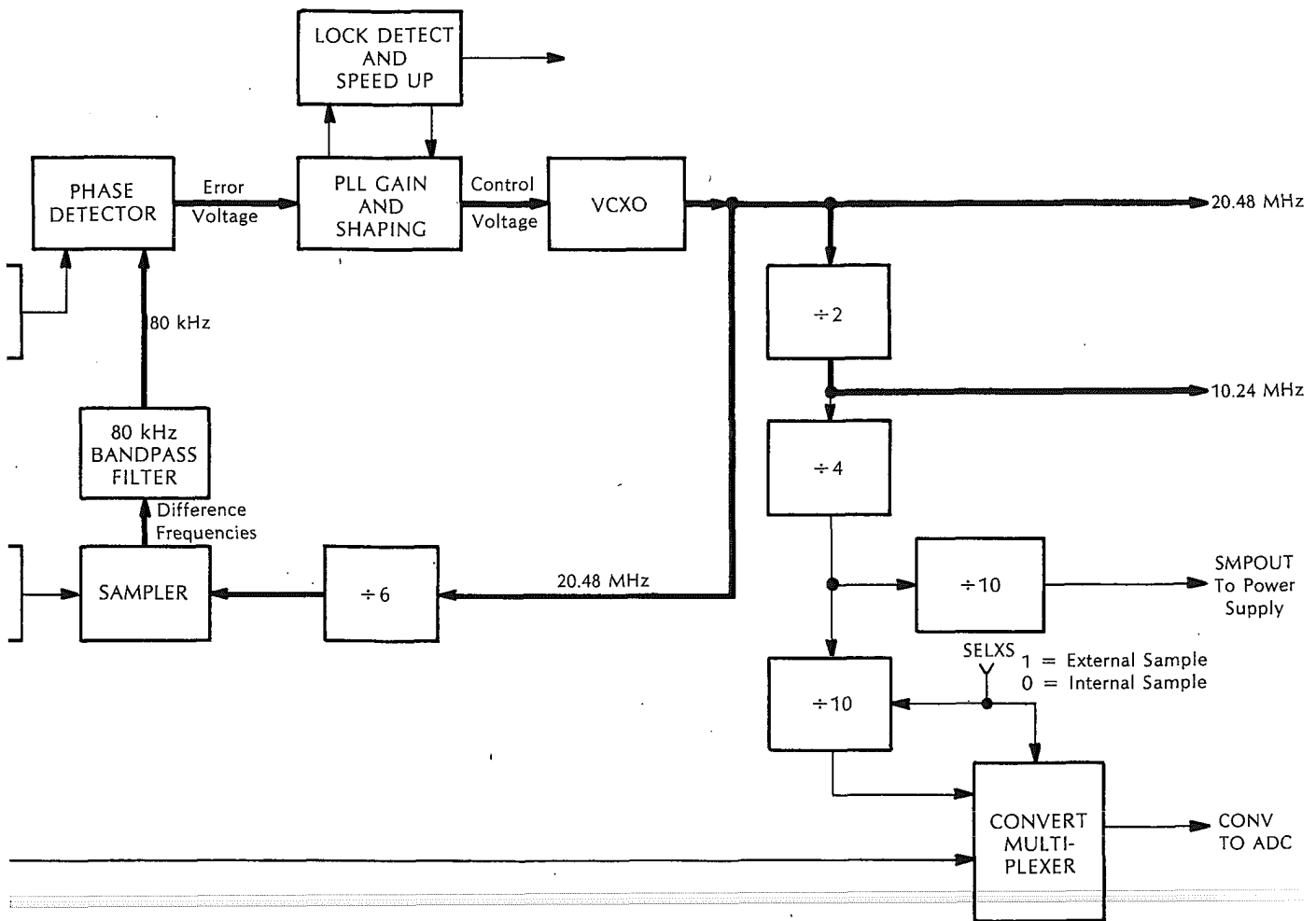


Figure 6-A31b Trigger Clock Block Diagram

6-15 A32, A34 ANALOG-to-DIGITAL CONVERTERS

(Refer to ADC Board Block Diagram on figure 6-A32) The ADC board converts analog data from the input board into 13-bit serial data words. The main parts of the ADC are two variable attenuators and their accompanying amplifiers, an anti-alias filter, a track and hold circuit, an 8-bit A/D converter (to avoid confusion, the board is referred to as "ADC" and the part is called "A/D converter"), a D/A converter (DAC), and a controller. Other circuits on the board include first and second pass circuits and the process switch, a dc offset D/A converter, an over range/half range circuit, a missed sample circuit, a diagnostic tester, and slave/master selection circuits.

The circuits in the data path may be divided into analog and digital. The signal is analog until it passes through the A/D converter. This discussion is divided into analog and digital sections.

Analog

The signal from the input board enters the ADC board through J200 and a balun and goes to attenuator #2 (#1 is on the input board). This attenuator is variable in 2 dB steps from 0 dB to 12 dB. It can also ground the input of the next amplifier (for calibration purposes). The configuration information for this attenuator and attenuator #3 come from serial-to-parallel (S/P) shift register U203. This information comes on the board from the input board and is shifted through U603, U203, and U202. The companion input board must be installed for the ADC board to receive configuration information.

The signal from attenuator #2 goes to amplifier #3. This amplifier is a non-inverting op amp circuit with a gain of 3. The signal from this amplifier goes to attenuator #3. This attenuator is identical to attenuator #2 except that instead of selecting a grounded input for the following amplifier it has another step of attenuation, giving it a range of 0 dB to 14 dB in 2 dB steps.

The purpose of all the amplifiers and variable attenuators up to this point is to assure that the strength of the signal to the anti-alias filter does not over drive it. Refer to table 6-A32a for information concerning attenuator configuration for a given range selection.

Table 6-A32a Attenuator configuration vs. range selection

| Range (dBV) | Input Atten (dB) | Atten #1 (dB) | Atten #2 (dB) | Atten #3 (dB) | Total Atten (dB) |
|-------------|------------------|---------------|---------------|---------------|------------------|
| -51 | 0 | 0 | 0 | 0 | 0 |
| -50 | 0 | 1 | 0 | 0 | 1 |
| -49 | 0 | 0 | 0 | 2 | 2 |
| -48 | 0 | 1 | 0 | 2 | 3 |
| -47 | 0 | 0 | 0 | 4 | 4 |
| -46 | 0 | 1 | 0 | 4 | 5 |
| -45 | 0 | 0 | 0 | 6 | 6 |
| -44 | 0 | 1 | 0 | 6 | 7 |
| -43 | 0 | 0 | 0 | 8 | 8 |
| -42 | 0 | 1 | 0 | 8 | 9 |
| -41 | 0 | 0 | 0 | 10 | 10 |
| -40 | 0 | 1 | 0 | 10 | 11 |
| -39 | 0 | 0 | 0 | 12 | 12 |
| -38 | 0 | 1 | 0 | 12 | 13 |
| -37 | 0 | 0 | 0 | 14 | 14 |
| -36 | 0 | 1 | 0 | 14 | 15 |
| -35 | 0 | 0 | 2 | 14 | 16 |
| -34 | 0 | 1 | 2 | 14 | 17 |
| -33 | 0 | 0 | 4 | 14 | 18 |
| -32 | 0 | 1 | 4 | 14 | 19 |
| -31 | 0 | 0 | 6 | 14 | 20 |
| -30 | 0 | 1 | 6 | 14 | 21 |
| -29 | 0 | 0 | 8 | 14 | 22 |
| -28 | 0 | 1 | 8 | 14 | 23 |
| -27 | 0 | 0 | 10 | 14 | 24 |
| -26 | 0 | 1 | 10 | 14 | 25 |
| -25 | 0 | 0 | 12 | 14 | 26 |
| -24 | 0 | 1 | 12 | 14 | 27 |
| -23 | 0 | 12 | 2 | 14 | 28 |
| -22 | 0 | 13 | 2 | 14 | 29 |
| -21 | 0 | 12 | 4 | 14 | 30 |
| -20 | 0 | 13 | 4 | 14 | 31 |
| -19 | 0 | 12 | 6 | 14 | 32 |
| -18 | 0 | 13 | 6 | 14 | 33 |
| -17 | 0 | 12 | 8 | 14 | 34 |
| -16 | 0 | 13 | 8 | 14 | 35 |
| -15 | 0 | 12 | 10 | 14 | 36 |
| -14 | 0 | 13 | 10 | 14 | 37 |
| -13 | 0 | 12 | 12 | 14 | 38 |
| -12 | 20 | 1 | 4 | 14 | 39 |

Table 6-A32a Attenuator configuration vs. range selection cont.

| Range (dBV) | Input Atten (dB) | Atten #1 (dB) | Atten #2 (dB) | Atten #3 (dB) | Total Atten (dB) |
|-------------|------------------|---------------|---------------|---------------|------------------|
| -11 | 20 | 0 | 6 | 14 | 40 |
| -10 | 20 | 1 | 6 | 14 | 41 |
| -9 | 20 | 0 | 8 | 14 | 42 |
| -8 | 20 | 1 | 8 | 14 | 43 |
| -7 | 20 | 0 | 10 | 14 | 44 |
| -6 | 20 | 1 | 10 | 14 | 45 |
| -5 | 20 | 0 | 12 | 14 | 46 |
| -4 | 20 | 1 | 12 | 14 | 47 |
| -3 | 20 | 12 | 2 | 14 | 48 |
| -2 | 20 | 13 | 2 | 14 | 49 |
| -1 | 20 | 12 | 4 | 14 | 50 |
| 0 | 20 | 13 | 4 | 14 | 51 |
| +1 | 20 | 12 | 6 | 14 | 52 |
| +2 | 20 | 13 | 6 | 14 | 53 |
| +3 | 20 | 12 | 8 | 14 | 54 |
| +4 | 20 | 13 | 8 | 14 | 55 |
| +5 | 20 | 12 | 10 | 14 | 56 |
| +6 | 20 | 13 | 10 | 14 | 57 |
| +7 | 20 | 12 | 12 | 14 | 58 |
| +8 | 40 | 1 | 4 | 14 | 59 |
| +9 | 40 | 0 | 6 | 14 | 60 |
| +10 | 40 | 1 | 6 | 14 | 61 |
| +11 | 40 | 0 | 8 | 14 | 62 |
| +12 | 40 | 1 | 8 | 14 | 63 |
| +13 | 40 | 0 | 10 | 14 | 64 |
| +14 | 40 | 1 | 10 | 14 | 67 |
| +15 | 40 | 0 | 12 | 14 | 68 |
| +16 | 40 | 1 | 12 | 14 | 69 |
| +17 | 40 | 12 | 2 | 14 | 68 |
| +18 | 40 | 13 | 2 | 14 | 69 |
| +19 | 40 | 12 | 4 | 14 | 70 |
| +20 | 40 | 13 | 4 | 14 | 71 |
| +21 | 40 | 12 | 6 | 14 | 72 |
| +22 | 40 | 13 | 6 | 14 | 73 |
| +23 | 40 | 12 | 8 | 14 | 74 |
| +24 | 40 | 13 | 8 | 14 | 75 |
| +25 | 40 | 12 | 10 | 14 | 76 |
| +26 | 40 | 13 | 10 | 14 | 77 |
| +27 | 40 | 12 | 12 | 14 | 78 |

The anti-alias filter is a passive low pass filter whose break frequency is 100 kHz. Following this filter are two non-inverting op amps, each with a gain of 3, which feed the track and hold circuit.

The track and hold circuit is controlled by the CONV signal from the trigger board and the TRH (track & hold) signal from the ADC controller. The CONV signal initiates the "hold" and the controller terminates it. The purpose of the track and hold circuit is to hold the voltage of the input signal for the period of time required for the value to be digitized. When tracking, the circuit acts like an inverting amplifier. See figure 6-A32a.

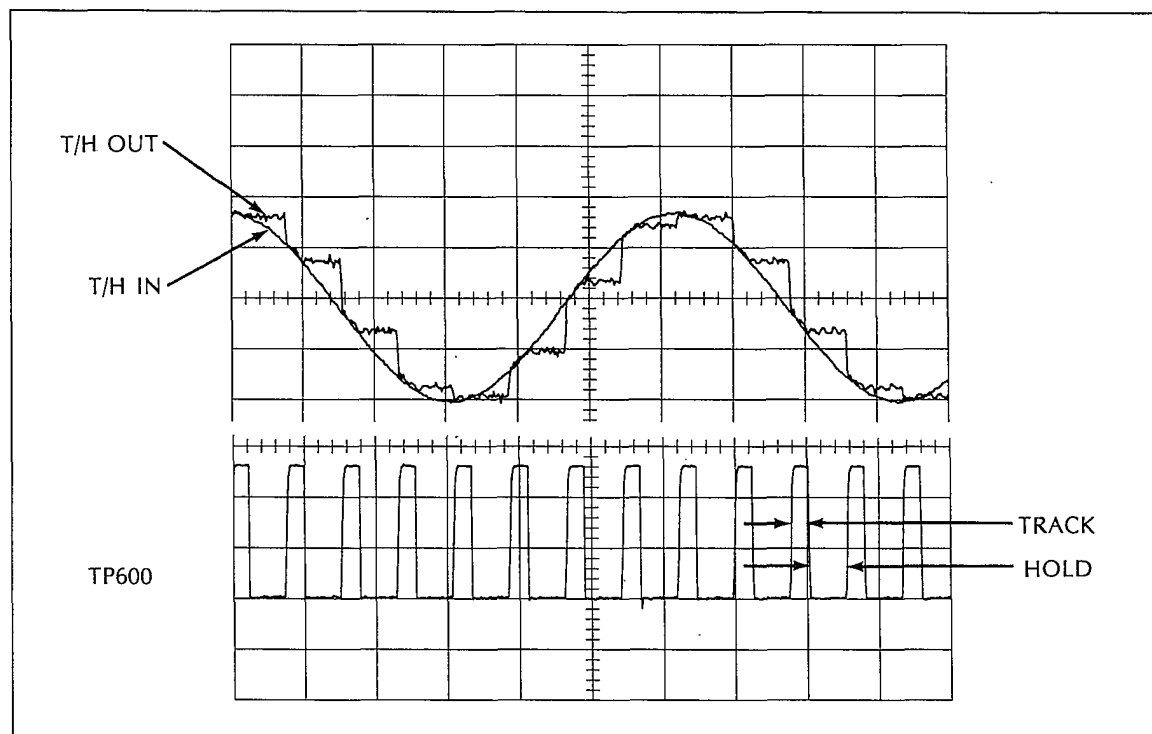


Figure 6-A32a Track & hold Input vs. output

Digital

The conversion process starts when the controller receives a start conversion signal (CONV) from the trigger board. The ADC board in channel two generates the control signals which coordinates the two passes and controls the process switches on both boards. The T/H OUT signal is converted to a 13-bit digital word by passing the signal through an 8-bit A/D converter twice as described in the following discussion.

The first pass circuit takes the track and hold output, divides it by four, and level shifts it for the A/D converter. The controller then sets the process switch (U405) to send this signal to the A/D converter (see table 6-A32b for process switch configuration information). When the conversion is complete, the 8-bit word goes to the controller which combines the word with dither (a noise signal generated inside the controller chip) and outputs a 13-bit word to the DAC.

The DAC converts the first pass word back to a voltage which goes to the second pass circuit (U406). This circuit compares the converted signal to the original input signal and produces a difference voltage. The controller sets the the process switch to send this difference voltage to the A/D converter where it is converted. When the conversion is complete, the controller inputs the result, scales it down and adds it to the first pass word to obtain a 13-bit data word. The controller sends the converted data to the digital filter in a serial format after the digital filter sends a request for the data (DREQ).

Between each of the passes, the controller sets the process switch to send a .34 volt dc signal to the A/D converter to reset it. This "third pass" shows in figure 6-A32b as the high portion of the signal. The first pass appears as the signal following a roughly sinusoidal pattern and the second pass appears as a noisy signal centered within the first pass sine wave.

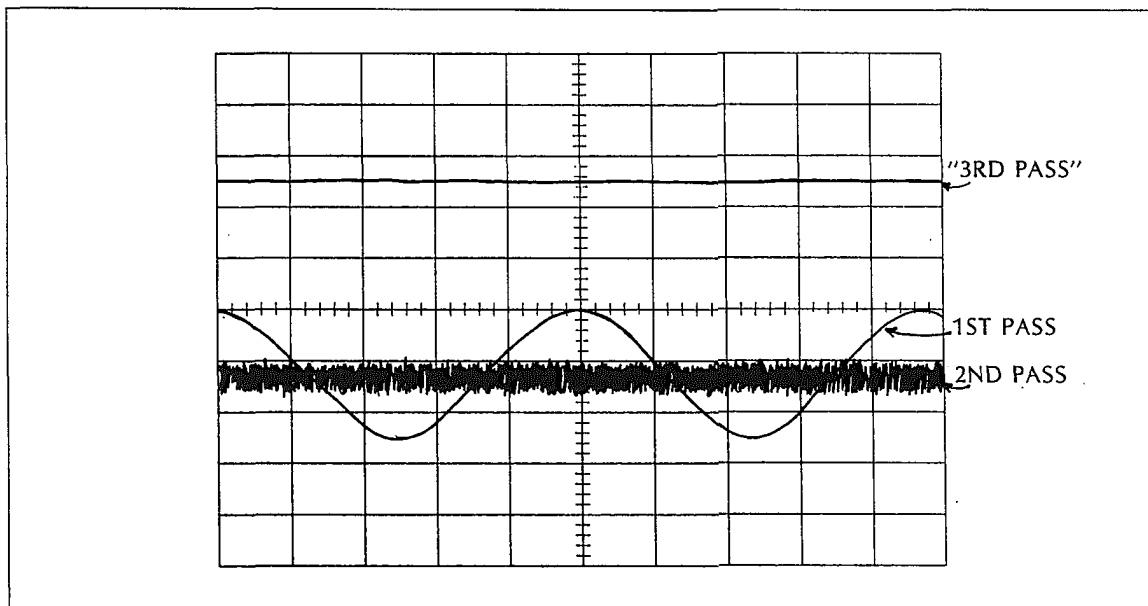


Figure 6-A32b Process switch output; TP405

Table 6-A32b Process switch configuration information

| Input Selected | GSW | CLADC |
|---------------------|-----|-------|
| First Pass Circuit | 1 | X |
| .34 Vdc Reference | 0 | 1 |
| Second Pass Circuit | 0 | 0 |

6.2 V reference voltage

The ADC board uses the 6.2 voltage reference generated by the DAC. This reduces the error due to temperature variations. The voltage reference is used by the A/D converter, the track and hold circuit, and the over range/half range circuit. Since the A/D converter's gain is controlled by this reference, the adjustment for the voltage reference is also the A/D converter's gain adjustment.

Offset D/A Converter

U201 is a D/A converter connected to the data path at the output of amp 4 (U101) to correct the accumulated dc offset of the amplifiers. This process occurs during auto zeroing. The offset control information comes onto the board as serial data through U603, U203 and U202. U202 converts the offset DAC information to parallel format and latches it.

Over Range/Half Range Circuit

This circuit compares the signal at the output of U501 (which is the signal from the data path at TP100, amplified X4) to a fixed voltage reference to generate the overload (OVLD) and half range (HLFSCALE) signals. This is done with comparators U500 and U502. (Note that the signal from U501 also leaves the board as the trigger signal TRIG@). The comparators of U500 are configured to trigger on the positive portions of the signal as U502 triggers on the negative. The outputs of both are wire OR'd together. The COVLD signal from the input board is OR'd with the overload signal from the ADC board so that either could activate the OVLD signal.

Missed Sample Circuit

If an external sample signal is used which is too fast, the MSMP signal is sent to the digital filter controller. The missed sample circuit digitally determines if the track and hold is holding a signal at the time a CONV signal is received.

Diagnostic Tester

The ADC controller (U602) is a custom built state machine. Problems with this part may be diagnosed by using self tests which are activated by front panel key presses. Configuration commands and test signals are sent to the ADC board as serial data through the serial/parallel shift register U603, so the self tests also check the CNTLDAD (control data) path.

Master/Slave Selection

There is an ADC board in each analyzer input channel. These are identical boards. The digitizing process must occur simultaneously on both boards, so one controller must control both boards. ~~When both boards are installed, the board in channel two acts as the controller of both boards. Each board contains a controller but only one controller is active. It sends the end of conversion (EOC) and the process switch (GSW) signals to the other controller so it can synchronize its operations with the controlling board. If no ADC board is installed in channel two, the controller on the board in channel 1 controls its own A/D conversion.~~

The slots on the mother board for the ADC boards are wired so that the controller on the board in channel two controls the A/D conversion process on both boards. The master/slave circuit on each board consists of an inverter (U503d) with a pull up resistor on the input. The mother board connects the output of this circuit of the board in the channel two slot to the input of the same circuit on the board in the channel one slot (they both control buffers U604 and U505 on their respective boards, too). When boards are installed in both slots, the board in slot two has a low level on the master/slave line which feeds the input of the inverter on the board in slot one, resulting in its master/slave line being high. When the channel two ADC board slot is empty the ADC board in channel one automatically becomes the "master"; it takes control of its own conversion process.

Internal Signal Descriptions

| | |
|---------------------------------|--|
| + 6.2R | ±-6.2 REFERENCE |
| - 6.2R | This is the analog digital converter's tracking voltage reference generated by the conversion DAC. It provides the voltage reference for the A/D converter, converter IC, the track and hold circuit, and the over range/half range circuit. |
| CLADC | CLEAR ADC Signal from the controlling ADC controller to the process switch on each board. It works with GSW to determine the input to each of the A/D converter ICs. |
| CONTOUT CONTIN | CONTROL OUT Control out is part of the connection between the A32 analog digital converter board and A34 analog digital converter board. This signal determines which board is in control. If both boards are installed, A32 is in control. |
| EOC | END OF CONVERSION When both analog digital converter boards are installed, A32's controller tells A34's controller it is done with a conversion. |
| GSW | PROCESS SWITCH SIGNAL Signal from the controlling ADC controller to the process switch on each board. It works with CLADC to determine the input to the A/D converter ICs. When both boards are installed, the GSW is also used as an input for timing to the A34 analog digital converter's controller. |
| LCNV | LOCAL A/D CONVERT The ADC controller's command to the A/D converter IC to start conversion. When both boards are installed, the LCNV signal goes to the A34 analog to digital converter's A/D converter IC. |
| TRH | TRACK AND HOLD Signal from the controlling ADC controller to the track and hold switch on each board. This signal determines when the track and hold switches are open and closed. |

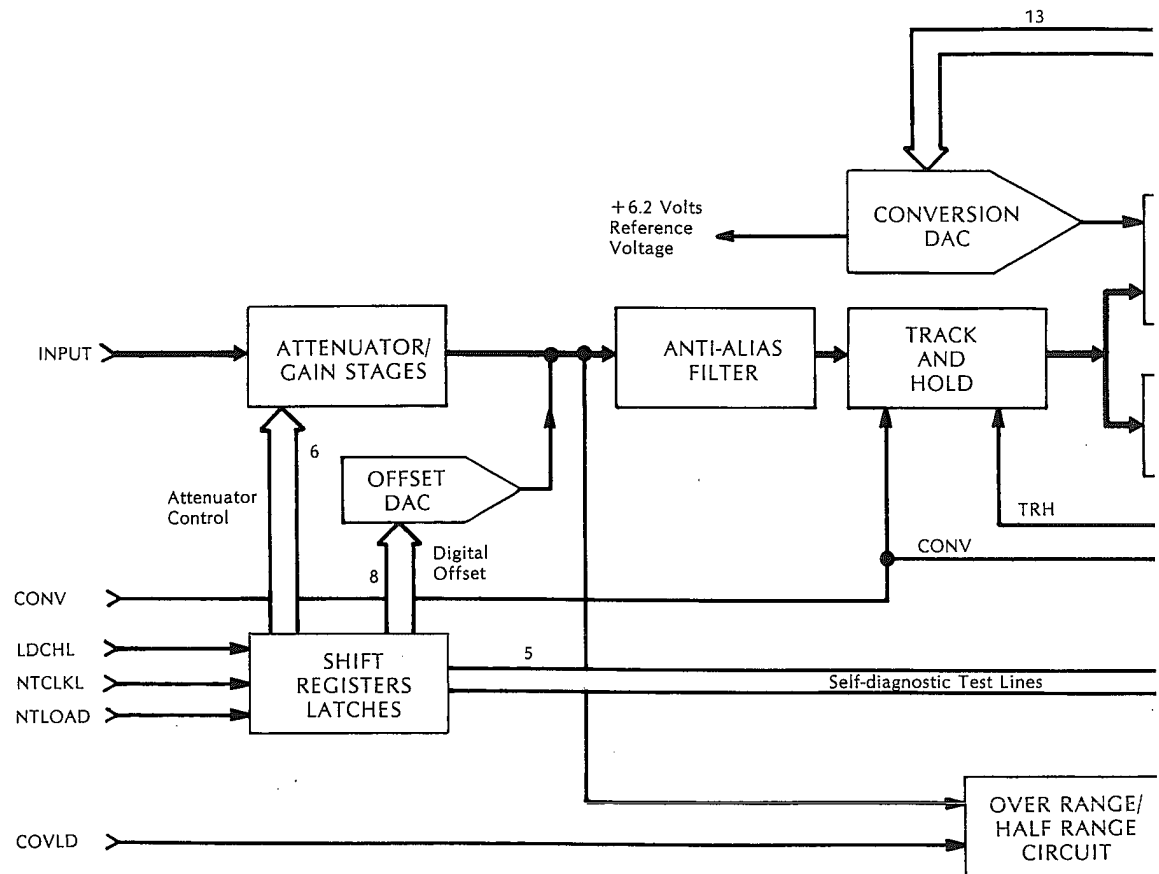
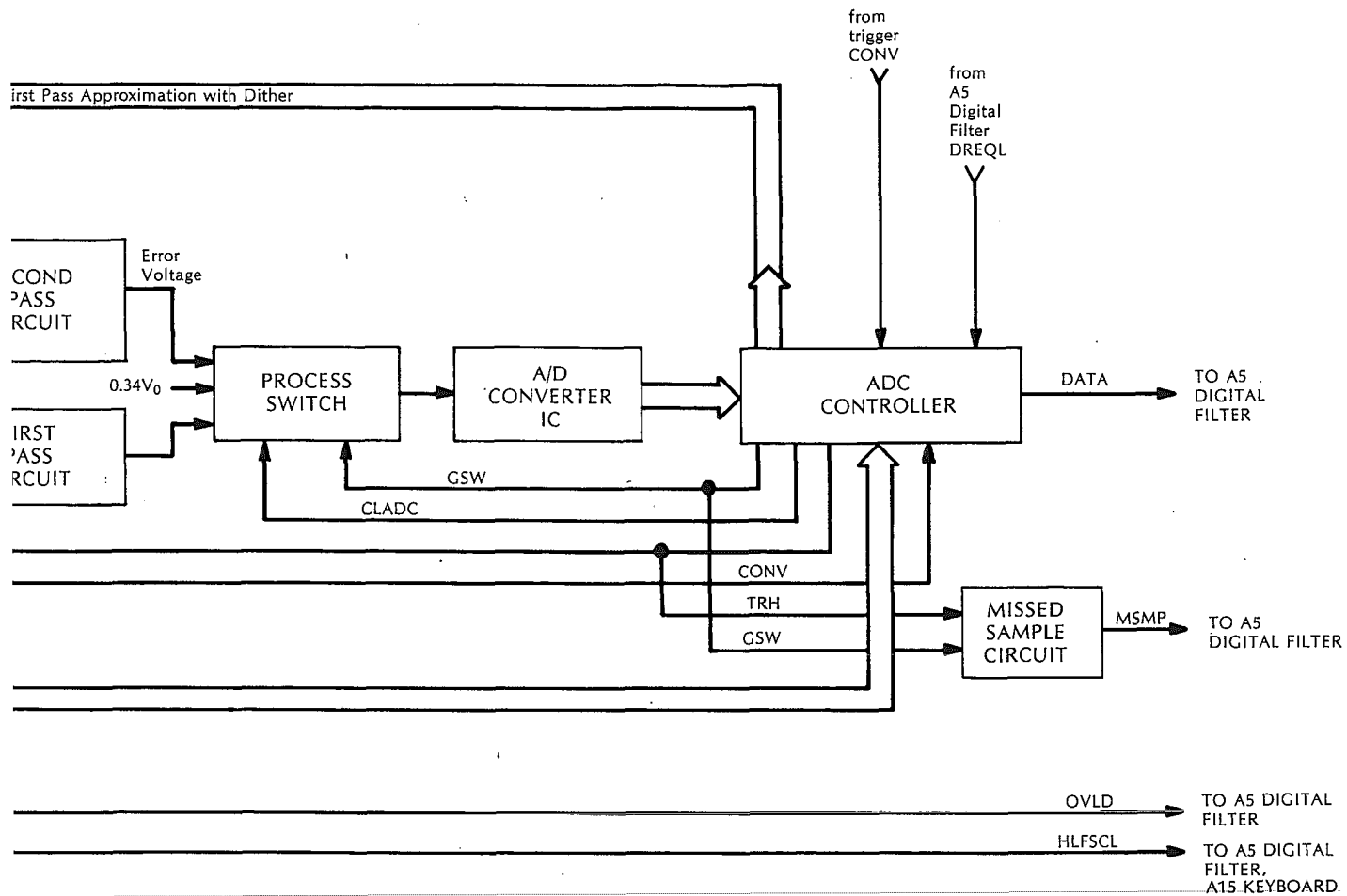


Figure 6-A32



Analog Digital Converter Block Diagram

6-16 A33, A35 INPUT

The input assembly (along with the ADC) implements the voltage ranges and conditions the input signals. The input overload detect circuit warns the operator that the reference voltage is excessively high. The common mode rejection DAC compensates for differences between the HIGH input and the LOW input circuits.

The block diagram of the input assembly is shown in figure 6-A33. The HP 3562A has two channels of balanced differential inputs; the A33 Input assembly is identical to the A35 Input assembly. Each assembly has a HIGH input and a LOW input. The HIGH input is the channel's BNC center conductor and the LOW input is the channel's BNC shell conductor. The HIGH and LOW input signals are attenuated by a ladder attenuators. The input attenuators use resistors for low frequency attenuation and adjustable capacitors for high frequency flatness response. An internal analog signal (STIM@) from the A30 Analog Source assembly is put into the HIGH signal path. The instrument uses this signal for self-tests and calibration.

After the signal is attenuated, it goes into a buffer. The buffer's power supplies are bootstrapped to allow for a 20V common mode signal. After the HIGH input and LOW input signals are attenuated and buffered, they are subtracted using a difference amplifier. The output of the difference amplifier is sent to a times three amplifier which is adjustable for gain and dc offset.

After the difference amplifier, three attenuator/gain stages provide the 2 dB intermediate gain and attenuation steps. One of the stages is on the input assembly and the other two stages are on the ADC assembly. Each stage contains a multiplexer and a times three amplifier.

The input assembly is controlled by two serial-in parallel-out shift registers and relay drive circuits. The serial control data word (CNTLD) from the A1 Digital Source is shifted into the registers and then the output is latched by the load channel signal (LDCHL). This control word determines which of the relays are set, the settings for the multiplexers in the attenuator/gain stages, the common mode rejection DAC output value, and the dc offset value (circuit on the ADC assembly). The input sends the ADC its control data word (CNTLD AD) from the interface shift registers.

Table 6-A33 Control Word

| IC Pin No. | Description | Function | |
|------------|------------------------|--|--|
| | | If bit = "1" | If bit = "0" |
| 7 | ac/dc Coupling | dc | ac |
| 8 | Input Enable | Disconnected | Connected if Source Enable is low |
| 9 | Internal Source Enable | Disables inputs and connects internal source | Inputs can be connected |
| 10 | Ground Low | Return signal shorted to chassis ground | |
| 11 | Attenuation | 0 dB | Note Only one should be selected at a time. |
| 12 | Select | 20 dB | |
| 13 | | 40 dB | |

For attenuator settings refer to table 6-A32a.

Attenuators and Buffers

The input relay switches perform the following functions: isolate the input connectors when the internal source is connected, provide ac/dc coupling, and select 0 dB, 20 dB, or 40 dB input attenuation. The attenuated signal leads to a FET source-follower buffer and then a unity gain operational amplifier (U351) with the FET in its feedback loop. As a result, any offsets in the source follower are eliminated.

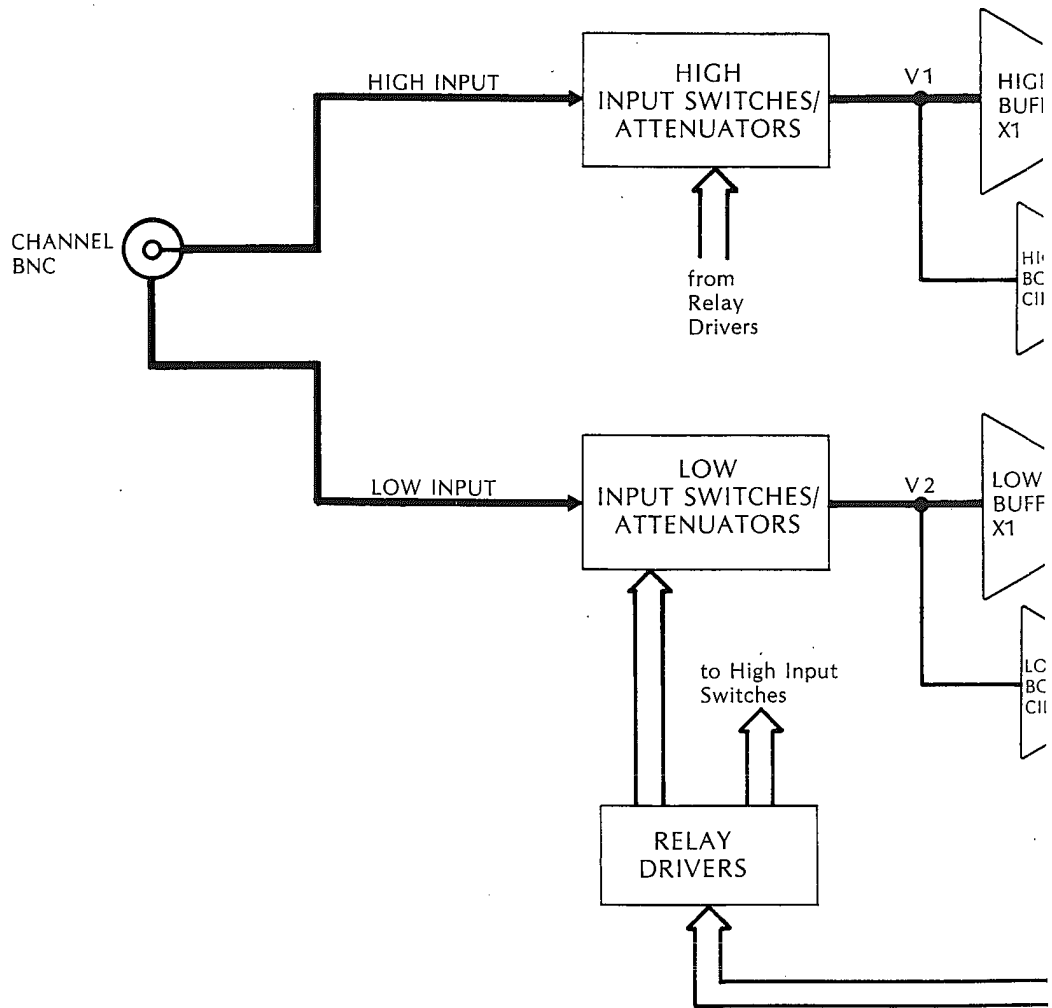
The bootstrapping of the power supplies consists of two current sources, one positive and one negative, with two emitter followers. The emitter follower provides the power to the buffer while the current source keeps the voltage across the zener at 5.6V above the input. This creates a stable power supply for the buffer so it has unity gain for a wide voltage range even at high frequencies. The 30V protection diodes are also bootstrapped to the power supply to avoid distortion. The LOW side of the input has the same configuration.

Input Overload Detector

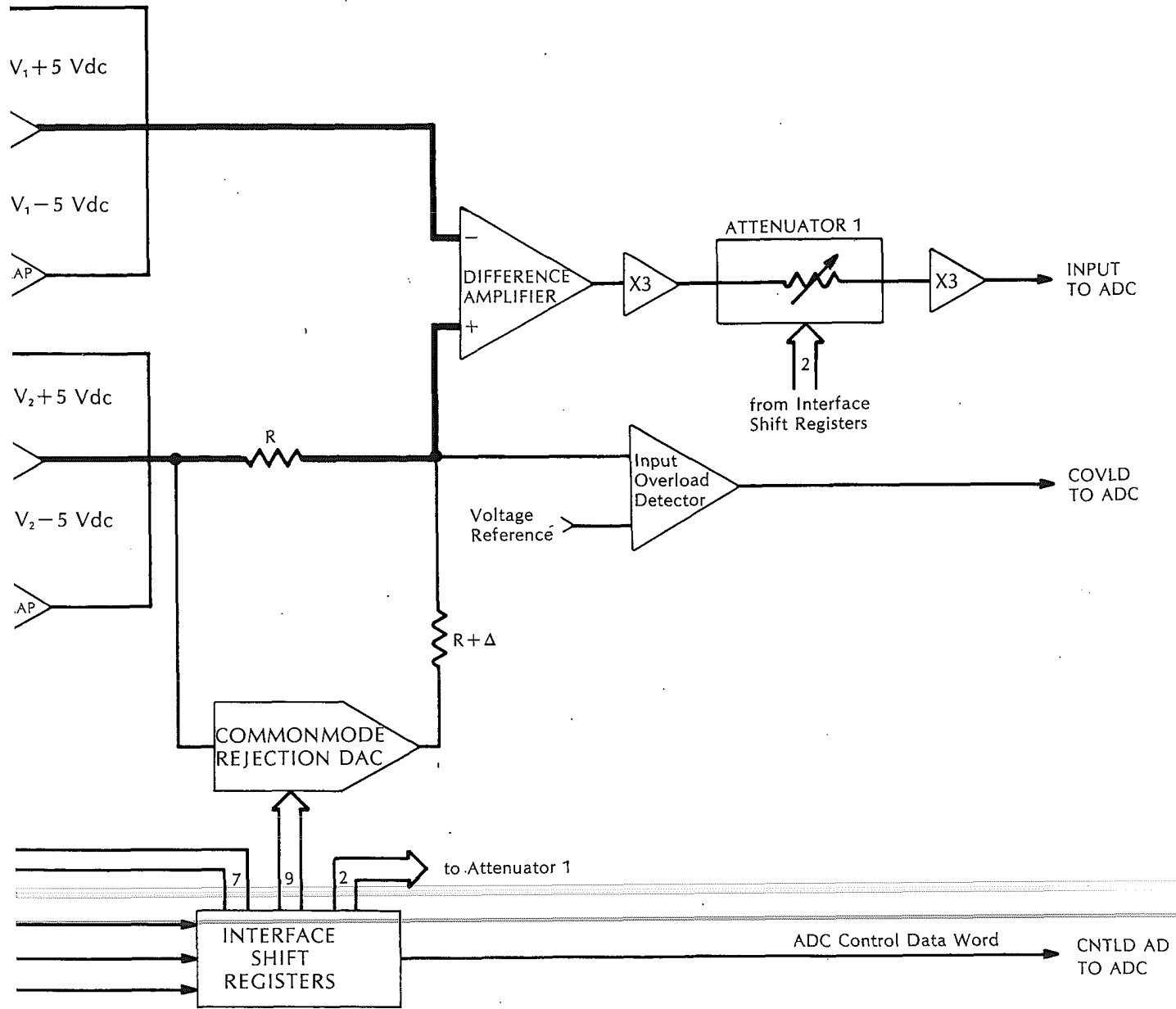
The input overload detector circuit receives its input from the HIGH signal path. It is active when the input signal to ground is over the limit of 20V with no attenuation. Resistors R503 and R502 attenuate the signal for the comparators (U501A, U501B). The attenuated signal is compared to a positive and negative reference voltage. If the value is greater than the reference level, the input overload signal (COVLD) is sent to the overload circuit on the ADC assembly.

Common Mode Rejection DAC

The common mode rejection DAC is a discrete DAC composed of operational amplifiers, FETs, and a resistor network. The DAC receives its digital input from the interface shift registers. The common mode rejection DAC's output is an effective resistance value which compensates for differences between the HIGH input and the LOW input circuits.



| | | | |
|---------|--------|---|-------------------|
| From | LDCH | > | Load Channel |
| A1 | CNTCLK | > | Control Clock |
| DIGITAL | CNTLO | > | Control Data Word |
| SOURCE | | | |



e 6-A33 Input Block Diagram

6-17 SIGNAL DESCRIPTIONS

This section describes the signal names between assemblies. All signals with a mnemonic ending in an L are active low.

± 15A ± 15 ANALOG VOLTS
 +15A A18 J1-3)
 -15A A18 J1-4)
 Voltage output from the A18 Power Supply that goes to the following assemblies:

| | |
|-----|----------------|
| A30 | Analog Source |
| A31 | Trigger |
| A32 | ADC (CHAN 1) |
| A34 | ADC (CHAN 2) |
| A33 | Input (CHAN 1) |
| A35 | Input (CHAN 2) |

± 15S ±15 VOLTS
 (+15S A18 J1-9)
 (-15S A18 J1-10)
 Voltage output from the A18 Power Supply that goes to the following assemblies:

| | |
|----|-----------------------|
| | HP 1345A Display |
| A1 | Digital Source |
| A5 | Digital Filter |
| A2 | System CPU (not used) |

+ 2.6V +2.6 VOLTS
 (A18 J1-6)
 Voltage output from the A18 Power Supply that goes to the termination networks on the A12 Mother Assembly.

± 30V ± 30 VOLTS
 (+30V A18 J1-1)
 (-30V A18 J1-2)
 Voltage output from the A18 Power Supply that goes to the following assemblies:

| | |
|-----|----------------|
| A33 | Input (CHAN 1) |
| A35 | Input (CHAN 2) |

+ 5FNTEND +5 VOLTS FRONTEND
 (A18 J1-5)
 This signal goes to the A32 ADC 1, A34 ADC 2, A33 Input 1, and A35 Input 2. It is the same signal as +5S which is the main five volt output from the A18 Power Supply.

+5S +5 VOLTS
 (A18 J1-5, A2 TP2)
 Main five volt output from the A18 Power Supply that goes to all the assemblies and the HP 1345A digital display.

+8S1 +8 VOLTS ONE
 (A18 J1-7)
 Voltage output from the A18 Power Supply that goes to the A5 Digital Filter.

+8S2 +8 VOLTS TWO
 (A18 J1-8)
 Voltage output from the A18 Power Supply that goes to the A5 Digital Filter.

±FAN ± FAN VOLTS
 Power supply to the fan. The fan supply is derived from the +8 V output and the -15 V output:
 $(+8) + (-15) = 23 \text{ Vdc}$

8MHz 8 MHz CLOCK
 (A2 TP5)
 Clock from the A2 System CPU to the following assemblies:

- A3 Program ROM
- A7 Floating Point Transform Processor
- A8 Global RAM/Display

10.24MHz 10.24 MHz CLOCK
 (A4 TP18)
 (A1 TP4)
 Clock from the A31 Trigger assembly to the following assemblies:

- A1 Digital Source
- A4 Local Oscillator
- ~~A5 Digital Filter~~
- A6 Digital Filter Controller
- A30 Analog Source
- A32 ADC 1
- A34 ADC 2

Serial data from the A32, A34 Analog Digital Converters and sine/cosine data from the A4 Local Oscillator to the A5 Digital Filter is synchronized to this clock. This signal is terminated by A12 R3 and A12 R4.

20.48MHz 20.48 MHz CLOCK
 (A31 TP10)
 Clock from the A31 Trigger assembly to the A32, A34 Analog Digital Converter assemblies.

A1L to A23L**SYSTEM ADDRESS BUS**

Active Low

These address lines from the A2 System CPU are part of the system bus. These addresses along with VIOL, ASL, UDSL, and LDSL are used to access various registers within the following assemblies:

| Lines | Assemblies |
|-----------|---------------------------------------|
| A1 to A2 | A15 Keyboard |
| A1 to A8 | A1 Digital Source |
| | A3 Program ROM |
| | A4 Local Oscillator |
| | A6 Digital Filter Controller |
| | A7 Floating Point Transform Processor |
| | A8 Global RAM |
| | A9 Fast Fourier Processor |
| A9 to A23 | A3 Program ROM |

ARML**ARM**

(A1 J705-1)

Active Low Low Signal from the A6 Digital Filter Controller to the A1 Digital Source to start a triggered measurement process. ARML stays asserted until the rising edge of BFST.

ASL**ADDRESS STROBE**

Active Low

This is the system address bus strobe from the A2 System CPU assembly. When the Address strobe signal is low, a valid address is on the system bus.

ATN**ATTENTION**

Signal to and from the A2 System CPU to the A22 HP-IB. This is the control line that places the HP-IB in the "Command Mode".

B2GDSL**HP 1345A GLOBAL DATA STROBE**

Active Low

This signal is from the A8 Global RAM to the A17 Display Interface.

It is similar to GDSL, except B2GDSL is only active during a global bus transfer to the display. When this signal goes from low to high, global data is put into the registers on the A17 Display Interface assembly.

BA1L to BA4L**BUFFERED ADDRESS LINES**

Active Low

These signals are the buffered version of the lower four system address lines of the A6 Digital Filter Controller. They are used by the A5 Digital Filter assembly for command decoding.

| | |
|--|--|
| BFST | <p>BUFFER START (A1 TP9)</p> <p>This signal from the A1 Digital Source goes to the A6 digital filter and the A4 Local Oscillator. When the instrument is in the triggered mode, BFST marks the first sample of the data block. After a trigger and sample clock are received by the digital source it sends the BFST signal to the digital filter controller telling it to start taking data. The local oscillator uses this signal to latch the phase of the sinusoidal output to the A5 Digital Filter.</p> |
| BLDSL | <p>BUFFERED LOWER DATA STROBE Active Low</p> <p>This signal is the buffered version of the LDS line of the A6 Digital Filter Controller. It is used by the A5 Digital Filter assembly for command decoding.</p> |
| BLK1FULLH BLK2FULLH BLK3FULLH | <p>BLOCK 1 FULL BLOCK 2 FULL BLOCK 3 FULL Active high</p> <p>These signals are from the A5 Digital Filter to the A6 Digital Filter Controller. When the imaginary filter auxiliary data block (BLK2FULL) or the unfiltered data block (BLK3FULL) is full, the positive going transition of these signals sets the corresponding interrupt flag flip-flop on the A6 Digital Filter Controller.</p> |
| BRESETL | <p>BUFFERED RESET Active Low</p> <p>This signal is from the A6 Digital Filter Controller to the A5 Digital Filter assembly. It is the buffered version of the system bus line RESETL.</p> |
| BUDSL | <p>BUFFERED UPPER DATA STROBE Active Low</p> <p>This signal is from the A6 Digital Filter Controller to the A5 Digital Filter assembly. It is the buffered version of the system bus line UDSL.</p> |
| BURSTEN | <p>BURST-ENABLE</p> <p>Signal from the A1 Digital Source to the A30 Analog Source that enables the A30 Analog Source when in burst mode.</p> |
| BWRITEL | <p>BUFFERED WRITE Active Low</p> <p>This signal is from the A6 Digital Filter Controller to the A5 Digital Filter assembly. It is the buffered version of the system bus line WRITEL. The A5 Digital Filter uses this signal for command decoding and register reading and writing.</p> |
| CALTRIG | <p>CAL TRIGGER</p> <p>Signal from the A30 Analog Source to the A32 trigger assembly. This signal is a pulse which is synchronous with the calibrator. It is used in the calibration to calculate phase.</p> |

| | |
|--------------------------------------|---|
| CH1BG1L CH2BG1L | <p>CHANNEL 1 BUS GRANT 1 CHANNEL 2 BUS GRANT 1 Active Low</p> <p>These signals are from the A5 Digital Filter assembly to the A6 Digital Filter Controller. They go low each time the A5 Digital Filter outputs a data sample to the A8 Global RAM. The A6 Digital Filter Controller primarily uses these signals to format the data block size.</p> |
| CH1BR1L CH2BR1L | <p>CHANNEL 1 BUS REQUEST 1 CHANNEL 2 BUS REQUEST 1 Active Low</p> <p>The A5 Digital Filter sends these signals to the A6 Digital Filter Controller. The A6 Digital Filter Controller uses CH1BR1L and CH2BR1L to determine when to start and stop outputting data to the A8 Global RAM. When the A5 Digital Filter is ready to output real filtered data, the corresponding signal (CH1BR1L or CH2BR1L) goes low. If the transfer is a real data transfer, CH1BR1L or CH2BR1L goes high when the A5 Digital Filter gets the grant signal (CH1BG1L or CH2BG1L) from the A6 Digital Filter Controller. If the transfer is a complex operation (zoom), CH1BR1L or CH2BR1L goes high after the second grant signal.</p> |
| CH1LOSELH CH2LOSELH | <p>CHANNEL 1 LOCAL OSCILLATOR SELECT BITS CHANNEL 2 LOCAL OSCILLATOR SELECT BITS Active High</p> <p>The A6 Digital Filter Controller outputs these signals from its command register to the A5 Digital Filter assembly. The A5 Digital Filter assembly uses them to select the input to the digital filters. The input can be either the sine/cosine data from the local oscillator or a locally generated constant.</p> |
| CH1STOP1 CH2STOP1 | <p>CHANNEL 1 STOP 1 CHANNEL 2 STOP 1 Active High</p> <p>These signals are from the A6 Digital Filter Controller to the A5 Digital Filter. <u>During measurements CH1STOP1 and CH2STOP1 are used to control the data output section of A5 Digital Filter. When the signals go high, the corresponding A5 Digital Filter output section is shut off. When these signals are low, the A5 Digital Filter is able to output filtered data.</u></p> |
| CHANNEL 1 CHANNEL 2 | <p>CHANNEL 1 CHANNEL 2 (A33, A35 J300)</p> <p>These are the input signals from the front panel to the A33 Input 1 and A35 Input 2 assemblies. The BNC center is the HIGH INPUT and the BNC shell is the LOW INPUT.</p> |
| CHASSIS | <p>CHASSIS</p> <p>This input from the front panel is connected to the frame of the instrument.</p> |

CLADC CLEAR A/D
(A32, A34 TP603)
This signal is used by the A32 ADC 1 and the A34 ADC 2. CLADC is from the ADC controller to the ADC process switch. This signal is used with GSW to determine the input to the A/D Converter IC. When both assemblies are installed, the CLADC signal goes to the A32 ADC 1 assembly's process switch.

CNTCLK CONTROL CLOCK
(A1 TP11)
Signal from the A1 Digital Source which clocks the command data word CNTLD into the following assemblies:

- A33, A34 Input
- A32, A34 Analog Digital Converter
- A31 Trigger
- A30 Analog Source

CNTLD CONTROL DATA WORD
(A1 TP10)
This is the serial command data word from the A1 Digital Source to the following assemblies:

- A33, A34 Input
- A31 Trigger
- A30 Analog Source

CNTL DAD1 CONTROL DATA WORD TO ADC 1
CNTL DAD2 CONTROL DATA WORD TO ADC 2
These are the serial command data words from the A33, A35 Input assemblies to the A32, A34 Analog Digital Converters. CNTL DAD1 and CNTL DAD2 are part of the data word CNTLD from the A1 Digital Source.

CONECTL CONNECT GROUND
A15 Keyboard ground to A12 Mother Assembly ground.

CONT IN CONTROL IN
CONT OUT CONTROL OUT
(A32, A34 TP504)
This line connects the A32 ADC 1 to A34 ADC 2. This connection determines whether the A32 analog digital converter or the A34 analog digital converter is in control. If an assembly's CONT IN is either high or floating, it is in control. If A34 ADC 2 is plugged in, the CONT IN of A32 ADC 1 is low and A34 ADC 2 is in control.

| | | | | | | | | | | | | | | | | | | | |
|----------------------------------|--|----|----------------|----|------------------|----|-------------|----|------------------|----|---------------------------|----|------------------------------------|----|--------------------|----|------------------------|-----|----------|
| CONV | <p>CONVERT The signal from the A31 Trigger assembly to the A32 and A34 analog digital converter assemblies telling the ADCs to start the conversion process. This signal is 256 kHz except when EXT SAMPLE IN is used. This signal is the same frequency as EXT SAMPLE IN as long as EXT SAMPLE IN is less than or equal to 256 kHz. If the external sample in signal is greater than 256 kHz, the CONVERT signal is then 256 kHz.</p> | | | | | | | | | | | | | | | | | | |
| COS | <p>COSINE (A4 TP24) This is a digital signal from the A4 Local Oscillator to the A5 Digital Filter. When in a frequency shifting mode this signal represents a cosine signal. When in the real mode, COS corresponds to $1 + j0$.</p> | | | | | | | | | | | | | | | | | | |
| COVLDL1 COVLDL2 | <p>INPUT OVERLOAD CHANNEL 1 INPUT OVERLOAD CHANNEL 2 (A32, A34 TP501) Active Low The signals from the A33, A35 Input assemblies to the A32, A34 Analog Digital Converters indicating the front panel input voltage to chassis ground is too high.</p> | | | | | | | | | | | | | | | | | | |
| D0L to D15L | <p>SYSTEM DATA BUS Active Low The system data bus is a bidirectional bus that serves as a general purpose data path for the following assemblies:</p> <table border="0" style="margin-left: 40px;"> <tr><td>A1</td><td>Digital Source</td></tr> <tr><td>A2</td><td>System CPU/HP-IB</td></tr> <tr><td>A3</td><td>Program ROM</td></tr> <tr><td>A4</td><td>Local Oscillator</td></tr> <tr><td>A6</td><td>Digital Filter Controller</td></tr> <tr><td>A7</td><td>Floating Point Transform Processor</td></tr> <tr><td>A8</td><td>Global RAM/Display</td></tr> <tr><td>A9</td><td>Fast Fourier Processor</td></tr> <tr><td>A15</td><td>Keyboard</td></tr> </table> | A1 | Digital Source | A2 | System CPU/HP-IB | A3 | Program ROM | A4 | Local Oscillator | A6 | Digital Filter Controller | A7 | Floating Point Transform Processor | A8 | Global RAM/Display | A9 | Fast Fourier Processor | A15 | Keyboard |
| A1 | Digital Source | | | | | | | | | | | | | | | | | | |
| A2 | System CPU/HP-IB | | | | | | | | | | | | | | | | | | |
| A3 | Program ROM | | | | | | | | | | | | | | | | | | |
| A4 | Local Oscillator | | | | | | | | | | | | | | | | | | |
| A6 | Digital Filter Controller | | | | | | | | | | | | | | | | | | |
| A7 | Floating Point Transform Processor | | | | | | | | | | | | | | | | | | |
| A8 | Global RAM/Display | | | | | | | | | | | | | | | | | | |
| A9 | Fast Fourier Processor | | | | | | | | | | | | | | | | | | |
| A15 | Keyboard | | | | | | | | | | | | | | | | | | |
| DACCLK | <p>DAC CLOCK This clock signal is used by the A1 Digital Source to shift the serial data DACDAT into the A30 Analog Source.</p> | | | | | | | | | | | | | | | | | | |
| DACDAT | <p>DAC DATA This is the serial data out of the A1 Digital Source to the A30 Analog Source.</p> | | | | | | | | | | | | | | | | | | |
| DACL D | <p>DAC LOAD Signal from the A1 Digital Source that latches the serial data DACDAT into the A30 Analog Source.</p> | | | | | | | | | | | | | | | | | | |

| | |
|-------------------------------|--|
| DATA1 | DATA1, DATA2 |
| DATA2 | (A32, A34 TP610) These two signals are the serial data streams from the A32, A34 Analog Digital Converters to the A5 Digital Filter. Data transfer begins three clock cycles after the assertion of DREQL and occurs at a 10.14 MHz rate. The first bit is the data valid bit, followed by the overload status bits, then the 13 bit serial data with the LSB first. |
| DAV | DATA VALID Signal to and from the A2 System CPU to the A22 HP-IB. This line is used in the HP-IB handshake sequence. |
| DAVL | DATA AVAILABLE Active Low The A8 Global RAM sends the A17 Display Interface this control signal after it writes the data for the HP 1345A into the A17 Display Interface registers. The A17 Display Interface then sends DAVL to the HP 1345A which tells the display that data is available. DAVL works with RFDL (Ready For Data) to transfer data to the HP 1345A display. Refer to the HP 1345A service manual section 3-6 for the handshake timing information. |
| DISPLAY OUTPUT X, Y, Z | These signals are outputs of the HP 1345A display. Refer to the HP 1345A operating and service manual for troubleshooting and adjusting the display. |
| DMADTACKL | DMA DATA TRANSFER ACKNOWLEDGE Active Low This signal is from the A5 Digital Filter to the A6 Digital Filter Controller. When a 'read filter status' command or a read/write to a A5 DMA controller register is completed, DMADTACKL goes low. The A6 Digital Filter Controller then sends DTACKL to the A2 System CPU to indicate the command is completed. |
| DREQL | DATA REQUEST (A1 J703-1) Active Low When the A5 Digital Filter is ready for data, it sends the DREQL signal to the A32, A34 Analog Digital Converters. The digital filter expects the data back on the forth clock cycle after the DREQL. This signal is also sent to the A1 Digital Source. The digital source uses the DREQL to synchronize the buffer start signal (BFST) going to the A6 Digital Filter Controller with the sample signal (SAMP) from the A34 Analog Digital Converter. |
| DSA SS | DSA START/STOP (A5 TP13, A6 TP7) This signal corresponds to bit 2 of the A5 Digital Filter assembly command register. The A5 Digital Filter and the A6 Digital Filter Controller use the DSA SS signal for diagnostic testing. |

DSHIFTEN DATA SHIFT
Shift clock from the A1 Digital Source to the A30 Analog Source that is used to shift in the DACDAT data.

DTACKL DATA TRANSFER ACKNOWLEDGE
Active Low
This is an open collector signal that is pulled up to +5V on the A2 System CPU. After an assembly receives the data strobes (UDSL, LDSL, or ASL) and has performed the appropriate read or write operation, it sends the A2 System CPU the handshake signal DTACKL. This signal indicates that the data has been transferred. The CPU puts the bus cycle in the wait mode until it receives the DTACKL signal or 1 ms has passed and BERRL is asserted. The following assemblies use the asynchronous DTACKL signal for data transfer:

- A1 Digital Source
- A3 Program ROM
- A6 Digital Filter Controller
- A7 Floating Point Transform Processor
- A8 Global RAM/Display
- A9 Fast Fourier Processor
- A15 Keyboard

EOC END OF CONVERSION
(A32, A34 TP605)
This signal is used by the A32 ADC 1 and the A34 ADC 2. When both assemblies are installed, ADC 2 tells ADC 1 when it is done with a conversion.

EOI END
Signal to and from the A2 System CPU to the A22 HP-Interface Bus. This line is used to indicate the end of a multiple-byte message on the bus. It is also used in parallel polling.

ENBLL ENABLE
Active Low
~~This is the enable clock for the system bus from the A2 System CPU. It is high for 750 ms and low for 500 ms with a period of 1.25 ms. ENBLL is used to interface synchronous 68000 peripherals (A1 Digital Source, A3 Program ROM, A4 Local Oscillator) to the 68000 (A2 U100).~~

EXT SAMPLE IN EXTERNAL SAMPLE INPUT
(A31 J501)
Sample rate from the rear panel to the A31 Trigger assembly. This signal is active only in external sample mode.

EXT TRIGGER EXTERNAL TRIGGER
(A31 J2)
The external trigger input from the front panel to the A31 Trigger assembly. This input has a 50 kΩ input resistance and a range of ±10V.

FLTRST DIGITAL FILTER MASTER RESET
 This signal is from the A5 Digital Filter controller to the A6 digital filter assembly. It goes high when a read filter status command or a read/write to an internal DMA controller register command has been completed. FLTRST is used to synchronize the channel 1 and channel 2 digital filter circuits.

GA1L to GA16L GLOBAL ADDRESS BUS
 Active Low
 The global address bus consists of 16 lines that allow the A8 Global RAM to be addressed by the following assemblies:

- A2 System CPU
- A5 Digital Filter
- A7 Floating Point Transform Processor
- A9 Fast Fourier Processor

GD0L to GD15L GLOBAL DATA BUS
 Active Low
 The global data bus provides a communication path between the following assemblies:

- A2 System CPU
- A5 Digital Filter
- A7 Floating Point Transform Processor
- A8 Global RAM/Display
- A9 Fast Fourier Processor
- A17 Display Interface

GDSL GLOBAL DATA STROBE
 Active Low
 When a device reads A8 Global RAM, the low to high edge of the global data strobe signal indicates valid RAM data is on the global data bus. Valid data must be set up a minimum of 30 ns before the rising edge of GDSL and held a minimum of 20 ns afterwards.

GLOBAL

GLOBAL BUS

The global bus is controlled by the arbiter on the A8 Global RAM. This bus provides a communication path between the following assemblies:

- A2 System CPU
- A5 Digital Filter
- A7 Floating Point Transform Processor
- A8 Global RAM/Display
- A9 Fast Fourier Processor
- A17 Display Interface

The global bus consists of the following signals:

- GD0L to GD15L global data bus
- GA1L to GA16L global address bus
- GDSL global data strobe
- GR/GWL global read/global write

Memory Request lines MRFFTL, MRDF2L, MRDF1L, MR68L, and MRFPLL.

Memory Grant lines MGFFT, MGDF2L, MGDF1L, MG68L, and MGFPLL.

- GR/GWL** GLOBAL READ/GLOBAL WRITE
Active Low
When low, this open collector signal defines the global data bus transfer as a write cycle. When it is high, the transfer is a read cycle.
- GRAMRSTL** GLOBAL RAM RESET
Active Low
Signal from the A2 System CPU to the A8 Global RAM. When power is applied to the instrument or A2 S1 is activated, GRAMRSTL goes low and resets the global RAM. This signal is used to reset the global RAM instead of RESETL, so a software reset does not reset the A8 Global RAM
- GSMPLL** GLOBAL SAMPLE
Active Low
At this time, this signal from the A8 Global RAM is not used by any assembly in the instrument.
- GSW** PASS GAIN SWITCH
(A32, A34 TP604)
This signal is used by the A32 ADC 1 and the A34 ADC 2. GSW is from the ADC controller to the ADC process switch. It is used with CLADC to determine the input to the A/D Converter IC. When both assemblies are installed, the GSW is used as an input for timing to the A32 ADC 1 assembly's controller.

- HD1 to HD8** DATA
These lines are the data lines between the A2 System CPU and the A22 HP-Interface Bus.
- HIGH INPUT 1** HIGH INPUT 1
HIGH INPUT 2 HIGH INPUT 2
(A33, A35 J300-1)
These are the input signals from the front panel BNC centers to the A33 Input 1 and A35 Input 2 assemblies.

| | |
|-------------------|--|
| HLFSCL1 | HALFSCALE CHANNEL 1 |
| HLFSCL2 | HALFSCALE CHANNEL 2 (A32, A34 TP503) These signals are status signals from the A32, A34 Analog Digital Converters and are asserted whenever the analog input exceeds half-range in amplitude. They are latched into the A5 Digital Filter and can be read by the A2 System CPU as part of the digital filter status word. HLFSCCL1 and HLFSCCL2 also go to the A15 Keyboard to turn on the halfscale LED. |
| HP-IB | HP-IB This is the HP-IB input from the rear panel to the A22 HP-Interface Bus assembly. The A22 HP-IB connects the rear panel input to the A2 System CPU assembly. |
| INBLKEMPTY | PARALLEL INPUT DATA BLOCK EMPTY This signal is from the A5 Digital Filter to the A6 Digital Filter Controller. INBLKEMPTY is used when parallel data from the A8 Global RAM is used instead of serial data from the A32 ADC 1 or A34 ADC 2 assemblies. This signal goes high when the current input block of the A8 Global RAM data is received by the A5 Digital Filter. The positive transition of this signal sets the corresponding interrupt flag on the A6 Digital Filter Controller. |
| INPUT1 | CHANNEL 1 ANALOG OUT |
| INPUT2 | CHANNEL 2 ANALOG OUT (A33, A35 TP400) These signals are the conditioned front panel input signals from the A33, A35 Input assemblies to the A32, A34 Analog Digital Converters. |
| IFC | INTERFACE CLEAR Signal to and from the A2 System CPU to the A22 HP-IB. When IFC is set all talkers and listeners on the HP-IB are unaddressed, and controllers go to the inactive state. |
| IRQT2L | INTERRUPT REQUEST 2 Active Low Interrupt request line from the A15 Keyboard to the A2 System CPU. This open collector signal is also used by the A2 programmable timer module. |
| IRQT3L | INTERRUPT REQUEST 3 Active Low Interrupt request line from the A7 Floating Point Transform Processor to the A2 System CPU. This is an open collector signal. |
| IRQT4L | INTERRUPT REQUEST 4 Active Low Interrupt request line from the A9 Fast Fourier Processor to the A2 System CPU. This is an open collector signal. |

| | |
|--------------------------------|--|
| IRQT5L | <p>INTERRUPT REQUEST 5 Active Low Interrupt request line from the A6 Digital Filter Controller to the A2 System CPU. This is an open collector signal.</p> |
| IRQT6L | <p>INTERRUPT REQUEST 6 Active Low Interrupt request line from the A8 Global RAM to the A2 System CPU. This is an open collector signal.</p> |
| KYBRDL | <p>KEYBOARD Active Low Signal from the A2 System CPU which selects the A15 Keyboard. The system processor uses this line along with A1L and A2L to address the keyboard.</p> |
| LCNV | <p>LOCAL A/D CONVERT (A32, A34 TP606) This signal is used by the A32 ADC 1 and the A34 ADC 2. The ADC controller sends this signal to the A/D converter IC to start converting. When both assemblies are installed, this signal also goes to the A32 ADC 1 assembly's A/D converter IC.</p> |
| LD0 to LD15 | <p>LOCAL DATA BUS These bidirectional data lines are used by the A5 Digital Filter and the A6 Digital Filter Controller. During a A5 Digital Filter read/write operation, these data lines are the inverted version of the system data bus.</p> |
| LDCH1L LDCH2L | <p>LOAD CHANNEL 1 LOAD CHANNEL 2 Active Low Signal from the A1 Digital Source that latches command data word CNTLD into the A33, A35 Input assemblies and the A32, A34 ADC assemblies.</p> |
| LDSL | <p>LOWER DATA STROBE Active Low Signal from the A2 System CPU indicating data is transferring on the lower half of the system data bus (D0 to D7). When LDSL goes low for a read cycle, the A2 System CPU is expecting valid data to be placed on the lower half of the data bus. In the write cycle a low on LDSL indicates there is valid data on the lower half of the system data bus.</p> |
| LDSRCL | <p>LOAD ANALOG SOURCE Active Low Signal from the A1 Digital Source that latches command data word CNTLD into the A30 analog source's shift register.</p> |

| | |
|------------------------------------|---|
| LDTRGL | <p>LOAD TRIGGER Active Low Signal from the A1 Digital Source that latches command data word CNTLD into the A31 Trigger assembly's shift register.</p> |
| LOW INPUT 1 LOW INPUT 2 | <p>LOW INPUT 1 LOW INPUT 2 (A33, A35 J300-3) These signals are the inputs from the front panel BNC shells to the A33 Input 1 and A35 Input 2 assemblies.</p> |
| MG68L | <p>CPU MEMORY GRANT Active Low After the A2 System CPU asserts the memory request line, the A8 Global RAM returns a memory grant. The memory grant signal clears the memory request signal (MR68L), enables the assertion of the global read/write signal (GR/GWL), and allows the A2 System CPU to use the global address bus (GA1L to GA16L)</p> |
| MGDF1L MGDF2L | <p>MEMORY GRANT DIGITAL FILTER CHANNEL 1 MEMORY GRANT DIGITAL FILTER CHANNEL 2 Active Low The A8 Global RAM responds to bus requests MRDF1L and MRDF2L by assertion of MGDF1L or MGDF2L. The two memory grant signals are asserted for about 410 ns. The global RAM expects valid data to be on the bus within 80 ns after the memory grant is given.</p> |
| MGFFTL | <p>FFT MEMORY GRANT Active Low (A9 TP3) After the A9 FFT asserts the memory request line, the A8 Global RAM returns a memory grant. The memory grant signal clears the memory request signal (MRFFT) and enables the assertion of the global read/write signal (GR/GWL).</p> |
| MGFPPL | <p>FPP MEMORY GRANT Active Low After the A7 FPP asserts the memory request line, the A8 Global RAM returns a memory grant. The memory grant signal clears the memory request signal (MRFPPL) and enables the assertion of the global read/write signal (GR/GWL).</p> |
| MR68L | <p>CPU MEMORY REQUEST Active Low The A2 System CPU asserts the memory request line when it wishes to address the A8 Global RAM.</p> |
| MRDF1L MRDF2L | <p>MEMORY REQUEST CHANNEL 1 MEMORY REQUEST CHANNEL 2 Active Low These two signals are from the A5 Digital Filter to A8 Global RAM to request use of the global bus for channel 1 data or channel 2 data.</p> |

| | |
|-----------------|--|
| MRFFTL | <p>FFT MEMORY REQUEST Active Low The A9 FFT asserts the memory request line when it wishes to address the A8 Global RAM.</p> |
| MRFPPPL | <p>FPP MEMORY REQUEST Active Low The A7 FPP asserts the memory request line when it wishes to address the A8 Global RAM.</p> |
| MSMP | <p>EXTERNAL SAMPLE ERROR (A32, A34 TP611) Active High Status signal from the A32, A34 Analog Digital Converters to the A5 Digital Filter. MSMP is asserted when operating in the external sample mode and the sample frequency is too fast. This signal is latched by the digital filter and can be read by the A2 System CPU as part of the digital filter status word.</p> |
| MYADDRSL | <p>MY ADDRESS Active Low The A6 Digital Filter Controller sends the A5 Digital Filter this signal when the A2 System CPU is addressing A5 Digital Filter. MY ADDRESS is used by the A5 Digital Filter for command decoding.</p> |
| NCLK | <p>CHIRP CLOCK (A4 TP19) The A1 Digital Source sends this signal to the A4 Local Oscillator at the beginning of chirp to reset the A4 Local Oscillator to the initial frequency of the chirp and to zero the phase. This signal is present when other modes are used, but the A4 Local Oscillator uses NCLK only for the chirp mode.</p> |
| NDAC | <p>DATA NOT ACCEPTED Signal to and from the A2 System CPU to the A22 HP-IB. This line is used in the HP-IB handshake sequence.</p> |
| NDAT | <p>LOCAL OSCILLATOR DATA (A4 TP16) Sine or dc data from the A4 Local Oscillator to the A1 Digital Source.</p> |
| NDCK | <p>DATA CLOCK (A4 TP14) The NDCK signal from the A4 Local Oscillator clocks the LO serial data (NDAT) into the the A1 Digital Source.</p> |
| NLD | <p>LOAD DIGITAL SOURCE (A4 TP17) Signal from the A4 Local Oscillator that latches the LO's serial data (NDAT) into the A1 Digital Source.</p> |

| | |
|--------------------------------|---|
| NRFD | <p>NOT READY FOR DATA</p> <p>Signal to and from the A2 System CPU to the A22 HP-IB. This line is used in the HP-IB handshake sequence.</p> |
| NSYNC | <p>NOISE SYNCHRONIZATION</p> <p>Signal from the A4 Local Oscillator to the A1 Digital Source. The digital source uses this signal for synchronizing the A1 LO receiver data with the chirp clock (NCLK).</p> |
| OTEMPL | <p>OVER TEMPERATURE</p> <p>(A18 J1-13)</p> <p>Signal from the A18 Power Supply to the A12 Mother Assembly. This signal from the over temperature circuit on the power supply shuts down the power supply if the temperature exceeds 80° centigrade.</p> |
| OVL D1 OVL D2 | <p>OVERLOAD CHANNEL 1</p> <p>OVERLOAD CHANNEL 2</p> <p>(A32, A34 TP502)</p> <p>Status signals from the A32, A34 Analog Digital Converters that are asserted whenever the analog input exceeds full scale. They are latched by the A5 Digital Filter and can be read by the A2 System CPU as part of the digital filter status word.</p> |
| PWRDNL | <p>POWER DOWN</p> <p>Active Low</p> <p>(A18 J1-14, A2 J16)</p> <p>Signal from the A18 Power Supply to the A30 Analog Source and the A2 System CPU. When this signal is active a power loss is occurring.</p> |
| PWRUP | <p>POWER UP</p> <p>(A18 J1-15, A2 J15)</p> <p>When a power failure has occurred the instrument is in the reset mode until the PWRUP signal goes high. This signal from the A18 Power Supply goes to the A2 System CPU. PWRUP is high when +5S is $\geq +4.75V$.</p> |
| REF IN | <p>EXTERNAL REFERENCE</p> <p>External clock reference from the rear panel to the A31 Trigger assembly. If the input signal is 1, 2, 5, or 10 MHz $\pm 0.01\%$, and between 0 and 20 dBm; the internal 10.24 MHz clock phase locks to the input frequency. REF IN has a 50Ω input resistance.</p> |
| REMTGL | <p>REMOTE TRIGGER</p> <p>Active Low</p> <p>When a HP-IB trigger is used, the A2 System CPU sends the trigger signal over the remote trigger line to the A1 Digital Source.</p> |
| REN | <p>REMOTE ENABLE</p> <p>Signal between the A2 System CPU and the A22 HP-IB. This line is used to enable bus compatible instruments to respond to commands from the controller or another talker.</p> |

| | |
|---------------------|--|
| RESETL | <p>RESET Active Low</p> <p>This signal resets the instrument. The instrument is reset by the A2 System CPU at power-up, when the reset switch A2 S1 is pressed, or by a software reset. RESETL goes to every assembly except the A5 Digital Filter, the A17 Display Interface, the A18 Power Supply, and the A22 HP-Interface bus.</p> |
| RFDL | <p>READY FOR DATA Active Low</p> <p>The A17 Display Interface sends the A8 Global RAM this control signal when the HP 1345A is ready for data. RFDL works with DAVL (data available) to transfer data to the HP 1345A display. Refer to the HP 1345A service manual section 3-6 for the handshake timing information.</p> |
| SAMP | <p>SAMPLE (A32, A34 TP608; A1 TP8)</p> <p>This is the signal from the A34 ADC 2 to the A1 Digital Source assembly saying a sample has been taken.</p> |
| SGND | <p>SIGNAL GROUND (A33, A35 J300-2)</p> <p>A12 Mother Assembly ground; connected to all the assemblies.</p> |
| SINE | <p>SINE (A4 TP23)</p> <p>This is a digital signal from the A4 Local Oscillator to the A5 Digital Filter. When in a frequency shifting mode this signal represents a sine signal. When in the real mode, SINE corresponds to $1 + j0$.</p> |
| SMPOUT | <p>SAMPLE OUT (A18 J1-12)</p> <p>The 256 kHz clock from the A31 Trigger to the A18 Power Supply. This signal is used to synchronize the pulse width modulator on the power supply with the 10.24 MHz clock.</p> |
| SOURCOUT@ | <p>SOURCE OUT ANALOG (A30 J200)</p> <p>This is the A30 source output to the front panel.</p> |
| SRCOUT FALTL | <p>SOURCE OUT FAULT Active Low</p> <p>Signal from the A30 Analog Source to the A1 Digital Source. This signal goes low when the output of the source is greater than 12 volts.</p> |
| SRQ | <p>SERVICE REQUEST</p> <p>Signal to and from the A2 System CPU to the A22 HP-IB. This line is set low by any instrument requesting service.</p> |

| | |
|-----------------|--|
| STIM GND | <p>STIMULUS GROUND</p> <p>Ground signal from A30 Analog Source to A33, A35 Input assemblies for stimulus signal.</p> |
| STIM@ | <p>STIMULUS ANALOG (A30 TP8)</p> <p>Signal from the A30 Analog Source to the A33, A35 Input assemblies. This signal can be the source output or the calibrator output.</p> |
| SYNC2 | <p>SERIAL DATA ACCEPTED (A4 TP8)</p> <p>This signal is from the A5 Digital Filter to the A6 Digital Filter Controller and the A4 Local Oscillator. This signal goes high when the digital filter accepts an input data word. SYNC2 is asserted within 25 ns of the rising edge of the 10.24 MHz clock for about 100 ns. The frequency of SYNC2 is determined by the rate of data acceptance. SYNC2 is used by the local oscillator and digital filter controller to initiate inputting serial sine/cosine data into the digital filter. When the LO receives SYNC2, it sends a complex value to the A5 Digital Filter and a real value to the A1 Digital Source.</p> |
| SYNC OUT | <p>ANALOG PULSE (A1 J10)</p> <p>This signal goes to the user output on the rear panel. It comes from the A1 Digital Source. SYNC OUT is high when burst is on and low when burst is off.</p> |
| SYSCLK | <p>SYSTEM CLOCK (A6 W2-1)</p> <p>This is a 4.915 MHz clock generated by the A6 Digital Filter Controller. It is used by the A6 Digital Filter Controller and the A5 Digital Filter to clock various sequential circuits.</p> |
| SYSTEM | <p>SYSTEM BUS</p> <p>The system bus is controlled by the A2 System CPU. The system CPU uses these lines to give commands and receive status from the following assemblies:</p> |

| | |
|-----|------------------------------------|
| A1 | Digital Source |
| A3 | Program ROM |
| A4 | Local Oscillator |
| A6 | Digital Filter Controller |
| A7 | Floating Point Transform Processor |
| A8 | Global RAM/Display |
| A9 | Fast Fourier Processor |
| A15 | Keyboard |

The system bus consists of the following signals:

- A1L to A23L system address bus
- D0L to D15L system data bus
- ASL address strobe
- UDSL upper data strobe
- LDSL lower data strobe
- WRITEL read/write
- DTACKL data transfer acknowledge
- VIOL valid I/O address
- ENBLL enable
- VMAL valid memory address
- REMTGL remote trigger
- RESETL reset
- IRQT2L to IRQT6L interrupt request lines
- VPAL valid peripheral address

TRH TRACK AND HOLD
 (A32, A34 TP609)
 This signal is used by the A32 ADC 1 and the A34 ADC 2. TRH is from the ADC controller to the ADC track and hold switch. When both assemblies are installed, the TRH signal from ADC 2 controls the track and hold switch on ADC 1.

TRIG1@ ANALOG TRIGGER CHANNEL 1
TRIG2@ ANALOG TRIGGER CHANNEL 2
 (A32, A34 TP303)
 Conditioned analog signal from A32, A34 Analog Digital Converters to the A31 Trigger assembly.

TRIGGER TRIGGER
 This signal is from the A6 Digital Filter Controller to the A15 Keyboard. TRIGGER controls the front panel trigger LED as follows:

| Measurement Mode | Measuring off | Measuring on |
|-------------------|--|-------------------------------|
| Free run | LED off | LED on |
| Outside Real Time | — | Flash LED |
| Triggered | Flash LED when input exceeds trigger level | Flash LED when trigger occurs |
| Time Capture | LED off | Flash LED when trigger occurs |

TRIGRO TRIGGER SIGNAL
 (A31 TP3)
 The trigger signal from the A31 Trigger assembly to the A1 Digital Source and the A6 Digital Filter Controller. This signal is asserted whenever the input has exceeded the trigger level. TRIGRO is used by the digital filter to set the TRIGGER signal.

UDSL UPPER DATA STROBE
Active Low
Signal from the A2 System CPU indicating data is transferring on the upper half of the system data bus (D8L to D15L). When UDSL goes low for a read cycle, the A2 System CPU is expecting valid data to be placed on the upper half of the data bus. In the write cycle, a low on UDSL indicates there is valid data on the upper half of the data bus.

UNLOCK UNLOCK
When this signal from the A31 Trigger assembly is active, the phase lock loop is unlocked. It is only active when an external reference is used. UNLOCK is passed through the A1 Digital Source assembly so the A2 System CPU can read the signal.

VIOL VALID I/O ADDRESS
Active Low
An I/O assembly may be addressed only when this line is low. This signal from the A2 System CPU is part of the address for the following assemblies:

| | |
|----|------------------------------------|
| A1 | Digital Source |
| A4 | Local Oscillator |
| A6 | Digital Filter Controller |
| A7 | Floating Point Transform Processor |
| A8 | Global RAM/Display |
| A9 | Fast Fourier Processor |

VIOL is also used by devices in the A2 System CPU assembly.

VMAL VALID MEMORY ADDRESS
Active Low
Signal from the A2 System CPU to the A4 Local Oscillator indicating the beginning of a synchronous bus transfer. After receiving the valid peripheral address signal (VPAL) from the local oscillator, it asserts VMAL synchronized with the enable clock (ENBLL).

VPAL VALID PERIPHERAL ADDRESS
(A4 TP5)
Active Low
Handshake signal from the A4 Local Oscillator to the A2 System CPU. The local oscillator sends the VPAL signal to the system CPU when the LO recognizes that it has been addressed. When the system CPU receives the VPAL signal, it asserts the valid memory address signal (VMAL) which is synchronized with the enable clock (ENBLL).

WRITEL READ/WRITE
This signal defines the system data bus transfer as a read or write cycle. When WRITEL is high the A2 System CPU is reading data from the system data bus. When WRITEL is low the A2 System CPU is writing data onto the system data bus.

SECTION VII FAULT ISOLATION

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SECTION VII FAULT ISOLATION

7-1 INTRODUCTION

This section contains the information required to isolate failures to the circuit board level. To accomplish this, extensive use is made of the power-up tests and the self-tests. After isolating the failure to an assembly go to Section VIII, "Service" to continue the failure isolation process.

The fault isolation procedure assumes only one independent failure. Multiple failures may cause false results in the diagnostic tests.

How To Use This Section

Start If the display and soft keys are operative, go to paragraph 7-7, "Test All".

If the instrument is displaying the 'MONITOR TEST LOG' or 'PROGRAM ROM DEAD', go to paragraph 7-5, "Initial Conditions Test".

If there is no display, incorrect display, or the instrument does not respond when a key is pressed, go to paragraph 7-5, "Initial Conditions Test".

For chirp and noise source failures, go to paragraph 7-9, "Source Failures".

For trigger failures, go to paragraph 7-11, "Isolating Trigger Failures".

For HP-IB failures, go to paragraph 8-6, "A2, A22 System CPU/HPIB".

For intermittent failures, go to paragraph 7-12, "Loop Mode and Intermittent Failures".

Reference For component locators and schematics refer to Section IX.

For the location of cables and boards refer to figure 4-1 in Section IV.

To find a particular soft key refer to paragraph 7-14, "SPCL FCTN Key Map".

To find the software revision code, refer to part B of paragraph 7-15, "Test Log and Fault Log Descriptions".

To understand the self-diagnostic process, refer to paragraph 7-16, "Diagnostic Descriptions".

To understand the self-calibration process, refer to paragraph 7-17, "Self-Calibration".

To understand the instrument's operation and signal mnemonics refer to Section VI.

Verify Use the oscilloscope waveforms in paragraph 7-13 to verify correct operation at various test points in the instrument.

Troubleshooting Hints

1. Intermittent cables can cause hardware failures.
2. Noise or spikes on power supplies can cause instrument failure.
3. Incorrect bias supply voltages can cause false diagnostic messages.
4. Use front panel diagnostics to isolate the problem before extensive troubleshooting.
5. It is possible that one circuit board can load another circuit board causing the wrong one to appear to be defective. This applies to both analog and digital signals.
6. Whenever possible, divide the circuit under test in half (half-splitting).
7. If the name of a nonnumerical key or 'ENTRY Not Enabled' appears in the lower left of the display immediately after the power-up routine, there may be a stuck key or shorted trace on the keyboard (go to 8-15).
8. Do not remove any assembly from the instrument with the power on. There are several sensitive components in the instrument that may be damaged by power supply glitches.
9. To stop the instrument calibration, press soft key S8 (last soft key) just after the display appears. Note: TEST ALL and SELF TEST may not be valid if this key is pressed before these tests are done.
10. ~~A12 Mother Board failures are not isolated in this section. If the mother board is suspected of failing, refer to paragraph 8-14, "A12 Mother Board".~~
11. Measurements in this section are only approximate (usually ± 1 dB or 10%) unless stated otherwise.

NOTE

FFT Global Interface . . . FAILS

This failure message may occur if the instrument is internally set with unknown parameters before running the test (this can be caused by various measurement setups). Before running any of the FFT self-tests, press the HP 3562A keys as follows:

PRESET . . . RESET

7-2 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for troubleshooting is listed in table 1-4. Any item which meets or exceeds the critical requirements can be substituted for the model listed. These procedures are designed to be run with a minimum amount of equipment.

7-3 LOGIC CONVENTIONS

Positive logic convention is used in this manual unless otherwise noted. Positive logic conventions define a logic "1" or "High" as more positive voltage and a logic "0" or "Low" as the more negative voltage.

7-4 SAFETY CONSIDERATIONS

The HP 3562A is a Safety Class 1 instrument (provided with a protective earth terminal). The instrument and manuals should be reviewed for safety markings and instructions before operation. Refer to the safety symbol table in the preface of this manual.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury.

CAUTION

Do not insert or remove any circuit board in the HP 3562A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards.

WARNING

230 Vdc is present in the A18 power supply assembly even with the line switch in the off position and the power cord removed. Be extremely careful when working in the power supply area. This high voltage could cause serious personal injury if contacted. To discharge the capacitors holding this charge perform steps 1 through 3.

- 1. Remove the power cord from the rear panel.*
- 2. Remove the bottom cover and power supply shield.*
- 3. Wait two minutes after turning the power off to allow the capacitors to discharge.*

7-5 INITIAL CONDITIONS TEST

A. Power Supply Check

1. Disconnect the power cord from the rear panel. Remove the bottom cover.
2. Connect the power cable and press the line switch on.
3. Use table 7-1 to verify the power supply is operating correctly. If any of the values are incorrect start troubleshooting with the A18 Power Supply (go to 8-16).

Table 7-1 Power Supply Nominal Values

Return Location is A18 TP13

| Supply Name | Output Location | Nominal Voltage | Voltage Tolerance | Ripple Tolerance |
|-------------|-----------------|-----------------|-------------------|------------------|
| +5 | A12 J16-1 | +5V | ±0.3V | 50 mV |
| +30V | A12 W13-1 | +30V | ±1.8V | 10 mV |
| -30V | A12 W13-2 | -30V | ±1.8V | 10 mV |
| +15A | A12 W13-3 | +15V | ±0.9V | 10 mV |
| -15A | A12 W13-4 | -15V | ±0.9V | 10 mV |
| +5FNTEND | A12 W13-5 | +5V | ±0.3V | 50 mV |
| +2.6V | A12 W13-6 | +2.6V | ±0.16V | 50 mV |
| +8S1 | A12 W13-7 | +8V | ±0.48V | 25 mV |
| +8S2 | A12 W13-8 | +8V | ±0.48V | 25 mV |
| +15S | A12 W13-9 | +15V | ±0.9V | 25 mV |
| -15S | A12 W13-10 | -15V | ±0.9V | 25 mV |
| OTEMPL | A12 W13-12 | TTL Level High | | |
| PWRDNL | A12 W13-13 | TTL Level High | | |
| PWRUP | A12 W13-14 | TTL Level High | | |

B. Keyboard Check

1. Press the line switch off.
2. Disconnect cable W10 (A12 J15) from the A12 Mother Board.
3. Connect the power cable and press the line switch on.
4. Reset the keyboard by putting A15 J9 to the test (T) position, then back to the normal (N) position (see note).

NOTE

On some A15 revisions the A15 J9 jumper is not in a convenient location. If this is the case, the keyboard can still be reset using the following procedure:

- a. *Press the line switch off.*
 - b. *Disconnect cable W17 (A12 J16) from the A12 Mother Board.*
 - c. *Connect a +5V dc power supply and ground to W17, +5V to the red wire and ground to the black wire.*
 - d. *To reset the keyboard, cycle the +5V power supply off, then on.*
5. The keyboard should respond as follows when it is reset:
 - a. Beeps the beeper and flashes all the LEDs three times except CR12 (Triggering), CR17 (Half Range), and CR19 (Half Range). These LEDs will flash on and stay on since they are controlled by other assemblies.
 - b. Beeps the beeper and then lights the LEDs one at a time in a pattern from left to right, top to bottom.
 - c. Beeps the beeper again and then all the lights should remain on.

 6. If the keyboard does not pass this test start troubleshooting with the A15 Keyboard (go to 8-15).
 7. This test only validates part of the keyboard, it does not validate the system bus interface circuits.
 8. Press the line switch off.
 9. Connect cables W10 and W17 to the A12 Mother Board.

NOTE

The keyboard cable (W10) can easily be connected wrong! After connecting the cable, verify that both rows of pins are connected.

C. Display Check

1. Remove the top cover and press the line switch on.
2. Set jumper A17 W1 (located in hole in display shield) to the test (T) position with the power ON.
3. The pattern displayed should be the same as shown in figure 7-1. The main lines should all connect as shown and the lines in the lower right corner should be parallel. If this pattern is not displayed start troubleshooting with the HP 1345A Display (go to 8-12).
4. Set jumper A17 W1 to the normal (N) position.

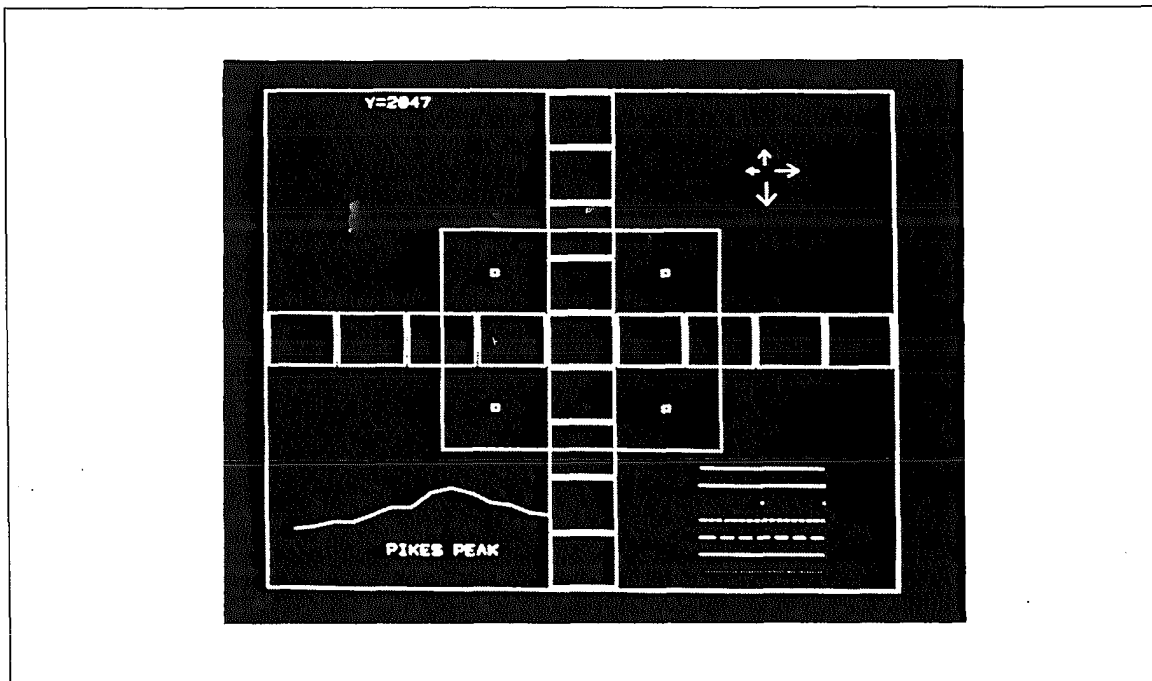


Figure 7-1 Display of Verification Pattern

D. Clock Check

1. Remove the top cover and press the line switch on.
2. Use table 7-2 to verify various clocks in the instrument. If any of the values are incorrect, go to Section VIII.

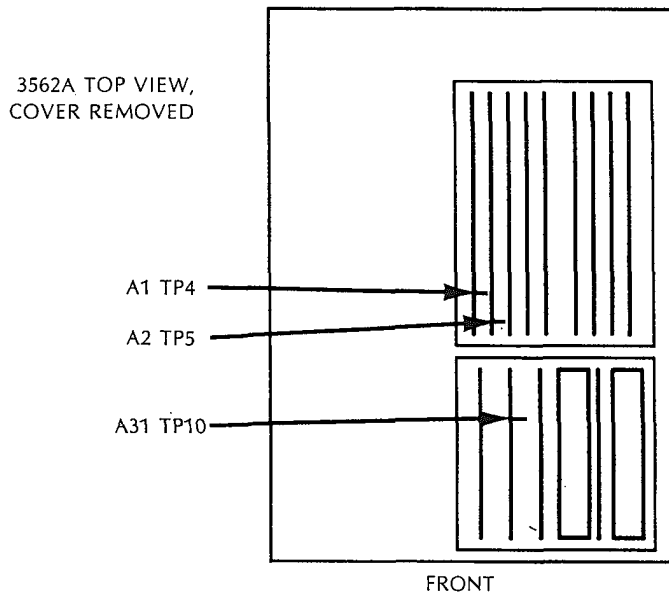


Table 7-2 Clocks

| Test Location | Signal Name | Waveform Number | Probable Cause of Failure | Go To |
|---------------|-------------|-----------------|---------------------------|-------|
| A31 TP10 | 20.48 MHz | #1 | A31 Trigger | 8-18 |
| A1 TP4 | 10.24 MHz | #2 | A31 Trigger | 8-18 |
| A2 TP5 | 8 MHz | #3 | A2 System CPU | 8-6 |

E. If the fault has not been found, go to paragraph 7-6, "Power-Up Tests".

7-6 POWER-UP TESTS

Introduction

The power-up test procedure is used when there is no display, incorrect display, or the instrument does not respond when a key is pressed. The initial conditions test (paragraph 7-5) must be completed before performing the power-up test procedure.

The power-up tests consist of two sets of tests, low-level and high-level. The low-level tests exercise the A2 System CPU, the A3 Program ROM, the A8 Global RAM, the global bus, and the system bus. Fault and pass codes for these core assemblies are displayed using the A2 System CPU test LEDs (A2 DS3, A2 DS4). The high-level power-up tests exercise the A9 FFT, A7 FPP, A5 DGTL FLTR, and A6 D FLTR CONT assemblies. Faults on these assemblies are displayed in the test log (refer to table 7-6 for the description of these messages). The instrument performs a calibration if the power-up tests pass.

Power-up test failures may be caused by one of the following conditions:

1. A core assembly is defective (A2, A3, A8).
2. An assembly on the system bus or global bus is defective, causing a bus failure.
3. The A15 Keyboard system bus interface circuits are defective. (This may be the case when the display is normal after power-up but the instrument does not respond when a key is pressed.)
4. A control line is defective.

Power-Up Test Procedure

To find the cause of the failure, start by referring to table 7-4 for the location of the A2 Test LEDs and the LEDs to Hex code translation.

A. To verify the core assemblies are operating correctly, perform steps 1 through 6:

1. Remove the top cover.
2. Press the line switch on.
3. Press the reset switch A2 S1 (reset switch on A2 CPU).
4. After the reset switch is pressed, the A2 System CPU should flash the test LEDs (A2 DS3, A2 DS4), light the LEDs one at a time, and cycle through several codes as listed in table 7-3. When finished, A2 DS1 should be off.

Table 7-3 LEDs Pass Sequence

| Binary | Hex | ≈ Time Visible | Description |
|-----------|-----|----------------|-----------------------------------|
| 0000 0101 | 05 | 1s | System Processor test |
| 0001 1110 | 1E | 2.5s | Starting Program ROM check sum |
| 1011 0101 | B5 | 3.6s | Starting Global RAM Test |
| 1011 0110 | B6 | 15s | Starting high-level power-up test |
| 1011 0111 | B7 | Remains Lit | Power-up Tests finished |

For A2 System CPU, A3 Program ROM, and system bus test failures, the power-up sequence stops on the first failure and displays the pass/error code, then stops.

For the Global RAM test failures (chart line #22 to #29), the power-up sequence displays Hex B5 while the test tries to isolate the failure (up to 3.5 minutes!), then one of the following occurs:

- a. B5 (Hex) continues to be displayed on the A2 Test LEDs.
 - b. Another Global RAM test pass/error code is displayed and the sequence stops.
5. If the LEDs pass sequence does not occur, A2 DS1 is on, or the instrument does not display the special function menu when SPCL FCTN is pressed; go to part C.
 6. If the LEDs pass sequence occurs and the instrument responds when SPCL FCTN is pressed (the special function menu is displayed) but the display is defective, an assembly on the global bus may be defective. To test the global bus when this is occurring, go to part B.
 7. If the LEDs pass sequence occurs but the instrument does not respond when SPCL FCTN is pressed, a control line may be defective, go to paragraph 7-10, "Control Line Test".

B. Perform this procedure (steps 1 through 13) if the display is defective but the LEDs pass sequence occurs and the instrument responds when SPCL FCTN is pressed:

1. Press the line switch off.
2. Remove the following assemblies:
 - A5 Digital Filter
 - A7 FPP
 - A9 FFT

3. Press the line switch on and the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST      . . . . . TEST
                               MEMORY . . . . . GLOBAL
                                                RAM
    
```

If the display does not appear as in figure 7-2, start troubleshooting with the A8 Global RAM (go to 8-11).

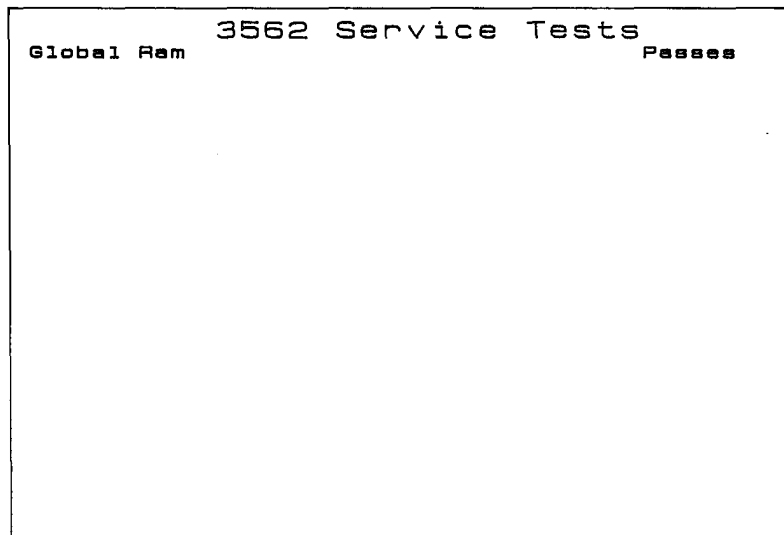


Figure 7-2 Global RAM test passes

4. Press the line switch off.
5. Replace the A7 FPP assembly.
6. Press the line switch on and the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST      . . . . . TEST
                               PROC  . . . . . TEST
                                                FPP      . . . . . FPP
                                                                FUNCTION
    
```

If this test fails, start troubleshooting with the A7 FPP (go to 8-10).

7. Press the line switch off.
8. Replace the A9 FFT assembly.

9. Press the line switch on and the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST  . . . . . TEST
                        PROC  . . . . . TEST
                                      FFT  . . . . . FFT
                                                FUNCTION

```

If this test fails, start troubleshooting with the A9 FFT (go to 8-13).

10. Press the line switch off.

11. Replace the A5 DGTL FLTR assembly.

12. Press the line switch on and the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST  . . . . . TEST
                        PROC  . . . . . TEST
                                      DFA  . . . . . FILTER
                                                TEST

```

If this test fails, start troubleshooting with the A5 DGTL FLTR (go to 8-9).

13. If the cause of the failure has not been found, go to paragraph 7-10, "Control Line Test".

C. Perform this procedure (steps 1 through 20) if the LEDs pass sequence does not occur, A2 DS1 is on, or the instrument does not display the special function menu when SPCL FCTN is pressed:

1. Press the line switch off.

2. Remove the bottom cover.

3. Disconnect cable W10 from the A12 Mother Board.

4. Remove the following assemblies:

- A1 Digital Source
- A3 Program ROM
- A4 Local Oscillator
- A5 Digital Filter
- A6 Digital Filter Controller
- A7 FPP
- A8 Global RAM/Display
- A9 FFT

5. Pull the following assemblies up in their card nests so they are no longer connected to the A12 Mother Board:

- A30 Analog Source
- A31 Trigger
- A32 ADC 1
- A33 Input 1
- A34 ADC 2
- A35 Input 2

6. Press the line switch on. The LEDs pass sequence should stop on Hex B1 and A2 DS1 should be on. If Hex B1 is not displayed, start troubleshooting with the A2 System CPU (go to 8-6).

7. Press the line switch off.

8. Replace the A3 Program ROM assembly.

9. Press the line switch on. The LEDs pass sequence should stop on Hex B5 and A2 DS1 should be off. If Hex B5 is not displayed, go to part E.

10. Press the line switch off.

11. Replace the A8 Global RAM.

12. Press the line switch on. The Global RAM and Global Bus tests are now performed. The LEDs pass sequence should now occur (it takes about 40s to complete) and A2 DS1 should be off. If the LEDs pass sequence does not occur go to part E.

13. The display should now appear as shown in figure 7-3. If the display is defective, the probable cause of the failure is the A8 Global RAM or A17 Display Interface (go to 8-11).

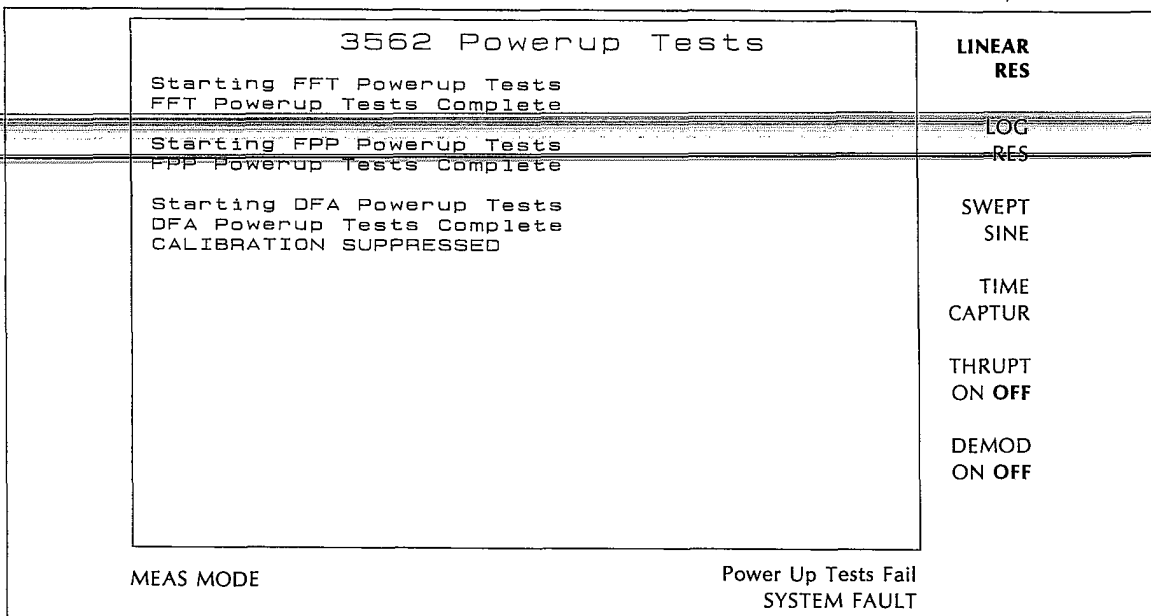


Figure 7-3 Display Active

14. Press the line switch off.
15. Connect the A15 Keyboard cable (W10) to the A12 Mother board.

NOTE

The keyboard cable (W10) can easily be connected wrong! After connecting the cable, verify that both rows of pins are connected.

16. Press the line switch on. The LEDs pass sequence should occur (it takes about 40s to complete) and A2 DS1 should be off. If the LEDs pass sequence does not occur, the probable cause of the failure is the A15 Keyboard system bus interface circuits (go to 8-15).
17. The soft keys should now be active and the display appear as shown in figure 7-3. Only the GLOBAL RAM and TEST KEYBD tests are valid. If the soft keys are not active or the display is defective, either the A8 Global RAM, A15 Keyboard, or A17 Display Interface is probably defective. If possible, press the keys as follows:

NOTE

If the display is blank or garbled, the soft key menus may be unreadable. The number of the soft key (S1 through S8 from top to bottom) for this procedure appears in parentheses after the soft key name.

| | | | |
|----------------------|---------------------------|---------------------------|--------------------------|
| SPCL FCTN | SERVIC TEST (S2) | TEST PROC (S3) | TEST KEYBD (S4) |
| | RETURN (S8) | TEST MEMORY (S2) | GLOBAL RAM (S1) |

If these tests pass, the A8 Global RAM (except for the display controller subblock) and the A15 Keyboard system bus interface circuits are probably working correctly. If a test fails, go to Section VIII.

18. The A17 Display Interface or the display controller subblock on the A8 Global RAM may be causing the failure (the self-tests do not verify these circuits). If the display does not appear as shown in figure 7-3, refer to paragraph 8-11 to test the display interface and display controller circuits.
19. Press the line switch off and replace the A9 FFT.
20. Press the line switch on. The LEDs pass sequence should occur and A2 DS1 should be off. If the LEDs pass sequence does not occur, go to part E. If the fault has not been found, continue with part D.

D. Perform steps 1 through 3 as follows for each of the remaining assemblies. Replace the assemblies in the following order:

- A6 Digital Filter Controller
- A7 FPP
- A1 Digital Source
- A4 Local Oscillator
- A31 Trigger
- A5 Digital Filter
- A34 ADC 2
- A35 Input 2
- A30 Analog Source
- A32 ADC 1
- A33 Input 1

1. Press the line switch off.
2. Replace the assembly.
3. Press the line switch on. The LEDs pass sequence should occur and A2 DS1 should be off. If the LEDs pass sequence does not occur, go to part **E**.

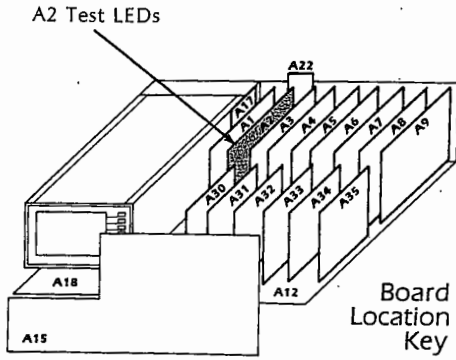
E. Power-Up Tests Code Table

After the power-up tests are completed, use table 7-4 to help determine the cause of the failure. (Refer to the beginning of this section for the description of the power-up test sequence). The table lists the tests in the order they are run. The A2 Test LEDs Hex code is listed on the vertical axis of the table. The assemblies and subblocks tested or used by the power-up tests are listed on the horizontal axis of the table.

There are two symbols used in table 7-4: **O** and **X**. When the symbol “**O**” is used in the table, the assembly or subblock is used in the test but is not a likely cause of the failure. When the symbol “**X**” is used in the table, the assembly or subblock is the probably the cause of the failure. No symbol means the assembly or subblock is not used in the test.

EXCEPTION NOTE

Shorts on the system bus, the global bus, an interrupt line, or the reset line, can cause false error codes. If an error code is caused by the last assembly inserted, it is probably the assembly defective.



Example:

LEDs ○○○●○○○

Binary 0001 1111

Hex 1 F

Chart Line #21

LED ON = 1

LED OFF = 0

| Binary | Hex |
|--------|-----|
| 0001 | 1 |
| 0010 | 2 |
| 0011 | 3 |
| 0100 | 4 |
| 0101 | 5 |
| 0110 | 6 |
| 0111 | 7 |
| 1000 | 8 |
| 1001 | 9 |
| 1010 | A |
| 1011 | B |
| 1100 | C |
| 1101 | D |
| 1110 | E |
| 1111 | F |

Hex Error Code to Chart Line #

| | |
|----------|----|
| 01 to 04 | 2 |
| 05 to 06 | 3 |
| 07 to 0B | 1 |
| 0C to 0F | 6 |
| 10 to 1C | 4 |
| 1D | 1 |
| 1E | 7 |
| 1F | 21 |
| 20 to 33 | 12 |
| 34 to 3F | 1 |
| 40 to 53 | 13 |
| 54 to 59 | 1 |
| 5A | 9 |
| 5B | 10 |
| 5C | 11 |
| 5D to 5F | 1 |
| 60 to 73 | 14 |
| 74 to 79 | 1 |
| 7A | 10 |
| 7B | 9 |
| 7C | 11 |
| 7D to 7F | 1 |
| 80 | 1 |
| 81 | 23 |
| 82 | 24 |
| 83 | 25 |
| 84 to 86 | 15 |
| 87 | 17 |
| 88 | 18 |
| 89 | 19 |
| 8A to 8C | 16 |
| 8D | 20 |
| 8E to 8F | 1 |
| 90 to 9F | 26 |
| A0 to AF | 27 |
| B0 | 1 |
| B1 | 8 |
| B2 to B4 | 1 |
| B5 | 22 |
| B6 | 30 |
| B7 | 31 |
| B8 to BF | 1 |
| C0 to CF | 5 |
| D0 to DF | 28 |
| E0 to EF | 29 |
| F0 to FF | 1 |

| Chart Line No. |
|----------------|
| 1 |
| 2 |
| 3 |
| 4 |
| 5 |
| 6 |

| |
|----|
| 7 |
| 8 |
| 9 |
| 10 |
| 11 |
| 12 |
| 13 |
| 14 |
| 15 |
| 16 |
| 17 |
| 18 |
| 19 |
| 20 |
| 21 |

| |
|----|
| 22 |
| 23 |
| 24 |
| 25 |
| 26 |
| 27 |
| 28 |
| 29 |
| 30 |
| 31 |

Table 7-4 Power-up Test Codes

* No info

001 X means the assembly or subblock is the most likely cause of the failure message.

001 O means the assembly or subblock is not the most likely cause of the failure message.

001 means the assembly or subblock is not the test.

These tests are run in order starting with the monitor ROM test. The error code is for the first test that fails. A pass code indicates a failure on the next test.

| Hex /Error Code | Test Description | Assembly/Subblock | | U100 System Processor | | | | Mother Board | | FFT System Interface | | Global RAM | | | | | |
|---|--|-------------------|-----|-----------------------|-----|----|----|--------------|----|----------------------|---|------------|----|----|---|----|----|
| | | A2 | A18 | 8 Mhz Clock | +5S | A2 | A2 | A2 | A2 | A12 | - | A3 | A3 | A9 | - | A8 | A8 |
| SYSTEM CPU TEST | | | | | | | | | | | | | | | | | |
| 00 | Initial Power Up | | | X | O | X | O | X | | | | | | | | | |
| 04 | Monitor ROM | | | O | O | X | O | O | | | | | | | | | |
| 08 | System Processor | | | O | O | X | O | O | | | | | | | | | |
| 1C | Monitor RAM Test Failure | | | O | O | O | O | X | | | | | | | | | |
| CF | Monitor RAM Address Failure | | | O | O | O | O | X | | | | | | | | | |
| 0F | Timer and Interrupt Failures | | | O | O | O | O | X | | | | | | | | | |
| PROGRAM ROM AND SYSTEM BUS TESTS | | | | | | | | | | | | | | | | | |
| 1E | Start Program ROM Check Sum | | | O | O | O | O | O | O | X | X | X | | | | | |
| B1 | Program ROM Installed ? | | | O | O | O | O | O | O | O | X | X | | | | | |
| 7A* | Program ROM failure, low byte | | | O | O | O | O | O | O | O | X | X | | | | | |
| 7B* | Program ROM failure, high byte | | | O | O | O | O | O | O | O | X | X | | | | | |
| 7C* | Program ROM failure, both bytes | | | O | O | O | O | O | O | O | X | X | | | | | |
| 33 | Program ROM, chip failure, high byte | | | O | O | O | O | O | O | O | X | X | | | | | |
| 53 | Program ROM, chip failure, low byte | | | O | O | O | O | O | O | O | X | X | | | | | |
| 73 | Program ROM, chip failure, both bytes | | | O | O | O | O | O | O | O | X | X | | | | | |
| 86 | Program ROM failure, System bus good | | | O | O | O | O | O | O | O | X | X | | | | | |
| 8C | Program ROM failure, System bus good | | | O | O | O | O | O | O | O | X | X | O | | | | |
| 87 | System bus failure, high byte | | | O | O | O | O | O | O | O | X | X | | | | | |
| 88 | System bus failure, low byte | | | O | O | O | O | O | O | O | X | X | | | | | |
| 89 | System bus failure, both bytes | | | O | O | O | O | O | O | O | X | X | | | | | |
| 1D | No ROM passes check sum, system bus good, Check system address bus | | | O | O | O | O | O | O | O | X | X | | | | | |
| F | Program ROM and System bus tests pass | | | O | O | O | O | O | O | O | O | O | | | | | |
| GLOBAL RAM TEST | | | | | | | | | | | | | | | | | |
| 5 | Starting Global RAM Test | | | O | O | O | O | O | O | O | O | O | | X | O | O | |
| 1 | Global RAM failure, both bytes | | | O | O | O | O | O | O | O | O | O | | O | X | X | |
| 2 | Global Ram failure, high byte | | | O | O | O | O | O | O | O | O | O | | O | X | X | |
| 3 | Global RAM failure, low byte | | | O | O | O | O | O | O | O | O | O | | O | X | X | |
| 9F | Global bus failure, bit "N" | | | O | O | O | O | O | O | O | O | O | | X | O | X | |
| AF | Global RAM address failure, bit "N", Check global address bus | | | O | O | O | O | O | O | O | O | O | | X | X | X | |
| DF | Global RAM failure, bit "N" | | | O | O | O | O | O | O | O | O | O | | O | X | X | |
| EF | Global RAM refresh failure, bit "N" | | | O | O | O | O | O | O | O | O | O | | O | X | X | |
| 3 | Executing high level power-up tests | | | O | O | O | O | O | O | O | O | O | | O | O | O | |
| 7 | Power-up tests finished | | | | | | | | | | | | | | | | |

ion about system bus

F. Global Bus Test

This test is used for power-up test code failures 90 to 9F. The 9"N" error code indicates a global bus line is defective. For example, if N=5, then a Hex 95 failure indicates the global bus line GD5 is defective.

1. Press the line switch off.
2. Remove the following assemblies:
 - A5 Digital Filter
 - A7 FPP
 - A8 Global RAM/Display
 - A9 FFT
 - A17 Display Interface
3. Place the A2 System CPU on the 03562A-66540 extender board.
4. Put jumpers A2 J8, A2 J12, A2 J13, and A2 J17 in test (T) position. This forces the system CPU to execute the Global RAM test.
5. Press the line switch on. The LEDs sequence should stop on Hex B5 for about 1.3 minutes and then display Hex AF.
6. If the pass/error code is still 9"N", start troubleshooting with the A2 System CPU (go to 8-6).
7. Perform steps (a) through (c) for each of the assemblies. Replace the assemblies in the following order:

- A8 Global RAM/Display
- A17 Display Interface
- A9 FFT
- A7 FPP
- A5 Digital Filter

(a) Press the line switch off.

(b) Replace the assembly.

(c) Press the line switch on. The LEDs sequence should read Hex B5 for about 1.3 minutes and then display Hex AF. If this sequence is not displayed, start troubleshooting with this assembly (go Section VIII).

8. Put jumpers A2 J8, A2 J12, A2 J13, and A2 J17 in normal (N) position.

G. If the fault has not been found, go to paragraph 7-10, "Control Line Test".

7-7 TEST ALL

Introduction

The Test All sequence thoroughly exercises the digital and the analog hardware in the instrument. This self-diagnostic actually does several types of measurements to determine what is operating correctly. When a fault is found the self-diagnostic exercises suspected circuits using digital signals generated internally, reading status registers, and using the internal analog source and calibrator. The Test All sequence then uses logic to determine the most likely failure based on the results of these measurements.

All failure messages are displayed in the Test Log (refer to 7-15 for test log description). If the Test All sequence does not isolate the defective assembly, the individual self-tests for the suspected assemblies can be done individually to help isolate the failure. Use table 7-6 as a reference when running any of the service tests. When a test passes the assemblies and subblocks exercised are most likely operating correctly.

The Test All feature does not isolate failures on the following assemblies:

- Core Assemblies
- A32 Trigger
- A15 Keyboard
- A18 Power Supply
- A12 Mother Board
- A17 Display Interface
- HP 1345A Display
- System and global control lines

If a keyboard related problem is suspected, go to 8-15 after performing TEST ALL. If the instrument does not respond when a key is pressed or the display is defective, go to paragraph 7-5, "Initial Conditions Test". The Test All diagnostic does not use or test the following circuits:

A22 HPIB (refer to 8-6 for HP-IB failures)

Trigger mode circuits (refer 7-11 for trigger failures)

Burst and noise source circuits (refer to 7-9 for burst and noise failures)

Follow the Test All procedure starting with part A to isolate the failure.

Test All Procedure

A. Start

1. Press the line switch on.

2. Press the HP 3562A keys as follows:

```

PRESET      ..... RESET (S8)

SPCL
FCTN      ..... SERVIC TEST ..... TEST
                                     RESULT ..... TEST
                                                         LOG
    
```

3. If the FPP, FFT, and Global RAM passed the power-up test, then these assemblies are probably operating correctly. If any of these assemblies failed the power-up test, refer to table 7-5.

4. Press the HP 3562A keys as follows:

```

SPCL
FCTN      ..... SERVIC
                                     TEST ..... TEST
                                                         ALL
    
```

If there are no failures, this test takes about two minutes to complete. If there is a failure, it may take three minutes to complete. The test log is displayed when the self-tests are completed.

5. Refer to figure 7-4 to verify the normal Test All result.

6. Use table 7-5 after running the Test All diagnostic.

| 3562 Service Tests | |
|-------------------------------|--------|
| Floating Point Processor | Passes |
| FFT Processor | Passes |
| Global Ram | Passes |
| Zoom Test | Passes |
| Calibration | Passes |
| DFA Filtered Chan Interrupt | Passes |
| DFA Unfiltered Chan Interrupt | Passes |

Figure 7-4 TEST ALL Passes

Table 7-5 TEST ALL Results

| <p>Test All Result Tests not listed may either pass or fail (don't cares). To use table, start with first line.</p> | <p>Go to Paragraph</p> |
|---|---|
| 1. Test All passes | 7-7, part B, "Test All Table" |
| 2. Test All does not complete self-tests (test log is not displayed) | 7-7, part C, "Test All Does Not Complete" |
| 3. FPP Fails | 8-10 A7 FPP |
| 4. FFT Fails | 8-13 A9 FFT |
| 5. Global RAM Fails | 8-11 A8, A17 Global RAM and Display Interface |
| 6. Keyboard Status Test Fails | 8-15 A15 Keyboard |
| 7. DFA Interrupt Fails | 7-8 Isolating Front End Failures |
| 8. DFA Unfiltered Chan Interrupt Fails | 7-8 Isolating Front End Failures |
| 9. Source Test Fails, Calibration Fails, Front End Passes | 7-9 Source Failures |
| 10. Calibration Fails, Front End Passes, Source Test Passes | 8-17 A30 Analog Source |
| 11. Calibration Fails, Front End Fails only on one channel, Source Test Passes | 7-8, part C, "A5, A6 Digital Filter Check" |
| 12. Source Test Fails, Front End Fails , Calibration Fails | 7-8 Isolating Front End Failures |

B. Test All Table

Use table 7-6 to help determine the failure after running the Test All diagnostic or any individual self-tests. The table lists the self-tests in the order the Test All diagnostic executes them. A pass message indicates the assemblies and subblocks tested are probably operating correctly. The pass/fail messages are listed on the vertical axis of the table. The assemblies and subblocks tested or used by the self-tests are listed on the horizontal axis of the table. (Refer to the introduction of paragraph 7-7 for the list of assemblies not tested by Test All.)

There are two symbols used in table 7-6: **O** and **X**. When the symbol "O" is used in the table, the assembly or subblock is used in the test but is not a likely cause of the failure. When the symbol "X" is used in the table, the assembly or subblock is probably the cause of the failure. No symbol means the assembly or subblock is not used in the test.

| <p>The symbol X means the assembly or subblock is the most likely cause of the failure message.</p> <p>The symbol O means the assembly or subblock is used in the circuit but is not the most likely cause of the failure message.</p> <p>No symbol means the assembly or subblock is not used in the test.</p> <p>Note: Press SELF TEST...SERVIC TEST...TEST ALL to run all of the tests. To run individual tests press the key listed under the "Press Key" column.</p> | | | Assembly / Subblock | | | | |
|---|------------------------------------|---------------|---------------------|-----------------|-----|----|----|
| | | | A2 | 8 MHz Clock +5S | A1B | A2 | A3 |
| Pass / Fail Messages | Description | Press Key | A2 | A1B | A2 | A3 | |
| Power-Up Test Codes | See Table 7-4 for Pass/Error Codes | A2 S1 (Reset) | O | O | O | O | |
| FFT "messages" | FFT Self-Tests | FFT FUNCTN | O | O | O | O | |
| FPP "messages" | FPP Self-Tests | FPP FUNCTN | O | O | O | O | |
| DFA Interrupt "messages" | DFA Interrupt Test | ----- | O | O | O | O | |
| DFA Counter "bit#" | DFA Local Bus Echo | LOCAL BUS | O | O | O | O | |
| DFA Local Bus "bit#" | DFA Local Bus Echo | LOCAL BUS | O | O | O | O | |
| Calibration "messages" | Self-Calibration | TEST ALL | O | O | O | O | |
| Channel 1 Zoom Signal | Zoom Test | ZOOM | O | O | O | O | |
| Channel 2 Zoom Signal | Zoom Test | ZOOM | O | O | O | O | |
| Channel 1 Zoom Noise | Zoom Test | ZOOM | O | O | O | O | |
| Channel 2 Zoom Noise | Zoom Test | ZOOM | O | O | O | O | |
| Source Distortion | Source Test | SOURCE FUNCTN | O | O | O | O | |
| Source Signal Level | Source Test | SOURCE FUNCTN | O | O | O | O | |
| Calibration Distortion | Source Test | SOURCE FUNCTN | O | O | O | O | |
| Calibration Signal Level | Source Test | SOURCE FUNCTN | O | O | O | O | |
| Channel 1 Operation | Front End Test | FR END FUNCTN | O | O | O | O | |
| Channel 2 Operation | Front End Test | FR END FUNCTN | O | O | O | O | |
| Channel 1 Distortion | Front End Test | FR END FUNCTN | O | O | O | O | |
| Channel 2 Distortion | Front End Test | FR END FUNCTN | O | O | O | O | |
| Digital Souce F/E Interface "bit#" | Digital Source Self Test | FR END INTFCE | O | O | O | O | |
| Digital Source Main Test "bit#" | Digital Source Self Test | SOURCE MAIN | O | O | O | O | |
| ADC Channel 1 "messages" | ADC Tests | DIGITAL TEST | O | O | O | O | |
| ADC Channel 2 "messages" | ADC Tests | DIGITAL TEST | O | O | O | O | |
| LO "messages" | LO Functional | LO FUNCTN | O | O | O | O | |
| DFA Functional Channel 1 | Zoom with Square Wave Test | DFA FUNCTN | O | O | O | O | |
| DFA Functional Channel 2 | Zoom with Square Wave Test | DFA FUNCTN | O | O | O | O | |
| DFA Channel 1 Real Filter | DFA Data Echo | FILTER TEST | O | O | O | O | |
| DFA Channel 1 Imaginary Filter | DFA Data Echo | FILTER TEST | O | O | O | O | |
| DFA Channel 2 Real Filter | DFA Data Echo | FILTER TEST | O | O | O | O | |
| DFA Channel 2 Imaginary Filter | DFA Data Echo | FILTER TEST | O | O | O | O | |
| DMA "messages" | DFA DMA Bus Echo | DMA BUS | O | O | O | O | |
| DFA Filter Bus 1 "bit#" | DFA Filter Bus Test | FILTER BUS | O | O | O | O | |
| DFA Filter Bus 2 "bit#" | DFA Filter Bus Test | FILTER BUS | O | O | O | O | |

Table 7-6 TEST ALL Messages

C. Test All Does Not Complete

Use this procedure when the test log is not displayed within 5 minutes after pressing TEST ALL.

1. Press the line switch off.
2. Remove the following assemblies:

A5 Digital Filter
 A7 FPP
 A9 FFT

3. Press the line switch on and the HP 3562A keys as follows:

```

SPCL
FCTN      ..... SERVIC
           TEST           ..... TEST
                               MEMORY ..... GLOBAL
                                           RAM
    
```

If test fails or the display does not appear as in figure 7-5, start troubleshooting with the A8 Global RAM (go to 8-11).

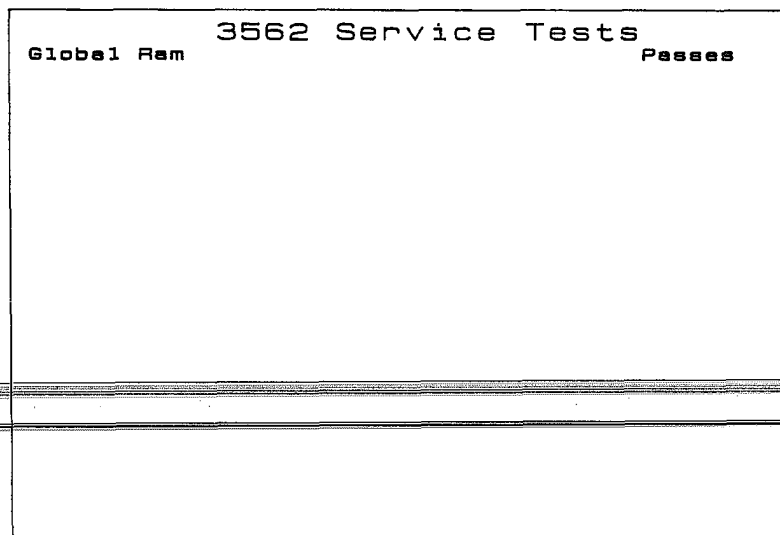


Figure 7-5 Global RAM Test Passes

4. Press the line switch off.
5. Replace the A7 FPP assembly.
6. Press the line switch on and the HP 3562A keys as follows:

SPCL
FCTN SERVIC
 TEST TEST
 PROC TEST
 FPP FPP
 FUNCTN

If this test fails, start troubleshooting with the A7 FPP (go to 8-10).

7. Press the line switch off.
8. Replace the A9 FFT assembly.
9. Press the line switch on and the HP 3562A keys as follows:

SPCL
FCTN SERVIC
 TEST TEST
 PROC TEST
 FFT FFT
 FUNCTN

If this test fails, start troubleshooting with the A9 FFT (go to 8-13).

10. Press the line switch off.
11. Replace the A5 DGTL FLTR assembly.
12. Press the line switch on and the HP 3562A keys as follows:

SPCL
FCTN SERVIC
 TEST TEST
 PROC TEST
 DFA FILTER
 TEST

If this test fails, start troubleshooting with the A5 DGTL FLTR (go to 8-9).

13. If the display is normal and the fault has not been found, go to paragraph 7-8, "Isolating Front End Failures".
14. If the display is defective and the fault has not been found, go to paragraph 7-10, "Control Line Test".

7-8 ISOLATING FRONT END FAILURES

This procedure assumes the core assemblies are operating correctly and the Test All procedure was done. The self-diagnostic message 'Front End Fails' can be caused by the following assemblies:

A1 Digital Source
 A4 Local Oscillator
 A5 Digital Filter
 A6 Digital Filter Controller
 A30 Analog source
 A32 Analog Digital Converter Channel 1
 A33 Input Channel 1
 A34 Analog Digital Converter Channel 2
 A35 Input Channel 2

NOTE

For some failures it takes up to three minutes to complete a test. If a test takes more than five minutes to terminate (the test log is displayed), the test has failed.

A. Signal Check

1. Press the line switch off.
2. Remove the top cover.
3. Press the line switch on.
4. After the power-up tests are completed, use a scope to verify the signals listed in table 7-7. If all the signals are operating correctly, go to step 5.

3562A TOP VIEW,
COVER REMOVED.

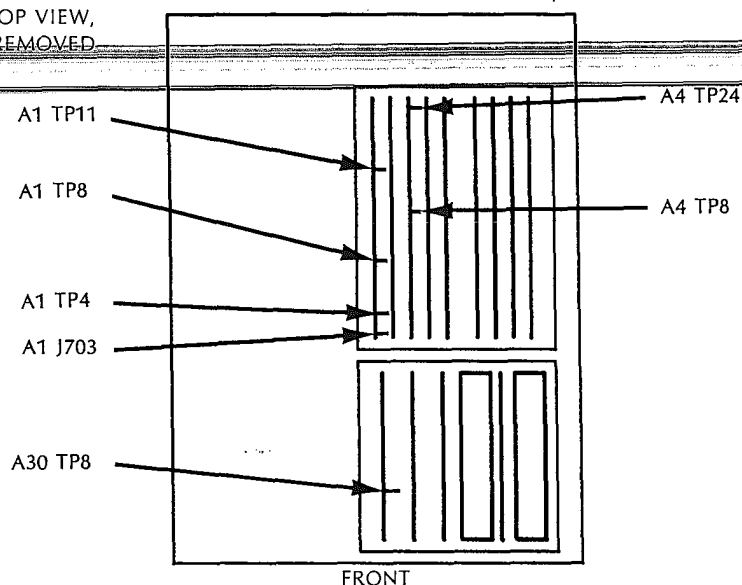


Table 7-7 Front End Signal Check

| Test Location | Signal Name | Waveform Number | Probable Cause of Failure | Go To |
|--|-------------|-----------------|--|----------------|
| A1 TP4 | 10.24 MHz | #2 | A31 Trigger | 8-18 |
| A1 TP8 | SAMP | #5 | A34 ADC 2 | 8-19 |
| A1 J703-1 | DREQL | #5 | A5 Digital Filter A6 D FLTR CONT | 8-9 |
| A4 TP8 | SYNC2 | #6 | A5 Digital Filter A6 D FLTR CONT A4 LO | 7-8, part G |
| A4 TP24 | COS | #6 | A4 LO | 8-8 |
| Refer to step 5 for key presses to view CNTCLK. | | | | |
| A1 TP11 | CNTCLK | #4 | A1 Digital Source | 8-5 |
| Press A2 S1 to view the STIM@ waveform (STIM@ is disabled when calibration is done). | | | | |
| A30 TP8 | STIM@ | #8 | A30 Analog Source | 8-17 |

5. Press the HP 3562A keys as follows:

```

SPCL FCTN . . . . . SERVIC
                TEST . . . . . LOOP
                                ON
                . . . . . TEST
                                SOURCE . . . . . FR END
                                                INTFCE
    
```

After Viewing the waveform, press A2 S1 (reset switch on A2 CPU)

B. A4 LO Check

1. Press the HP 3562A keys as follows:

```

SPCL
FCTN . . . . . SERVIC
                TEST . . . . . TEST
                                SOURCE . . . . . LO
                                                FUNCTN
    
```

2. If this test fails, start troubleshooting with the A4 Local Oscillator (go to 8-8).

3. If this test passes, the A4 Local Oscillator is probably working correctly.

C. A5, A6 Digital Filter Check

1. Press the line switch off.
2. Pull the following assemblies up in their card nests:

A32 ADC 1
 A33 INPUT 1
 A34 ADC 2
 A35 INPUT

3. Press the line switch on.
4. Press the HP 3562A keys as follows:

SPCL
FCTN SERVIC
 TEST TEST
 PROC
 TEST DFA
 DFA FUNCTN

5. If this test fails, start troubleshooting with the A5 Digital Filter and A6 Digital Filter Controller (go to 8-9).
6. If this test passes, the A5 Digital Filter and A6 Digital Filter Controller assemblies are probably operating correctly. Replace all assemblies in their card nests.
7. Press the HP 3562A keys as follows:

SPCL
FCTN SERVIC
 TEST TEST
 INPUT ADC DIGITAL
 TEST

-
8. If the ADC Gate Array test passes, the data path from the ADC to the digital filter is probably functioning correctly.
 9. If only one channel is failing and the DFA Functional test (DFA FUNCTN) passed for both channels, go to part F.

D. A1 Digital Source Check

1. Press the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST  . . . . . TEST
                              SOURCE . . . . . SOURCE
                                      MAIN
    
```

2. When this test is finished press the keys as follows:

```

. . . . . FR END
          INTFCE
    
```

3. If the Source Main test or the Digital Source F/E Interface test fails, start troubleshooting with the A1 Digital Source (go to 8-5).
4. If these tests pass, the A1 Digital Source interface circuits to the A33/A35 Inputs, the A32/A34 ADCs, and the A30 Analog Source are probably operating correctly (see exception note). If the digital source check passes, go to part E.

EXCEPTION NOTE

If the following is occurring:

a. Result of TEST ALL is:

| | |
|-------------------------------|--------------|
| Floating Point Processor | Passes |
| FFT Processor | Passes |
| Digital Source F/E Interface | Passes |
| Digital Source Main Test | Passes |
| Digital Source Counters | Passes |
| Global RAM | Passes |
| ADC Channel 1 Gate Array | Fails |
| ADC Channel 2 Gate Array | Fails |
| Source Test | Fails |
| Chan 1 Input Operation | Fails |
| Chan 2 Input Operation | Fails |
| Calibration | Fails |
| LO Functional Test | Passes |
| DFA Filtered Chan Interrupt | Passes |
| DFA Unfiltered Chan Interrupt | Passes |

b. The signals in table 7-7 are correct.

The probable cause of the failure is the A1 Digital Source shift registers (A1 U206, A1 U207). There is one failure mode of these shift registers that is not detected by the self-test.

E. Output Sine Check

1. Connect a scope to the source output on the front panel. Set the scope as follows:

CH1 V/Div 2 V/Div
Coupling dc
Time/Div 500 μ s/Div
Trigger CH1

2. Press the HP 3562A keys as follows:

SOURCE SOURCE
 LEVEL 5 V

 FIXED
 SINE 1 kHz

3. Refer to figure 7-6 to verify the correct result.

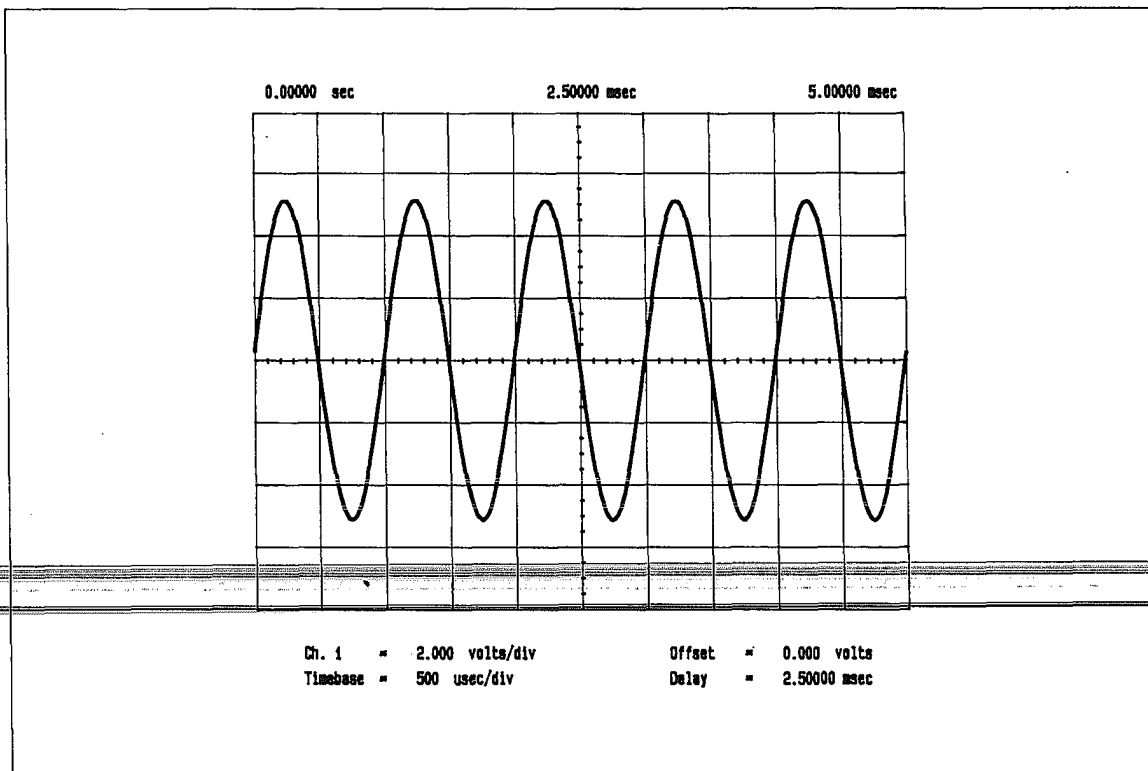


Figure 7-6 Sine Wave

4. If this test passes, the A4 Local Oscillator, the A1 Digital Source, and the A30 Analog Source are probably operating correctly, (except for chirp, noise, and trigger circuits).

F. Input and ADC Failures

This procedure isolates failures between the following assemblies:

- A32 ADC1
- A33 INPUT 1
- A34 ADC 2
- A35 INPUT 2

The HP 3562A has two sets of identical assemblies: A32 is identical to A34 and A33 is identical to A35. This procedure interchanges these assemblies to aid in troubleshooting.

NOTE

*A failure on the A34 ADC2 may cause **both** channels to fail.*

1. Press the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST  . . . . . TEST
                              INPUT  . . . . . FR END
                                                FUNCTN
    
```

2. If this test passes the A32/34 ADC and the A33/A35 Input assemblies are probably operating correctly.
3. Press the line switch off.
4. Exchange A32 ADC1 with A32 ADC2.
5. Press the line switch on and repeat step 1.
6. If the same channel fails as failed before the exchange, start troubleshooting with the input assembly for that channel (go to 8-20).

7. If the other channel now fails, start troubleshooting with the ADC assembly for that channel (go to 8-19).

8. If both channels failed before the exchange and also after the exchange, the A33, A35 Input and A32, A34 ADC assemblies are probably not the cause of the failure. Go to paragraph 7-10, "Control Line Test".

G. SYNC2 Test

The A4 Local Oscillator will function without the A5 Digital Filter if the SYNC2 signal is activated. Perform this procedure to determine if the A5 Digital Filter is the cause of the failure.

1. Press the line switch off.
2. Remove the A5 Digital Filter.

3. Put the 03562-66540 extender board in the A5 Digital Filter's card nest.
4. Connect a square wave to pin 16 on the extender board as follows:

```

Function .....Square Wave
Frequency .....250 kHz
Amplitude.....5 Vp-p
dc Offset.....2.5 V
    
```

5. Press the line switch on and press the HP 3562A keys as follows:

```

SOURCE ..... SOURCE
          LEVEL ..... 5 V

          ..... FIXED
          SINE ..... 1 kHz
    
```

6. Use a scope to verify COS at A4 TP24, Waveform #7. If this signal is not correct, start troubleshooting with the A4 LO (go to 8-8).
7. Connect the scope to the source output on the front panel. Set the scope as follows:

```

CH1 V/Div   2 V/Div
Coupling    dc
Time/Div    500 ,s/Div
Trigger     CH1
    
```

8. Refer to figure 7-7 to verify the correct result.

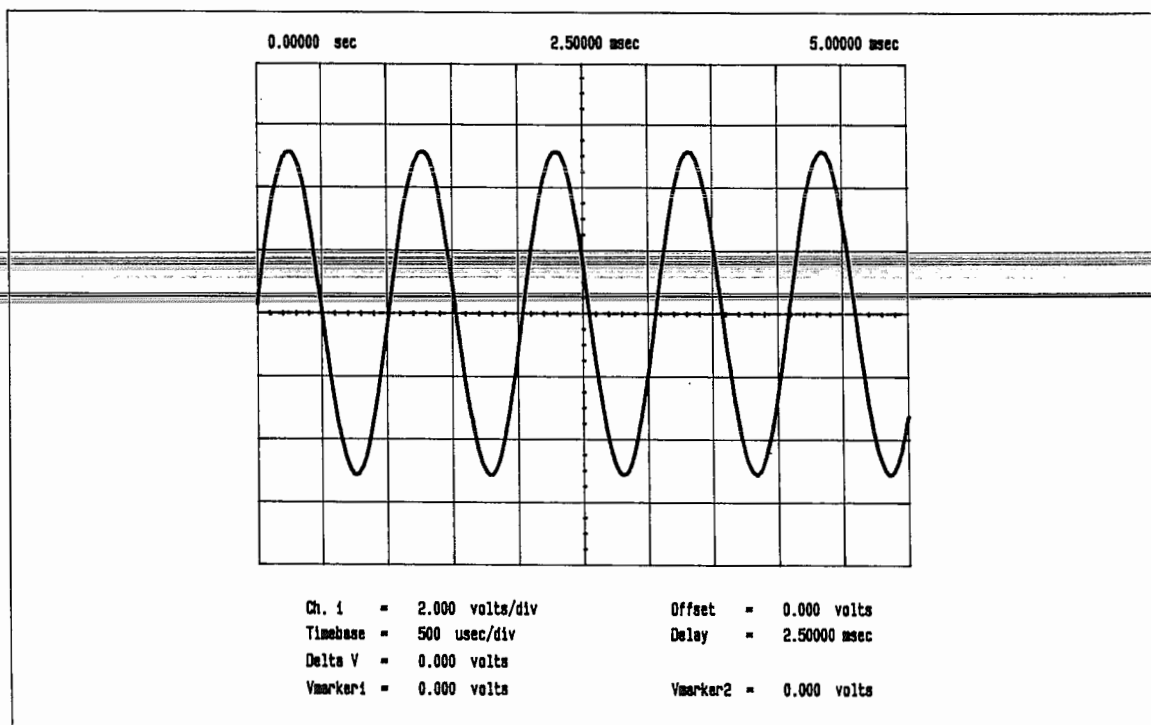


Figure 7-7 SYNC 2 Test Sine Wave

9. If this test fails, start troubleshooting with the A4 Local Oscillator (go to 8-8).
10. If this test passes, the A4 Local Oscillator, the A1 Digital Source, and the A30 Analog Source are probably operating correctly, (except for chirp, noise, and trigger circuits). If this test passes, start troubleshooting with the A5 Digital Filter and A6 Digital Filter Controller assemblies (go to 8-9).

NOTE

If the cause of the failure has not been found, go to paragraph 7-10, "Control Line Test".

7-9 SOURCE FAILURES

Source output failures can be caused by the A1 Digital Source, the A4 Local Oscillator, or the A30 Analog Source. Follow the Source Failures procedure starting with part A to isolate the defective assembly.

A. Start

1. If all the source functions are operating except the random noise and burst random, start troubleshooting with the A1 Digital Source (go to 8-5).
2. If all the source functions are operating except burst random, periodic chirp, or burst chirp, go to part D.
3. Press the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST  . . . . . TEST
                               SOURCE . . . . . LO
                                               FUNCTN
    
```

4. If this test fails, start troubleshooting with the A4 Local Oscillator (go to 8-8).

5. If this test passes, the A4 Local Oscillator is probably working correctly.

6. Press the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST  . . . . . TEST
                               SOURCE . . . . . SOURCE
                                               MAIN
    
```

7. When this test is finished press the keys as follows:

```

. . . . . FR END
          INTFCE
    
```

- 8. If the Source Main test or the Digital Source F/E Interface test fails, start troubleshooting with the A1 Digital Source (go to 8-5).
- 9. If these tests pass, the A1 Digital Source is probably working correctly.

B. Use a logic probe or scope to verify the signals in table 7-8 are toggling between TTL level high and TTL level low. If any of the values are incorrect, go to 8-8.

Table 7-8 Source Data

| Test Location | Signal | In/Out | Waveform Number | Probable Cause of Failure |
|---------------|--------|--------|-----------------|---------------------------|
| A4 TP24 | COS | A4 Out | #6 | A4 Local Oscillator |
| A4 TP16 | NDAT | A4 Out | #9 | A4 Local Oscillator |
| A4 TP17 | NLD | A4 Out | #11 | A4 Local Oscillator |
| A4 TP14 | NDCK | A4 Out | #11 | A4 Local Oscillator |

C. If part B passed, start troubleshooting with the A30 Analog Source (go to 8-17).

D. Burst Failures

- 1. Press the line switch off.
- 2. Place the A1 Digital Source on the 03562-66540 extender board. Connect the source output to the channel 1 input.
- 3. Press the line switch on.
- 4. Press the HP 3562A keys as follows:

```

SOURCE ..... SOURCE
                LEVEL ..... 5 V
-----
                BURST
                CHIRP

MEAS
DISP ..... FILTRD
                INPUT ..... TIME
                        REC 1
    
```

- 5. Refer to figure 7-8 to verify a normal burst chirp.

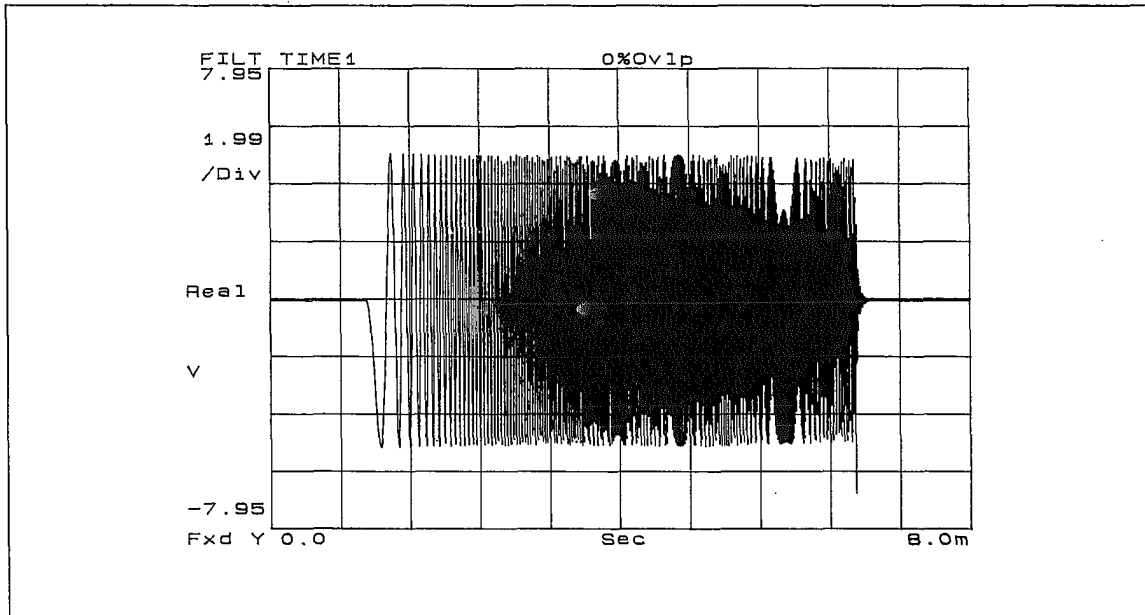


Figure 7-8 Burst Chirp

- Use a scope and logic probe to verify the signals in table 7-9 are toggling between TTL level high and TTL level low. If any of the values are incorrect, go to Section VIII.

Table 7-9 Burst Mode Signals

| Test Location | Signal | In/Out | Waveform Number | Probable Cause of Failure |
|---------------|---------|--------|-----------------|---------------------------|
| A1 J701-3 | NCLK | A1 Out | #13 | A1 Digital Source |
| A1 J701-1 | NSYNC | A4 Out | #13 | A4 Local Oscillator |
| A1 J1-1 | DACDAT | A1 Out | — | A1 Digital Source |
| A1 J1-5 | BURSTEN | A1 Out | — | A1 Digital Source |

NOTE

If NCLK fails, NSYNC also fails. Start troubleshooting with the A1 Digital Source (go to 8-5).

- If the signals in table 7-9 are correct, start troubleshooting with the A30 Analog Source (go to 8-17).

7-10 CONTROL LINE TEST

Control line failures can cause false error codes and multiple failure messages. This procedure determines if a control line is defective.

A. Perform steps 1 through 7:

1. Press the line switch off.
2. Place the A2 System CPU on the 03562-66540 extender board.
3. Press the line switch on.
4. Verify the RESETL line is a TTL level high at test point A2 U604-16.
5. After the power-up sequence is completed, use a logic probe to verify the signals in table 7-10 are toggling between TTL level high and TTL level low.
6. If a line is TTL level stays low, go to part **B**.
7. Use table 7-10 to determine which assembly is defective.

Table 7-10 Control Lines Set #1

| Test Location | Signal | In/Out | Probable Causes of Failure |
|---------------------------------|-----------------|-------------------|---|
| A2 U500-1 | IRQT4L | A9 Out | A2 CPU, A9 FFT |
| A2 U500-2 | IRQT5L | A6 Out | A2 CPU, A6 D FLTR CONT |
| A2 U500-3 | IRQT6L | A8 Out | A2 CPU, A8 RAM |
| A2 U500-13 | IRQT3L | A7 Out | A2 CPU, A7 FPP |
| Press any key to toggle KYBRDL. | | | |
| A2 U604-3 | KYBRDL | A2 Out | A2 CPU, A15 KEYBD |
| A2 U604-5 | ASL | A2 Out | Any assembly on the system bus: A2 CPU A1 DGTL SCE A3 ROM A4 LO |
| A2 U604-7 | WRITEL | A2 Out | |
| A2 U604-9 | UDSL | A2 Out | |
| A2 U604-12 | LDSL | A2 Out | |
| A2 U604-14 | VIOL | A2 Out | A6 D FLTR CONT A7 FPP A8 RAM/DSPL A9 FPP A15 KEYBD |
| A2 U508-4 | DTACKL | A2 In | |
| A2 P1-11 | ENBLL | A2 Out | A2 CPU, A1 DGTL SCE, A3 ROM, A4 LO |
| A2 U604-18 | VMAL | A2 Out | A2 CPU, A4 LO |
| A2 U508-2 | VPAL | A4 Out | A2 CPU, A4 LO |
| A2 U508-5 | MR68L | A2 Out | A2 CPU, A8 RAM |

B. Perform steps 1 through 6 for each of the following assemblies:

- A1 Digital Source
- A3 Program ROM
- A6 Digital Filter Controller (also remove the A5 Digital filter)
- A7 FPP
- A8 Global RAM (MR68L should remain low with the RAM removed)
- A9 FFT
- A15 Keyboard (disconnect cable W10 from the A12 Mother Board)

1. Press the line switch off.
2. Remove the assembly.
3. Press the line switch on.
4. If the failing control line in table 7-10 is now toggling or TTL level high, start troubleshooting with this assembly (go to Section VIII).
5. Press the line switch off.
6. Replace the assembly.

C. Perform steps 1 through 6 as follows:

1. Press the line switch off.
2. Replace the A2 System CPU in its card nest. Place the A8 Global RAM on the 03562-66540 extender board.
3. Press the line switch on.
4. After the power-up sequence is completed, use a logic probe to verify the signals in table 7-11 are toggling between TTL level high and TTL level low.
5. If a line is TTL level stays low, go to part D.
6. Use table 7-11 to determine which assembly is defective.

Table 7-11 Control Lines Set #2

| Test Location | Signal | In/Out | Probable Causes of Failure |
|---------------|---------|---------|---|
| A8 U306-8 | GDSL | A8 Out | Any assembly on the global bus: A2 CPU, A5 DGTL FLTR A7 FPP, A8 RAM A9 FFT, A17 DSPL |
| A8 U608-11 | GR/GWL | A8 Out | |
| A8 U608-12 | RFDL | A17 Out | A8 RAM, A17 DSPL |
| A8 U608-14 | MRFPPPL | A7 Out | A8 RAM, A7 FPP |
| A8 U608-16 | MRDF2L | A5 Out | A8 RAM, A5 DGTL FLTR |
| A8 U608-17 | MRDF1L | A5 Out | A8 RAM, A5 DGTL FLTR |
| A8 U608-18 | MRFFTL | A9 Out | A8 RAM, A9 FFT |
| A8 U509-7 | MGDF2L | A8 Out | A8 RAM, A5 DGTL FLTR |
| A8 U509-12 | MGFFTL | A8 Out | A8 RAM, A9 FFT |
| A8 U509-14 | MGDF1L | A8 Out | A8 RAM, A5 DGTL FLTR |
| A8 U509-16 | MGFPPL | A8 Out | A8 RAM, A7 FPP |
| A8 U301-8 | B2GDSL | A8 Out | A8 RAM, A17 DSPL |
| A8 U406-8 | DAVL | A8 Out | A8 RAM, A17 DSPL |

D. Perform steps 1 through 6 for each of the following assemblies:

- A2 System CPU
- A5 Digital Filter
- A7 FPP
- ~~A9 FFT~~
- ~~A17 Display Interface~~

1. Press the line switch off.
2. Remove the assembly.
3. Press the line switch on.
4. If the failing control line in table 7-11 is now toggling or TTL level high, start troubleshooting with this assembly (go to Section VIII).
5. Press the line switch off.
6. Replace the assembly.

E. Perform steps 1 through 5 as follows:

1. Press the line switch off.
2. Replace the A8 Global RAM in its card nest. Place the A6 Digital Filter Controller on the 03562-66540 extender board.
3. Press the line switch on.
4. After the power-up sequence is completed, use a logic probe to verify the signals in table 7-12 are toggling between TTL level high and TTL level low.

Table 7-12 Control Lines Set #3

| Test Location | Signal | In/Out |
|---------------|---------|--------|
| A6 U304-6 | BLDSL | A6 Out |
| A6 U304-7 | BWRITEL | A6 Out |
| A6 U304-9 | BUDSL | A6 Out |

5. If any of the lines are not toggling, start troubleshooting with the A6 Digital Filter Controller (go to 8-9).
6. Replace the A6 Digital Filter Controller in its card nest.

7-11 ISOLATING TRIGGER FAILURES

This procedure assumes the instrument operates correctly in the free run mode, but does not operate correctly in the trigger mode. Follow this procedure starting with part A to isolate the defective assembly.

A. Start

1. If the trigger operates correctly except in external (EXT) trigger mode, start troubleshooting with the A31 Trigger assembly (go to 8-18).

2. Press the HP 3562A keys as follows:

```

SPCL
FCTN  ..... SERVIC
                TEST  ..... TEST
                                ALL
    
```

3. If any self-tests fail, go to paragraph 7-7.

Table 7-11 Control Lines Set #2

| Test Location | Signal | In/Out | Probable Causes of Failure |
|---------------|--------|---------|---|
| A8 U306-8 | GDSL | A8 Out | Any assembly on the global bus: A2 CPU, A5 DGTL FLTR A7 FPP, A8 RAM A9 FFT, A17 DSPL |
| A8 U608-11 | GR/GWL | A8 Out | |
| A8 U608-12 | RFDL | A17 Out | A8 RAM, A17 DSPL |
| A8 U608-14 | MRFPPL | A7 Out | A8 RAM, A7 FPP |
| A8 U608-16 | MRDF2L | A5 Out | A8 RAM, A5 DGTL FLTR |
| A8 U608-17 | MRDF1L | A5 Out | A8 RAM, A5 DGTL FLTR |
| A8 U608-18 | MRFFTL | A9 Out | A8 RAM, A9 FFT |
| A8 U509-7 | MGDF2L | A8 Out | A8 RAM, A5 DGTL FLTR |
| A8 U509-12 | MGFFTL | A8 Out | A8 RAM, A9 FFT |
| A8 U509-14 | MGDF1L | A8 Out | A8 RAM, A5 DGTL FLTR |
| A8 U509-16 | MGFPPL | A8 Out | A8 RAM, A7 FPP |
| A8 U301-8 | B2GDSL | A8 Out | A8 RAM, A17 DSPL |
| A8 U406-8 | DAVL | A8 Out | A8 RAM, A17 DSPL |

D. Perform steps 1 through 6 for each of the following assemblies:

- A2 System CPU
- A5 Digital Filter
- A7 FPP
- ~~A9 FFT~~
- A17 Display Interface

1. Press the line switch off.
2. Remove the assembly.
3. Press the line switch on.
4. If the failing control line in table 7-11 is now toggling or TTL level high, start troubleshooting with this assembly (go to Section VIII).
5. Press the line switch off.
6. Replace the assembly.

E. Perform steps 1 through 5 as follows:

1. Press the line switch off.
2. Replace the A8 Global RAM in its card nest. Place the A6 Digital Filter Controller on the 03562-66540 extender board.
3. Press the line switch on.
4. After the power-up sequence is completed, use a logic probe to verify the signals in table 7-12 are toggling between TTL level high and TTL level low.

Table 7-12 Control Lines Set #3

| Test Location | Signal | In/Out |
|---------------|---------|--------|
| A6 U304-6 | BLDSL | A6 Out |
| A6 U304-7 | BWRITEL | A6 Out |
| A6 U304-9 | BUDSL | A6 Out |

5. If any of the lines are not toggling, start troubleshooting with the A6 Digital Filter Controller (go to 8-9).
6. Replace the A6 Digital Filter Controller in its card nest.

7-11 ISOLATING TRIGGER FAILURES

This procedure assumes the instrument operates correctly in the free run mode, but does not operate correctly in the trigger mode. Follow this procedure starting with part A to isolate the defective assembly.

A. Start

~~1. If the trigger operates correctly except in external (EXT) trigger mode, start troubleshooting with the A31 Trigger assembly (go to 8-10).~~

2. Press the HP 3562A keys as follows:

```

SPCL
FCTN  .....  SERVIC
                TEST  .....  TEST
                                ALL
    
```

3. If any self-tests fail, go to paragraph 7-7.

4. Press the HP 3562A keys as follows:

```

SPCL
FCTN  . . . . . SERVIC
          TEST  . . . . . TEST
                               SOURCE . . . . . SOURCE
                                                MAIN
    
```

5. When this test is finished press the keys as follows:

```

          . . . . . FR END
                    INTFCE
    
```

6. If the Source Main test or the Digital Source F/E Interface test fails, start troubleshooting with the A1 Digital Source (go to 8-5).

7. If the trigger operates correctly except in remote HP-IB trigger mode and the A1 Digital Source self-tests passed, start troubleshooting with the A2 System CPU (go to 8-6).

B. Use a BNC Tee to connect the front panel source output to channel 1 and channel 2.

Press the HP 3562A keys as follows:

```

SOURCE . . . . . SOURCE
          LEVEL . . . . . 5 V

          . . . . . FIXED
          SINE  . . . . . 125 Hz
    
```

```

SELECT
TRIG  . . . . . CHAN 1
          INPUT
    
```

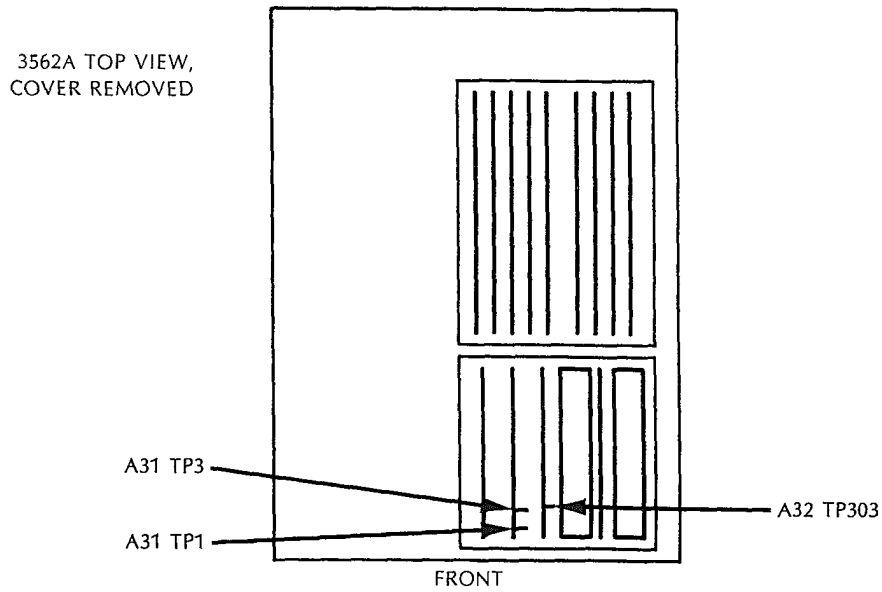
```

MEAS
DISP . . . . . FILTRD
          INPUT . . . . . TIME
                               REC 1
    
```

```

SCALE . . . . . Y FIXD
          SCALE . . . . . -7, 7 V
    
```

Refer to figure 7-9 to verify the correct result.



D. Use a scope to verify the signals TRIG IN and TRIGRO are operating correctly as shown in waveform -14 (refer to 7-13). If these signals are correct go to part G.

E. Perform steps 1 through 5 as follows:

1. Press the line switch off.
2. Put A32 ADC 1 on the 03562-66541 extender board.
3. Press the line switch on.
4. Repeat part **B**.
5. Use a scope to verify the signals in table 7-13 are operating correctly.

Table 7-13 Trigger Signal Check #1

| Test Location | Signal | In/Out | Waveform Number | Probable Cause of Failure |
|---------------|--------|---------|-----------------|---------------------------|
| A32 TP303 | TRIG1@ | A32 Out | #15 | A32 ADC 1 (go to 8-19) |
| A31 TP3 | TRIGRO | A31 Out | #15 | A31 Trigger (go to 8-18) |

F. Perform steps 1 through 5 as follows:

1. Press the line switch off.
2. Put A32 ADC 2 on the 03562-66541 extender board.
3. Press the line switch on.
4. Repeat part C.
5. Use a scope to verify the signals in table 7-14 are operating correctly.

Table 7-14 Trigger Signal Check #2

| Test Location | Signal | In/Out | Waveform Number | Probable Cause of Failure |
|---------------|--------|---------|-----------------|---------------------------|
| A34 TP303 | TRIG2@ | A34 Out | #16 | A34 ADC 2 (go to 8-19) |
| A31 TP3 | TRIGRO | A31 Out | #16 | A31 Trigger (go to 8-18) |

G. Perform steps 1 through 4 as follows:

1. Press the line switch off.
2. Put A30 Analog Source on the 03562-66541 extender board.
3. Press the line switch on.
4. Use a scope to verify the signals in table 7-15 are operating correctly. Press A2 S1 (reset switch on A2 CPU) to view the STIM@ and CALTRIG waveforms (these signals are disabled when calibration is finished).

Table 7-15 Trigger Signal Check #3

| Test Location | Signal | In/Out | Waveform Number | Probable Cause of Failure |
|--------------------------------|---------|---------|-----------------|---------------------------|
| Press A2 S1 to view waveforms. | | | | |
| A30 TP8 | STIM@ | A30 Out | #17 | A30 ANLG SCE (go to 8-17) |
| A30 J30-19 | CALTRIG | A30 Out | #17 | A30 ANLG SCE (go to 8-17) |

H. Perform the following steps:

1. Press the line switch off.
2. Put the A1 Digital Source on the 03562-66540 extender board.
3. Press the line switch on.

4. Repeat part B.
5. Use a logic probe or scope to verify the signals in table 7-16 are toggling between TTL level high and TTL level low.

Table 7-16 Trigger Signal Check #4

| Test Location | Signal Name | In/Out |
|---------------|-------------|--------|
| A1 TP9 | BFST | A1 Out |
| A1 J1-83 | ARML | A6 Out |

6. Press the PAUSE/CONT key. ARML should now remain at TTL level high.
7. If ARML and BFST are operating correctly, start troubleshooting with the A6 Digital Filter Controller (go to 8-9).
8. Connect A1 TP12 to A1 J705-2.
9. Repeat part B.
10. If the instrument now triggers (the waveform may move around on the display), start troubleshooting with the A6 Digital Filter Controller (go to 8-9).
11. If the instrument still does not trigger, start troubleshooting with the A1 Digital Source (go to 8-5).

7-12 LOOP MODE AND INTERMITTENT FAILURES

Loop mode is used for some signature analysis tests and to find intermittent failures. Many intermittent failures can be isolated by running the self-tests in this mode. When the loop mode is activated, the instrument continually repeats a test until power is cycled, the loop mode is shut off, or a failure is found. Most of the self-tests can be run in loop mode.

~~Run one of the following self-tests in loop mode to help isolate intermittent failures:~~

- TEST ALL
- HP-IB DIAG
- DFA FUNCTN
- FILTER TEST
- FFT FUNCTN
- FPP FUNCTN
- GLOBAL RAM
- PROG ROM
- SOURCE FUNCTN
- LO FUNCTN
- FR END FUNCTN
- DIGITAL TEST

Use paragraph 7-14 for the location of the service test keys.

To turn the loop mode on press the following keys:

SPCL
FCTN **SERVIC**
TEST **LOOP**
ON

Press the keys to start a self-test. Failures of a test are entered in the test log, the self-test stops, and the test log is displayed.

To turn the loop mode off press A2 S1 (reset switch on A2 CPU) or press the keys as follows:

RETURN **LOOP**
OFF

Troubleshooting Hints

1. Common causes of intermittent failures are:

- Cold solder joints
- Loose cables
- ICs loose in sockets
- Loose screws on power supply
- An assembly partially out of its card nest

2. An intermittent failure in the instrument can be caused by an assembly's bottom connector that attaches the assembly to the A12 Mother Board. Check for loose pins on the connector.
 3. If the instrument intermittently fails to power up, the most likely cause is the power supply control circuits (go to 8-16).
 4. Intermittent keyboard failures can be caused by the ribbon cable (W10) between the A15 Keyboard and A12 Mother Board.
-
-

7-13 WAVEFORMS

Use these waveforms to verify operation at various test points in the instrument. All oscilloscope measurements are taken using a 10:1 probe. Notes unique to a measurement are written next to the waveform.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury.

Table 7-17 Instrument Waveforms

| All jumpers should be in normal position Probe 10:1 | | |
|---|--------------------------------|---------------------------------------|
| Setup | Important Parameters | Waveform |
| <p>20.48 MHz</p> <p>Connect CH1 to A31 TP10</p> <p>Oscilloscope:</p> <p>CH1 V/Div 100 mV/Div</p> <p>CH1 Coupling dc</p> <p>Time/Div 20 ns/Div</p> <p>Trigger CH1</p> | <p>Time</p> <p>Pulse shape</p> | <p style="text-align: center;">#1</p> |
| <p>10.24 MHz</p> <p>Connect CH1 to A1 TP4</p> <p>Oscilloscope:</p> <p>CH1 V/Div 100 mV/Div</p> <p>CH1 Coupling dc</p> <p>Time/Div 50 ns/Div</p> <p>Trigger CH1</p> | <p>Time</p> <p>Pulse shape</p> | <p style="text-align: center;">#2</p> |

Table 7-17 Instrument Waveforms cont.

| <p><i>All jumpers should be in normal position Probe 10:1</i></p> | | |
|--|--------------------------------|----------|
| Setup | Important Parameters | Waveform |
| <p>8 MHz</p> <p>Connect CH1 to A2 TP5</p> <p>Oscilloscope:</p> <p>Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH1 Coupling dc</p> <p>Time/Div 50 ns/Div Trigger CH1</p> | <p>Time</p> <p>Pulse shape</p> | |
| <p>Press the keys as follows to view CNTCLK:</p> <p>SPCL FCTN SERVIC TEST LOOP ON</p> <p>. TEST SOURCE FR END INTFCE</p> | | |
| <p>CNTCLK</p> <p>Connect CH1 to A1 TP11</p> <p>Oscilloscope:</p> <p>Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH1 Coupling dc</p> <p>Time/Div 10 μs/Div Trigger CH1</p> | <p>Time</p> | |
| <p>Press A2 S1 (reset switch on A2 CPU) after viewing waveform.</p> | | |

Table 7-17 Instrument Waveforms cont.

| All jumpers should be in normal position Probe 10:1 | | |
|---|--|-----------|
| Setup | Important Parameters | Waveform |
| <p>SAMP and DREQ</p> <p>Connect CH1 to A1 TP8 Connect CH2 to A1 J703-1</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc</p> <p>Time/Div 1 μs/Div Trigger CH1</p> | <p>Time relationship</p> | <p>#5</p> |
| <p>SYNC2 and COS</p> <p>Connect CH1 to A4 TP8 Connect CH2 to A4 TP24</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 100 mV/Div CH1 Coupling dc CH2 Coupling dc</p> <p>Time/Div 1 μs/Div Trigger CH1</p> | <p>Time relationship</p> <p>Pulse shapes</p> | <p>#6</p> |

Table 7-17 Instrument Waveforms

| All jumpers should be in normal position Probe 10:1 | | |
|---|---|--|
| Setup | Important Parameters | Waveform |
| Refer to the SYNC2 Test for setup (7-8, part G). | | |
| <p>COS (no DFA)</p> <p>Connect CH1 to A4 TP24</p> <p>Oscilloscope:</p> <p>CH1 V/Div 100 mV/Div</p> <p>CH1 Coupling dc</p> <p>Time/Div 1 μs/Div</p> <p>Trigger CH1</p> | <p>Time</p> <p>Pulse shape</p> | <p>#7</p> |
| Press A2 S1 to view STIM@. | | |
| <p>STIM@</p> <p>Connect CH1 to A30 TP8</p> <p>Oscilloscope:</p> <p>Bandwidth Limit: ON</p> <p>CH1 V/Div 10 mV/Div</p> <p>CH1 Coupling dc</p> <p>Time/Div 5 μs/Div</p> <p>Trigger CH1</p> | <p>Time</p> <p>Pulse shape</p> <p>Amplitude</p> | <p>CH1 CPLG=DC CH1 = 10 mV/Div</p> <p>MT=CH1 Main = 5 μs/Div</p> <p>#8</p> |
| <p>NDAT and NLD</p> <p>Connect CH1 to A4 TP16</p> <p>Connect CH2 to A4 TP17</p> <p>Oscilloscope:</p> <p>CH1 V/Div 100 mV/Div</p> <p>CH2 V/Div 200 mV/Div</p> <p>CH1 Coupling dc</p> <p>CH2 Coupling dc</p> <p>Time/Div 500 ns/Div</p> <p>Trigger CH1</p> | <p>Time</p> <p>relationship</p> | <p>CH1 CPLG=DC CH2 CPLG=DC CH1 = 100 mV/Div CH2 = 200 mV/Div</p> <p>MT=CH1 Main = 500 ns/Div</p> <p>#9</p> |

Table 7-17 Instrument Waveforms

| All jumpers should be in normal position Probe 10:1 | | |
|---|----------------------|----------|
| Setup | Important Parameters | Waveform |
| <p>SYNC2 and NLD</p> <p>Connect CH1 to A4 TP8 Connect CH2 to A4 TP17</p> <p>Oscilloscope: Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 1 μs/Div Trigger CH2</p> | Time relationship | |
| <p>NLD and NDCK</p> <p>Connect CH1 to A4 TP17 Connect CH2 to A4 TP14</p> <p>Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc</p> <p>Time/Div 1 μs/Div Trigger CH1</p> | Time relationship | |
| Set A8 J3 in test (T) position to view Display Refresh. | | |
| <p>Display Refresh</p> <p>Connect CH1 to A8 TP3</p> <p>Oscilloscope: CH1 V/Div 200 mV/Div CH1 Coupling dc Time/Div 5 ms/Div Trigger CH1</p> | Time | |
| Set A8 J3 to normal (N) position after viewing waveform. | | |

Table 7-17 Instrument Waveforms

| All jumpers should be in normal position Probe 10:1 | | |
|--|--------------------------------------|----------|
| Setup | Important Parameters | Waveform |
| Press the keys as follows to view NSYNC and NCLK: SOURCE SOURCE LEVEL 5 V BURST CHIRP | | |
| NSYNC and NCLK Connect CH1 to A1 J701-1 Connect CH2 to A1 J701-3 Oscilloscope: CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 ms/Div Trigger CH1 | Time | |
| Refer to paragraph 7-11 for the HP 3562A input and key presses to view TRIG IN and TRIGRO. | | |
| TRIG IN and TRIGRO Connect CH1 to A31 TP1 Connect CH2 to A31 TP3 Oscilloscope: Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 2 ms/Div Trigger CH2 | Time Relationship Pulse shape | |

Table 7-17 Instrument Waveforms

| All jumpers should be in normal position Probe 10:1 | | |
|--|---|------------|
| Setup | Important Parameters | Waveform |
| Refer to paragraph 7-11 for the HP 3562A input and key presses to view TRIG1@ and TRIGRO. | | |
| <p>TRIG1@ and TRIGRO</p> <p>Connect CH1 to A32 TP303 Connect CH2 to A31 TP3</p> <p>Oscilloscope:</p> <p>Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 1 ms/Div Trigger CH2</p> | <p>Time Relationship</p> <p>Pulse shape</p> | <p>#15</p> |
| Refer to paragraph 7-11 for the HP3562A input and key presses to view TRIG2@ and TRIGRO. | | |
| <p>TRIG2@ and TRIGRO</p> <p>Connect CH1 to A34 TP303 Connect CH2 to A31 TP3</p> <p>Oscilloscope:</p> <p>Bandwidth Limit: ON CH1 V/Div 100 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 1 ms/Div Trigger CH2</p> | <p>Time Relationship</p> <p>Pulse shape</p> | <p>#16</p> |

Table 7-17 Instrument Waveforms

| All jumpers should be in normal position Probe 10:1 | | |
|---|---|--|
| Setup | Important Parameters | Waveform |
| Press A2 S1 to view STIM@ and CALTRIG. | | |
| <p>STIM@ and CALTRIG</p> <p>Connect CH1 to A30 TP8 Connect CH2 to A30 J30-19</p> <p>Oscilloscope:</p> <p>Bandwidth Limit: ON CH1 V/Div 10 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 5 μs/Div Trigger CH1</p> | <p>Time Relationship</p> <p>Pulse shape</p> | <p>CH1 CPLG=DC CH2 CPLG=DC CH1 = 10 mV/Div CH2 = 200 mV/Div</p> <p>0Vdc</p> <p>0Vdc</p> <p>MT=CH1 Main= 5 μs/Div</p> <p>#17</p> |

7-14 SPCL FCTN KEY MAP

This paragraph shows the location of all the service test keys. Use the key map to find the key for a particular self-test. All keys marked in bold perform a self-test or a group of self-tests. Other soft keys are either used to reach the next level of soft keys or are used for other purposes such as adjustments and signature analysis.

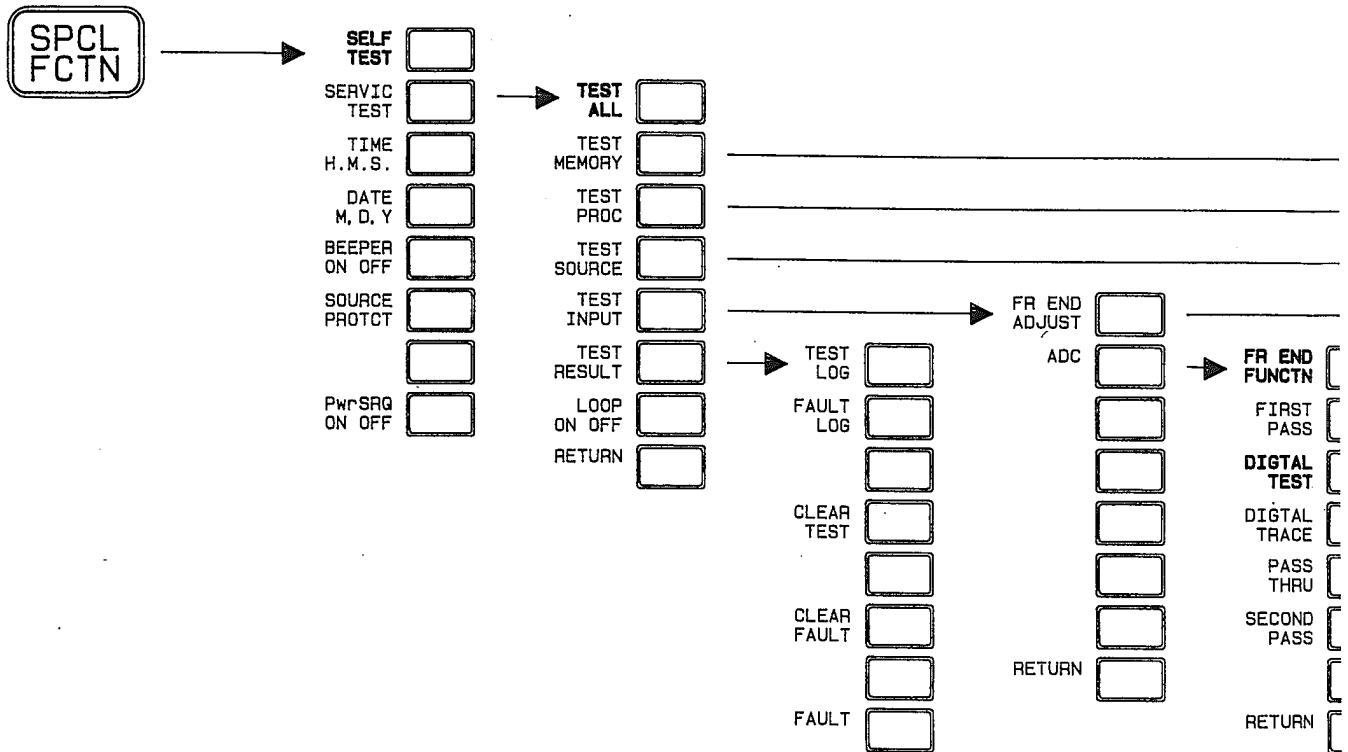
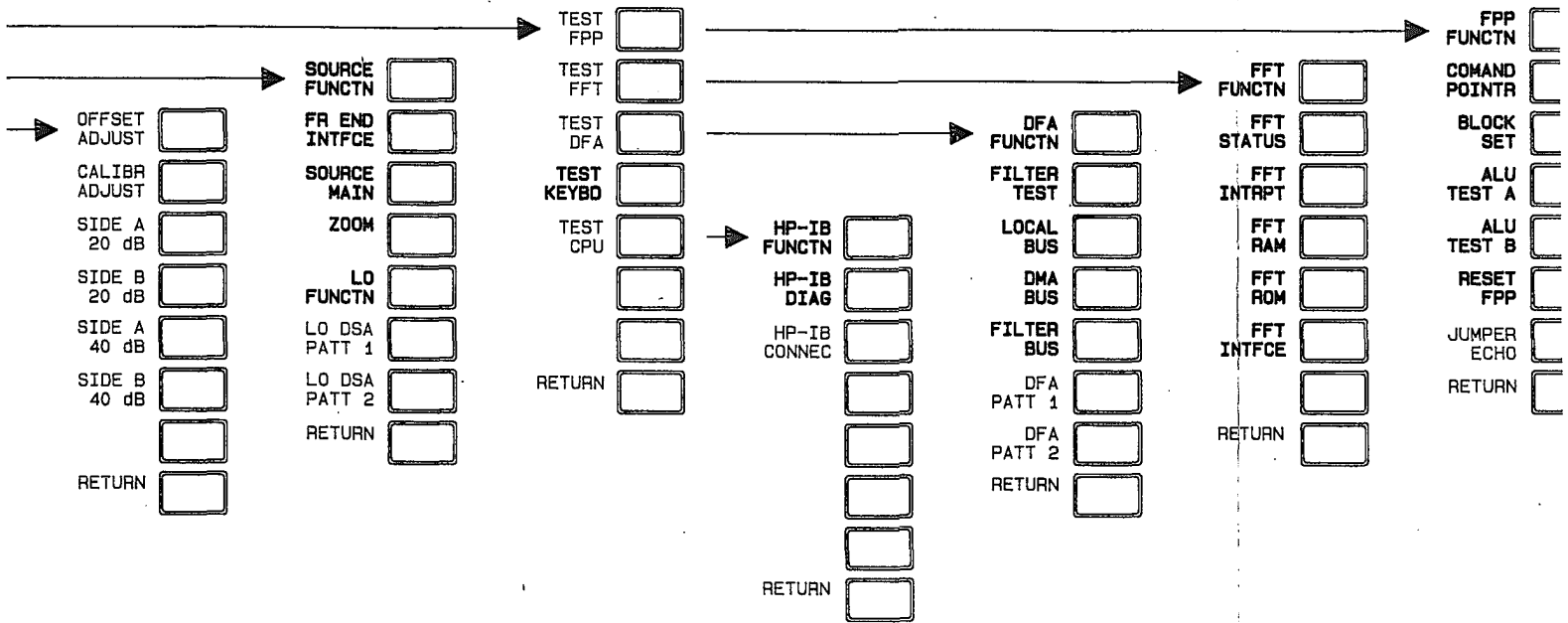


Figure 7-10 SPCL FCTN Key Map



7-15 TEST LOG AND FAULT LOG DESCRIPTIONS

A. Test Log

The test log is a record of the results of the last self-test run. Pass and fail messages are entered in the test log while a self-test is running. The results of the power-up tests are also entered in the test log. If a self-test stops before finishing or to verify the result of the power-up tests, the test log can be read by pressing the keys as follows:

```

SPCL
FCTN  . . . . . SERVICE
          TEST  . . . . . TEST
                        RESULT . . . . . TEST
                                LOG

```

If a self-test fails, error messages are listed for each test, then the test name is listed. For example (figure 7-11), the Gate Array Test only failed on channel 1 when the test was performed in the TEST ALL sequence.

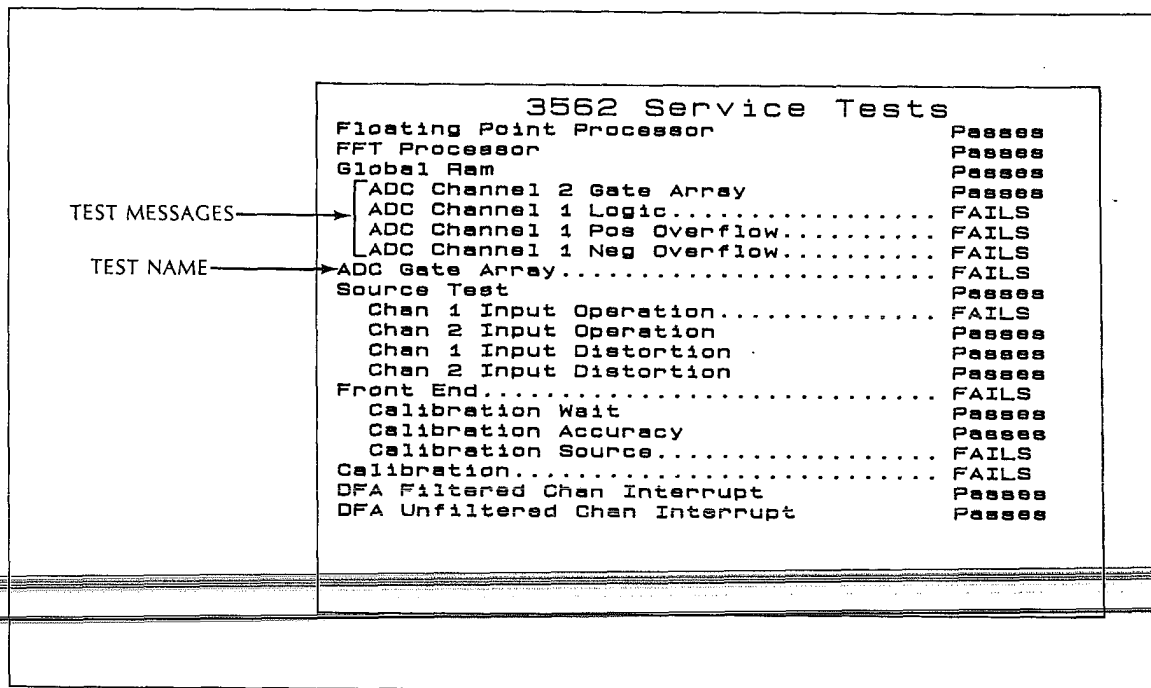


Figure 7-11 Test Log Example

B. Fault Log

The fault log lists the A2 System CPU run-time errors or discrepancies. It also gives the revision code of the software that is in the instrument. Only assemblies that use the system bus generate fault log error messages, however, a failure on any assembly may cause a fault log entry. Use the fault log as a supplement to the fault isolation procedure. To read the test log press the keys as follows:

```
SPCL
FCTN  ..... SERVICE
          TEST  ..... TEST
                          RESULT ..... FAULT
                                  LOG
```

Fault log messages accumulate in the fault log until the log is cleared. Use table 7-18 to interpret fault log messages.

NOTE

Using beeper commands other than those specified in this manual may result in a 'software fault' entry in the fault log.

Table 7-18 System CPU Address Map

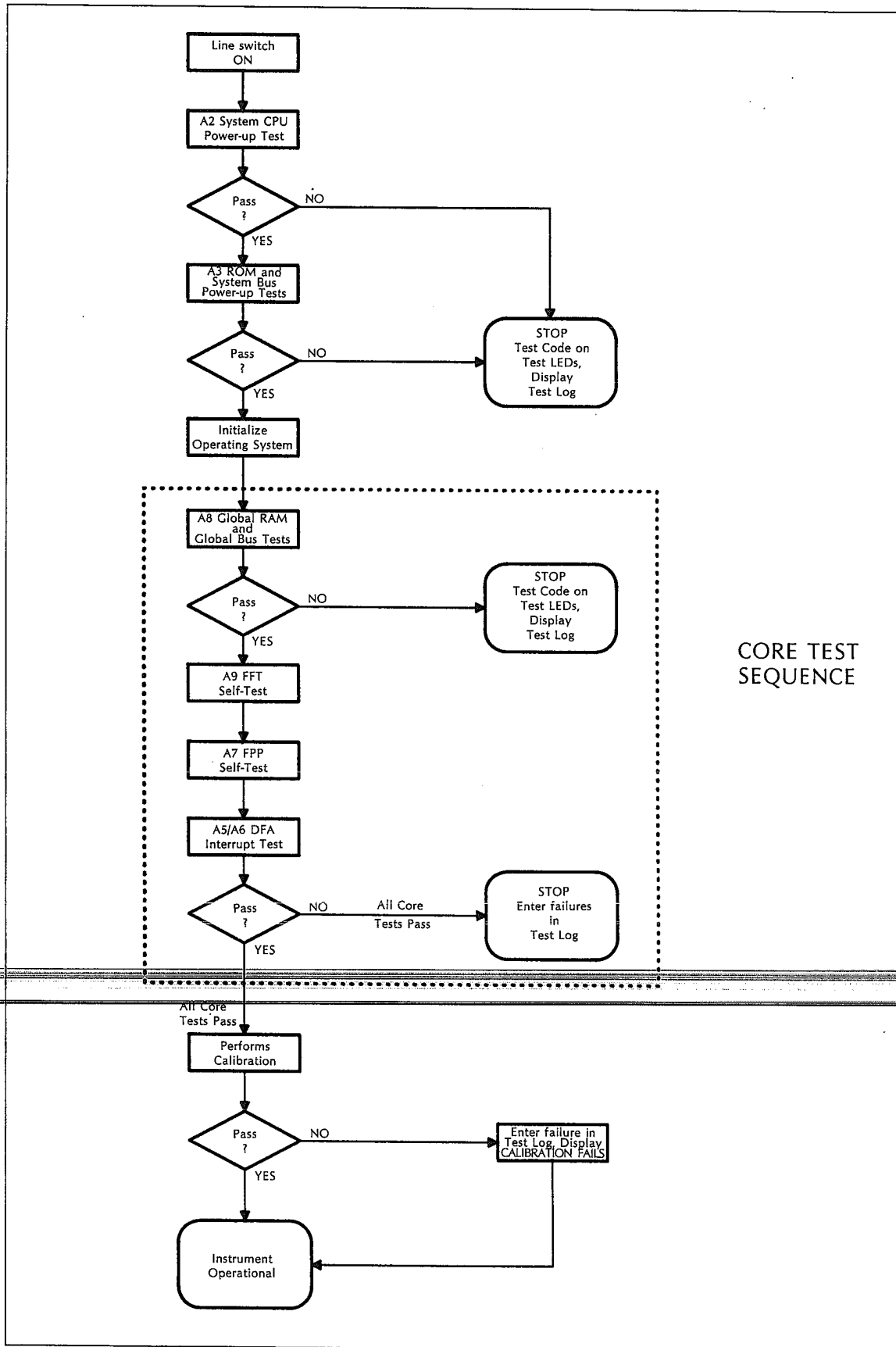
| Data Address | | Description | | |
|--------------|-----------|---|-----------------------------|---|
| From | To | Fault | Assembly Generating Message | Possible Assemblies Failing |
| 00000000 | 00007FFF | Monitor ROM | A2 | A2 |
| 00003D000 | 000040FFF | Program RAM | A2 | A2 |
| 000060000 | 00007FFFF | Data RAM | A8 | A2, A8 |
| 000D00000 | 000E3FFFF | Program ROM | A3 | A2, A3 |
| OFFF8001 | OFFF800F | HPIB | A2 | A2, A22 |
| OFFF8011 | OFFF801F | Programmable Timer | A2 | A2 |
| OFFF8100 | OFFF8104 | Display | A8 | A2, A8, A17 |
| OFFF8121 | OFFF8127 | Keyboard | A15 | A2, A15 |
| OFFF8140 | OFFF8142 | FPP | A7 | A2, A7 |
| OFFF8160 | OFFF817E | IBC | A6 | A2, A5, A6, A31 |
| OFFF8180 | OFFF818F | Front End CONA Timeout Trig Phase Error | A1 | A1, A2, A3, A4, A5, A6 |
| OFFF81A1 | OFFF81AF | LO Lcl Oscil. | A4 | A1, A2, A3, A4, A5, A6, A31, A32, A34 |
| OFFF81C0 | OFFF81CE | FFT | A9 | A2, A9 |
| — | — | Cal Failure | — | Any assembly |

7-16 DIAGNOSTIC DESCRIPTIONS

The self-tests consist of approximately 40 different tests that are run either in groups or individually to test a particular assembly, a function, or the entire instrument. The power-up tests are executed on turn-on, and the rest of the self-tests are invoked by pressing soft keys. This section describes the sequence of tests executed in groups and the SERVIC TEST soft key tests. Refer to table 7-4, "Power-up Test Codes" and table 7-6, "TEST ALL Messages" for a general description of the test result messages. For a detailed explanation of test result messages, refer to the troubleshooting paragraph for the assembly failing.

A. Power-Up Tests

The power-up tests consist of two sets of tests, low-level and high-level. The low-level tests exercise the A2 System CPU, the A3 Program ROM, the A8 Global RAM, the global bus, and the system bus. Fault and pass codes for these assemblies are displayed using the A2 System CPU test LEDs (A2 DS3, A2 DS4). The high-level tests exercise the A9 FFT, A7 FPP, A5 DGTL FLTR, and A6 D FLTR CONT assemblies. Faults on these assemblies are displayed in the test log. The instrument performs a calibration if the power-up tests pass. Refer to figure 7-12 for the power-up sequence.



CORE TEST SEQUENCE

Figure 7-12 Power-up Sequence

B. Service Test Soft Keys

This section describes the function of each of the service test soft keys. Refer to figure 7-10, "SPCL FCTN Key Map" for the location of each of the soft keys. Refer to Section VII and Section VIII for information on how to use the service test soft keys to isolate a failure.

SELF TEST

The SELF TEST key invokes a sequence of self-tests that thoroughly exercises the digital and analog hardware of the instrument. This test is designed to be used by the user to determine if the instrument is functioning correctly. If this self test sequence fails, the failure is entered in the test log and 'Self Test Fails' is displayed. Refer to figure 7-13 for the SELF TEST sequence.

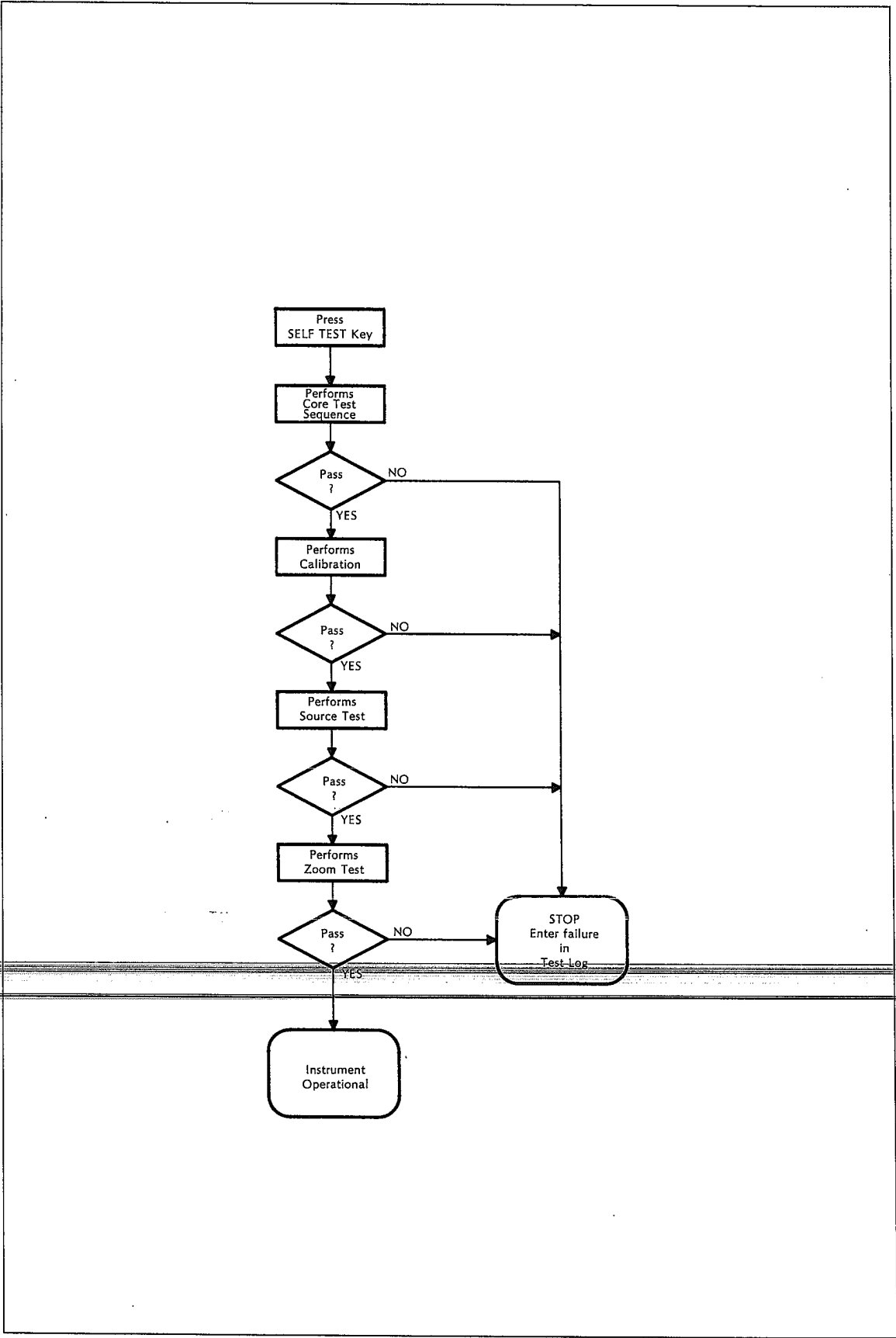


Figure 7-13 SELF TEST Sequence

SERVIC TEST

This key displays the first level of soft keys used in servicing the HP 3562A.

TEST ALL

The TEST ALL key invokes a sequence of self-tests that thoroughly exercises the digital and the analog hardware in the instrument. Each of the self-tests in the TEST ALL sequence can be run individually to help isolate the failure (Refer to paragraph 7-7, "TEST ALL"). As the TEST ALL sequence is executed the results of each self-test is entered in the test log. When the sequence is completed the test log is displayed. Refer to figure 7-14 for the TEST ALL sequence.

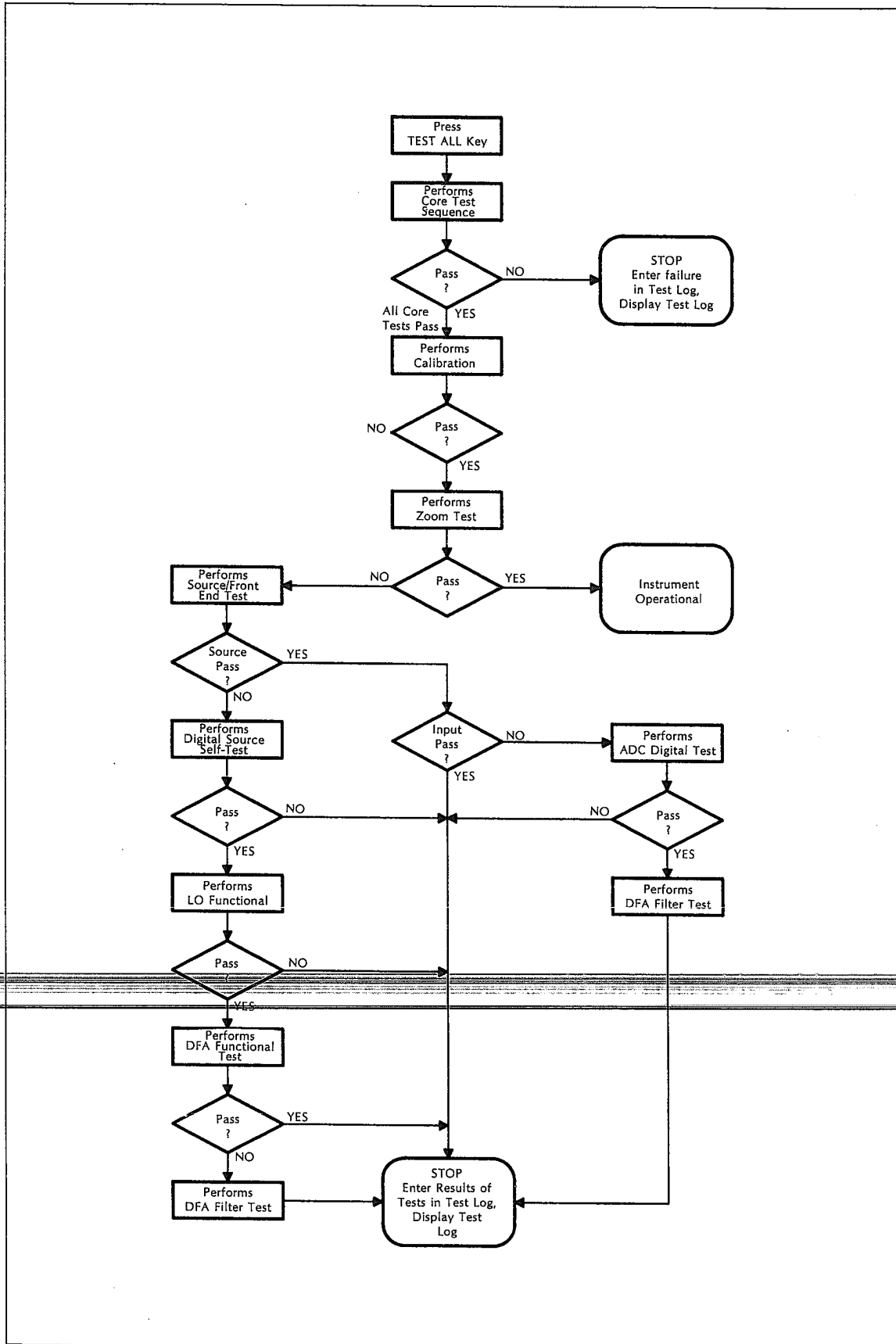


Figure 7-14 TEST ALL Sequence

TEST MEMORY

This key displays the menu of soft keys used in testing the A8 Global RAM and A17 Display Interface.

GLOBAL RAM

This key initiates the global functional test (this test is done on power-up). The global bus is tested by echoing data over the bus. If this test passes, a 'marching pattern' test is done to TEST ALL of the A8 Global memory. In the marching pattern test, data is written into each memory location and then read from the the memory location. The global RAM test also isolates problems on the address lines and in the refresh circuits. To find address failures, the memory is initialized by writing the address of each location into the location. The contents are then read out and verified. (Refer to 8-11)

PROG ROM

At this time, this test has no function. A complete test of the A3 Program ROM is done on power-up.

DSPINT TEST 1, DSPINT TEST 2, DSPINT TEST 3, DSPINT TEST 4

These keys are used to isolated failures in the display interface circuits on the A8 Global RAM and A17 Display Interface assemblies (refer to 8-11). When one of these keys is pressed the HP 1345A display is disabled.

TEST PROC

This key displays the menu of soft keys used to test processing assemblies in the instrument.

TEST FPP

This key displays the menu of soft keys used to test the A7 Floating Point Processor. The FPP function test performs a complex multiplication on internally generated data. For a complete description of the FPP self-tests refer to paragraph 8-10, part C. The JUMPER ECHO test requires jumper A7 J2B to be set to the test position.

TEST FFT

This key displays the menu of soft keys used to test the A9 Fast Fourier Transform Processor. The FFT function test exercises the FFT functions by performing a forward and a reverse FFT, and exponential, Hanning, uniform, flattop, and user-defined windows on a known block of data. For a complete description of the FFT self-tests refer to paragraph 8-13, part A. The instrument needs to be preset before running any of the FFT self-tests. Several measurement setups can cause the FFT self-tests to fail by setting parameters used by the FFT to unknown values.

TEST DFA

This key displays the menu of soft keys used to test the A5 Digital Filter and the A6 Digital Filter Controller. The DFA functional test performs a zoom test using each channel on an internally generated square wave. This test does not use the inputs, ADCs, or analog source assemblies. For a complete description of the DFA self-tests, refer to paragraph 8-9. The DFA PATT 1 test requires jumper A5 J7 to be set to test position. The DFA PATT 1 test is used for self-test and for signature analysis. The DFA PATT 2 is used only for signature analysis. When DFA PATT 2 is pressed 'System Fault' is displayed.

TEST KEYBD

This key tests the A15 Keyboard system interface circuits. The A2 System CPU reads the keyboard status register and compares the result with a known good value. At the same time, the front panel LEDs are flashed on, then off.

TEST CPU

This key displays the menu of the soft keys used to test the HP-IB circuits on the A2 System CPU and the A22 HP-Interface Bus. The HP-IB FUNCTN key tests the General Purpose Interface Bus Adapter (A2 U412) by writing data to its registers and reading the data back. This test does not disturb devices connected to the HP-IB connector. The HP-IB DIAG key tests all of the HP-IB circuits and must not be run with devices attached to the HP-IB connector. The HP-IB CONNEC test is used to troubleshoot the A22 HP-IB connector. Refer to paragraph 8-6, part D for instructions to use the HP-IB Connector test.

TEST SOURCE

This key displays the menu of soft keys used in testing the A1 Digital Source, A4 Local Oscillator, and the A30 Analog Source.

SOURCE FUNCTN

The SOURCE FUNCTN key is used to test the A30 Analog Source (including the calibrator), the A32, A34 ADCs, and the A33, A35 Inputs. This test enables the analog source output and then the calibrator output into the input channels. The results are compared to known values. This test is the same test as the front end functional test (FR END FUNCTN).

FR END INTFCE

This key initiates the Front End Interface test (A1 Digital Source Test test). The A2 System CPU loads the A1 Digital Source with test data for the front end interface circuits (control registers subblock). The system CPU then reads the contents of the digital source's status registers. Failed bits of the status registers are entered in the test log. The front end interface test verifies the circuits on the digital source used to set up the A30 Analog Source, A31 Trigger, A32, A34 ADCs, and the A33, A35 Input assemblies. (Refer to 8-5)

SOURCE MAIN

This key initiates the Digital Source Self Test. The A2 System CPU loads the A1 Digital Source with test data to test most of the digital source's subblocks. The system CPU then reads the contents of the digital source's status registers. Failed bits of the status registers are entered in the test log. (Refer to 8-5)

ZOOM

This key initiates the Zoom Test. A zoomed measurement is done using a test signal from the A30 Analog Source. If this test passes, the A30 Analog Source main output, A4 LO, A5 Digital Filter, A6 Digital Filter Controller, A7 FPP, A9 FFT, and the A8 Global RAM are verified.

LO FUNCTN

This key initiates the LO Functional test. This test causes the LO to output phase and sine values to the A2 System CPU. The system CPU then compares the values to known good values. This test first executes using external clocks (SYNC2 and 10 MHz) and then runs again substituting internal clocks for the SYNC2 and 10 MHz clocks. (Refer to 8-8)

LO DSA PATT 1

This key is used in the A4 Local Oscillator signature analysis tests. (Refer to 8-8)

LO DSA PATT2

This key is used in the A4 Local Oscillator signature analysis tests. (Refer to 8-8)

TEST INPUT

This key displays the menu of soft keys used in testing and adjusting the A30 Analog Source, A32, A34 Analog Digital Converter and the A33, A35 Input assemblies.

FR END ADJUST

This key displays the menu of soft keys used in adjusting the instrument. For a complete description of the adjustments, refer to Section III, "Adjustments".

ADC

This key displays the menu of soft keys used in testing the A32, A34 Analog Digital Converter. The A5 Digital Filter status words are displayed when DIGITAL TRACE, PASS THRU, or SECOND PASS keys are pressed.

FR END FUNCTN

The FR END FUNCTN key is used to test the A30 Analog Source (including the calibrator), the A32, A34 ADCs, and the A33, A35 Inputs. This test enables the analog source output and then the calibrator output into the input channels. The results are compared to known values. This test is the same test as the Source Test (SOURCE FUNCTN).

FIRST PASS

This key displays the result of the first conversion pass of the ADCs. (Refer to 8-19)

DIGITAL TEST

This key initiates a test of the ADC's digital section. The ADC Controller (A32 U602) outputs test patterns to the A5 Digital Filter. The A2 System CPU reads the results from the A5 Digital Filter and compares the results with known good values.

DIGITAL TRACE

When this key is pressed, a test pattern is generated. By running the Digital Trace test in loop mode, a logic probe or oscilloscope can be used to trace digital signals on the A32, A34 assemblies.

PASS THRU

When this key is pressed, the ADC's outputs are displayed in the test log.

SECOND PASS

This key displays the result of the second conversion pass of the ADCs. (Refer to 8-19)

TEST RESULT

This key displays the menu for the Test and Fault Logs. Refer to paragraph 7-15 for a complete description of the Test Log and the Fault Log. The CLEAR TEST key is used to clear the Test Log (press twice to clear log). The CLEAR FAULT key is used to clear the Fault Log (press twice to clear log).

LOOP ON OFF

This key activates and disables the loop mode. The loop mode is used for signature analysis tests and to find intermittent failures. Refer to paragraph 7-12, "Loop Mode and Intermittent Failures" for a complete description of the loop mode and how to use it.

7-17 SELF-CALIBRATION

The HP 3562A has a stable internal calibration source which is used periodically to calibrate the input circuits. The calibration signal is generated on the A30 Analog Source circuit board. The self-calibration runs at the following times if the 'AUTO' calibration key is on: power-on, 8 minutes after power-on, 12 minutes after power-on, 40 minutes after power-on, and every two hours thereafter.

The self-calibration process consists of taking various measurements then generating calibration curves. These curves are used to correct measurements before they are displayed (the A7 FPP includes in its measurement process a complex multiply by a calibration correction curve). Since the calibration adjustments are done to the measurement after it is taken, the input assemblies remain unchanged by the calibration process (except for the value put in the common mode rejection DAC, refer to 6-7 for a description of the common mode rejection DAC). The following measurements are taken to produce the calibration curves:

Free-run measurement using the fixed sine from the analog source (this measurement is used to set the common mode rejection DAC on the A33, A35 Input assemblies)

Single channel triggered measurements using the calibrator (Pseudo Random Noise Source subblock (PRN), the inverse of the PRN, and the 64 kHz square wave)

Free-run frequency response measurement using the periodic chirp from the analog source

Free-run measurement using the fixed sine from the analog source

Press the HP 3562A keys as follows to display an example of the calibration curves:

```

PRESET      ..... RESET

RANGE       ..... 0 dBVrms

SOURCE     ..... SOURCE
                ..... LEVEL          ..... 0 dBVrms

WINDOW    ..... UNIFRM
                ..... (NONE)

A & B

PAUSE/CONT

-----
SPCL
FCTN      ..... BEEPER
                ..... ON OFF          ..... - 516          ..... ENTER
                ..... (toggle key)

SCALE     ..... Y FIXD
                ..... SCALE          ..... -1.5, 1.5 dB

```

Refer to figure 7-15 to see the example of the calibration curves. The range and source level can be varied to display calibration curves for different ranges.

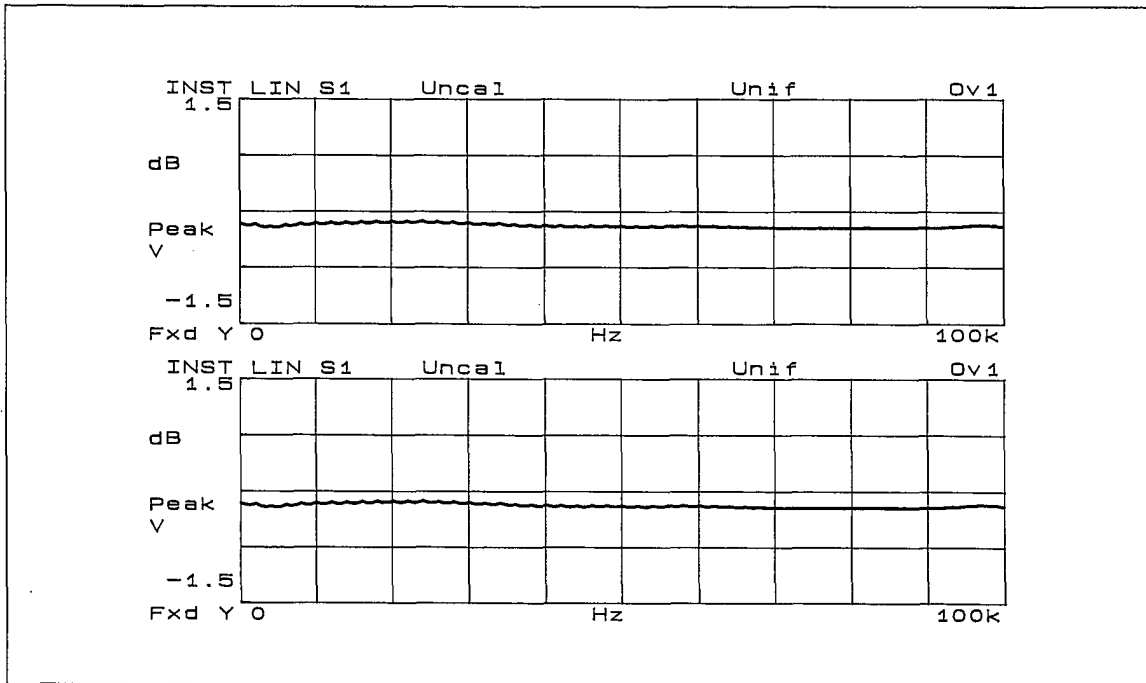


Figure 7-15 Calibration Curves

Calibration Failures

There are three type of calibration failures: calibration wait, calibration accuracy, and calibration source. Calibration failure messages are entered in the test log on power-up and when self-test or TEST ALL are run. A calibration wait failure means the calibration measurement did not complete within the specified time. A calibration accuracy failure means the magnitude or phase values exceeded the following calibration limits:

Single Channel Flatness

±1.5 dBVpk,

Frequency Response

±3.0 dBVpk, ±40°

Single Channel Phase at 0°

±1.5°

If the calibration accuracy failure occurs, the failure is entered in the test log and the calibration curves are used in measurement reading. Any assembly in the instrument can cause a calibration failure. If calibration fails, run the TEST ALL diagnostic to isolate the failing assembly (refer to 7-7). It is also possible that all the assemblies pass their self-tests and there still is a calibration failure.

If the assemblies self-tests pass but there is a 'Calibration Wait' failure, the measurement may not be triggering. Verify the trigger circuits in the instrument (go to 7-11).

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Hewlett-Packard GmbH
Geschäftsstelle
Messerschmittstrasse 7
D-7910 NEU ULM
Tel: 0731-70241

Telex: 0712816 HP ULM-D
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Hewlett-Packard GmbH
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Ehhericherstr. 13
D-8500 NÜRNBERG 10
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Telex: 0623 860
CH,CM,E,MS,P
Hewlett-Packard GmbH
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D-8028 TAUFKIRCHEN
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Telex: 0524985
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PLAISIO S.A.
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Avenida Reforma 3-48, Zona 9
GUATEMALA CITY
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Telex: 4192 TELTRO GU
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Hewlett-Packard Hong Kong, Ltd.
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5th Floor, Sun Hung Kai Centre
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Telex: 66678 HEWPA HX
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E,CH,CS,P

CET Ltd.
1402 Tung Wah Mansion
199-203 Hennessy Rd.
Wanchia, HONG KONG
Tel: 5-729376
Telex: 85148 CET HX
CM

Schmidt & Co. (Hong Kong) Ltd.
Wing On Centre, 28th Floor
Connaught Road, C.
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Tel: 5-455644
Telex: 74766 SCHMX HX
A,M

ICELAND

Elding Trading Company Inc.
Hafrarnvoll-Tryggvagotu
P.O. Box 895
IS-REYKJAVIK
Tel: 1-58-20, 1-63-03
M

INDIA

Computer products are sold through
Blue Star Ltd. All computer repairs and
maintenance service is done through
Computer Maintenance Corp.
Blue Star Ltd.
Sabri Complex II Floor
24 Residency Rd.
BANGALORE 560 025
Tel: 55660
Telex: 0845-430
Cable: BLUESTAR
A,CH*,CM,CS*,E

Blue Star Ltd.
Band Box House
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A,M

Blue Star Ltd.
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Telex: 011-4093
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15/16/C Wellesley Rd.
PUNE 411 011
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A

Blue Star Ltd.
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SECUNDERABAD-500-003
Tel: 72057
Telex: 0155-459
Cable: BLUEFROST
A,E

Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
TRIVANDRUM 695 013
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E
Computer Maintenance Corporation
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115, Sarojini Devi Road
SECUNDERABAD 500 003
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Arranged alphabetically by country

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P

BERCA Indonesia P.T.

P.O.Box 2497/Jkt

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JAKARTA-PUSAT

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A,CS,E,M

BERCA Indonesia P.T.

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SURABAYA

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Telex: 31146 BERSAL SB

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A,E,M,P*

IRAQ

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Telex: 212-455 HEPARQA IK

CH,CS

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A,CH,CM,CS,E,M,P

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M

ISRAEL

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P.O.Box 1270

JERUSALEM 91000

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M

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Hewlett-Packard Italiana S.p.A.

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Viale C. Pavese 340

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CH,E

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CH,E,M,P

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Arranged alphabetically by country

5



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Municipio de Garza Garcia
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Northrop Instruments & Systems Ltd.

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N-5033 FYLLINGSDALEN (Bergen)

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Telex: 16621 hpnas n

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Khimji Ramdas

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MUSCAT

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Telex: 3289 BROKER MB MUSCAT

P

Suhail & Saud Bahwan

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MUSCAT

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Telex: 3274 BAHWAN MB

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Cable: FEMUS Rawalpindi

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Mushko & Company Ltd.

Oosman Chambers

Abdullah Haroon Road

KARACHI 0302

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Calle Samuel Lewis, Ed. Alfa

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Cía Electro Médica S.A.

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MACKAY BOOTH

P

PORTUGAL

Mandinter

Intercambio Mundial de Comércio

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P-LISBON

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M

Soquimica

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1298 LISBOA Codex

Tel: 56 21 81/2/3

Telex: 13316 SABASA

P

Telectra-Empresa Técnica de

Equipamentos Eléctricos S.A.R.L.

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Hewlett-Packard Puerto Rico

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QATAR

Computearbia

P.O. Box 2750

DOHA

Tel: 883555

Telex: 4806 CHPARB

P

Eastern Technical Services

P.O. Box 4747

DOHA

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Nasser Trading & Contracting

P.O. Box 1563

DOHA

Tel: 22170, 23539

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M

SAUDI ARABIA

Modern Electronic Establishment

Hewlett-Packard Division

P.O. Box 22015

Thuobah

AL-KHOBAR

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Abdul Ghani El Ajou

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RIYADH

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P

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A,CH,CS,E,MS,P

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Arranged alphabetically by country



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CM

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Hewlett-Packard So Africa (Pty.) Ltd.
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Pinelands

CAPE PROVINCE 7405

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A,CH,CM,E,MS,P

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Hewlett-Packard So Africa (Pty.) Ltd.

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Hewlett-Packard So Africa (Pty.) Ltd.

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A,CH,CS,E,MS,P

Hewlett-Packard Española S.A.

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A,CH,E,MS

Hewlett-Packard Española S.A.

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A,CS,MS,P

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July 1983 5952-6900

Indicates main office

HP distributors are printed in italics.



SERVICE MANUAL

MODEL 3562A

DYNAMIC SIGNAL ANALYZER

Serial Number: 2435A00101

IMPORTANT NOTICE

This manual applies to instruments with the above serial number and greater. As changes are made in the instrument to improve performance and reliability, the appropriate pages will be revised to include this information.

WARNING

To prevent potential fire or shock hazard, do not expose instrument to rain or moisture.

Manual Part No. 03562-90010
Microfiche No. 03562-90210

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**HEWLETT
PACKARD**

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by -hp-. Buyer shall prepay shipping charges to -hp- and -hp- shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to -hp- from another country.

HP software and firmware products which are designated by HP for use with a hardware product, when properly installed on that hardware product, are warranted not to fail to execute their programming instructions due to defects in materials and workmanship. If HP receives notice of such defects during their warranty period, HP shall repair or replace software media and firmware which do not execute their programming instructions due to such defects. HP does not warrant that the operation of the software, firmware or hardware shall be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements. This is a Safety Class 1 instrument.

GROUND THE INSTRUMENT

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SAFETY SYMBOLS

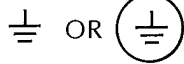
General Definitions of Safety Symbols Used On Equipment or In Manuals.



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.



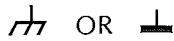
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

N O T E: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

SECTION VIII

SERVICE

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SECTION VIII SERVICE

8-1 INTRODUCTION

This section contains all the information required to isolate failures to the component level. Use this section after using the fault isolation procedures in Section VII. This section is used to isolate a failure to the subblock level. Each functional subblock consists of a small number of components, and the technician's expertise is relied upon to isolate the faulty component.

How to Use This Section

Start After isolating the fault to an assembly, go to the troubleshooting procedures for that assembly. The troubleshooting information is listed in order of the circuit board assembly number, A1 through A33.

Reference Use the component locators and schematics in Section IX with each of the troubleshooting procedures.

For the location of cables and boards refer to figure 4-1 in Section IV.

For the circuit block diagrams refer to Section VI.

To understand the instrument's operation and signal mnemonics refer to Section VI.

Keys There are two types of keys on the HP 3562A, hard keys and soft keys. In this section the hard keys are in bold text, and the soft keys are in regular text.

For example:

FREQ FREQ SPAN **10** kHz

This example instructs you to press the hard key **FREQ** and the soft key FREQ SPAN. After pressing the soft key FREQ SPAN enter 10 kHz.

Loop Mode The loop mode is used for some signatures analysis tests and to find intermittent failures. For description of the loop mode refer to paragraph 7-12, "Loop Mode and Intermittent Failures".

NOTE

After completing a test or repair, check that all jumpers are in the NORMAL or RUN position and that all cables are connected.

8-2 RECOMMENDED TEST EQUIPMENT

The recommended test equipment for troubleshooting is listed in table 1-4. Any item which meets or exceeds the critical requirements can be substituted for the model listed.

8-3 LOGIC CONVENTIONS

Positive logic convention is used in this manual unless otherwise noted. Positive logic conventions define a logic "1" or "High" as more positive voltage and a logic "0" or "Low" as the more negative voltage.

8-4 SAFETY CONSIDERATIONS

The HP 3562A is a Safety Class 1 instrument (provided with a protective earth terminal). The instrument and manuals should be reviewed for safety markings and instructions before operation. Refer to the safety symbol table in the preface of this manual.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury.

CAUTION

Do not insert or remove any circuit board in the HP 3562A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards.

WARNING

230 Vdc is present in the A18 power supply assembly even with the line switch in the off position and the power cord removed. Be extremely careful when working in the power supply area. This high voltage could cause serious personal injury if contacted. To discharge the capacitors holding this voltage perform steps 1 through 3.

- 1. Remove the power cord from the rear panel.*
- 2. Remove the bottom cover and power supply shield.*
- 3. Wait two minutes after turning the power off to allow the capacitors to discharge.*

8-5 A1 DIGITAL SOURCE

The information in this section should be used to isolate faulty subblocks in the A1 Digital Source assembly. All procedures assume the Fault Isolation procedures of Section VII have been used to determine which board has failed, and the circuit descriptions of Section VI are understood.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury.

CAUTION

Do not insert or remove any circuit board in the HP 3562A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards.

How to Use This Section

| | |
|---------------------|--|
| Start | The primary method for troubleshooting the digital source assembly is to use signature analysis and the waveforms provided in parts E and F. Start troubleshooting by using part A, "Digital Source Diagnostics" to isolate the failure to a subblock. |
| Reference | For the component locator and schematic refer to Section IX. For the location of cables and boards refer to figure 4-1 in Section IV. |
| Verify | Use the oscilloscope waveforms in table A1-10 to see correct operation at various test points in the assembly. |
| After-Repair | Use table A1-11 to determine which adjustments and tests need to be done to complete instrument service. |

A. Digital Source Diagnostics

The digital source is tested using two self-tests; the front end interface test and the source main test. When either of these tests are initiated, the test registers and control registers are loaded with test data and the TEST signal to the test registers goes low. The test is performed and the contents of the status registers is read and verified by the A2 System CPU. Any failed bits are annunciated on the display. These tests are also used in loop mode for signature analysis patterns.

1. To perform the self-tests, press the HP 3562A keys as follows:

```

SPCL
FCTN      ..... SERVIC
                TEST      ..... TEST
                                SOURCE ..... FR END
                                                INTFCE

                                                ..... SOURCE
                                                                MAIN
    
```

2. Refer to table A1-2 for single bit failures to determine the probable subblock failing.
3. Go to part B for multiple bit failures.
4. If both tests pass but a source function or a trigger mode is failing, use table A1-1 to determine the probable subblock failing.

Table A1-1 Digital Source Functions

| Function Failing or Defective | Probable Cause of Failure |
|---|---|
| Triggered Mode | Phase Resolution Circuit (go to part E) |
| Single Channel Phase | Phase Resolution Circuit (go to part E) |
| CNTCLK | Control Registers (go to part E, step 7) |
| Sine Wave Output | LO Input Receiver (go to part E) |
| Source Energy Measurement fails (2-41) but random noise operates at full span | Effective Sample Rate Generator (go to part D) |
| Random Noise Output | Noise Generator (go to part E, step 8) |
| Burst Mode | Burst Control Circuit (go to part E, step 5) |
| SYNC OUT output | Burst Control Circuit (refer to waveform #5) |
| Periodic Chirp | Effective Sample Rate Generator (go to part D) |

Table A1-2 Digital Source Diagnostics

| Bit # | Signal Name | From Component | Subblock Returning Status Bit Probable subblock failing |
|-------|---------------------------------|-------------------------|---|
| 0 | LDCH1L | U208-6 | Control Registers (Go to part E, step 7) |
| 1 | LDCH2L | U208-7 | |
| 2 | LDTRL | U208-5 | |
| 3 | LDSRCL | U208-4 | |
| 4 | SRCOUTFALTL | — | Status Registers (Go to part E) |
| 5 | UNLOCK | — | |
| 6 | C10FSE | U101-7 | Timing Control Circuit (Go to part D) |
| 7 | CNTLD | U206-9 | Control Registers (Go to part E, step 7) |
| 8 | NCLK | U202-12 | Burst Control Circuit (Go to part E, step 5) |
| 9 | DOUT | U209-6 | Multiplier (Go to part E) |
| 10 | DMID | U13-13 | LO Input Receiver (Go to part E) |
| 11 | NSR | U311-11 | Noise Generator (Go to part E, step 8) |
| 12 | CNTRL BUSY | U106-8 | Control Registers (Go to part E, step 7) |
| 13 | BUSYL | U5-14 | Phase Resolution Circuit (Go to part E) |
| 14 | TRIGGERED | U8-9 | |
| 15 | ARMEDL | U5-15 | |
| — | Digital Source Counters Fail | U305, U7, U107, U108 | These counters are used in the following subblocks: Phase Resolution Circuit Timing Control Circuit Burst Control Circuit (Go to part E) |

B. Subblock Verification Tests

The digital source performs several functions including generating band-limited random noise, interfacing the local oscillator with the analog source, synchronizing trigger operations, and interfacing the front end assemblies (inputs, ADCs, trigger, and analog source) with the A2 System CPU. Most functions use only a few of the DS subblocks. To isolate the failure to a subblock, use table A1-3 after performing the following steps:

1. Connect the front panel source output to channel 1.
2. Connect the rear panel SYNC OUT output to channel 2.
3. Press the HP 3562A keys as follows:

```

PRESET ..... RESET

RANGE ..... 5.6 V

SOURCE ..... SOURCE
                  LEVEL ..... 5 V
                  ..... FIXED
                  ..... SINE ..... 1 kHz

MEAS
DISP ..... FILTRD
                  INPUT ..... TIME
                                      REC 1

SCALE ..... Y FIXD
                  SCALE ..... 6, -6 V
    
```

Refer to figure A1-1 to verify result.

NOTE

The free-run mode is used for most of the following waveforms. This is done to isolate failing functions to a subblock. When the trigger mode is not used, the waveforms move around on the display. The trigger mode is verified in step 7.

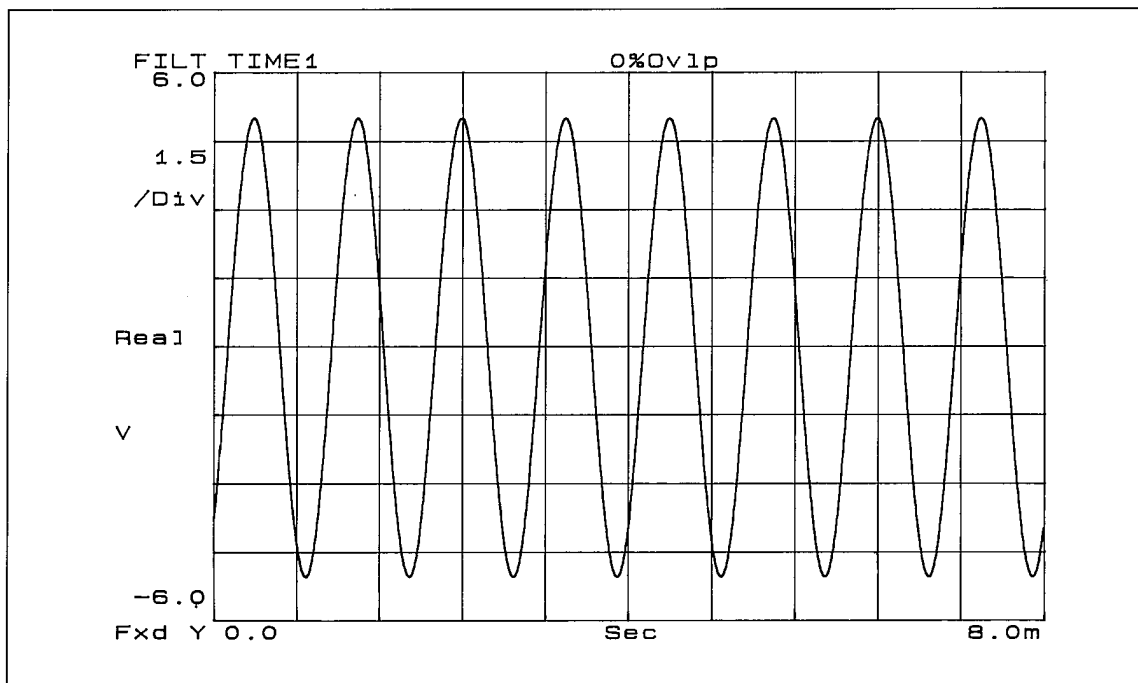


Figure A1-1 Sine Wave

If the figure A1-1 is correct, the following subblocks are verified:

LO Input Receiver

Multiplier

Timing State Machine (U3)

4. Press the HP 3562A keys as follows:

**SOURCE RANDOM
NOISE**

Refer to figure A1-2 to verify result.

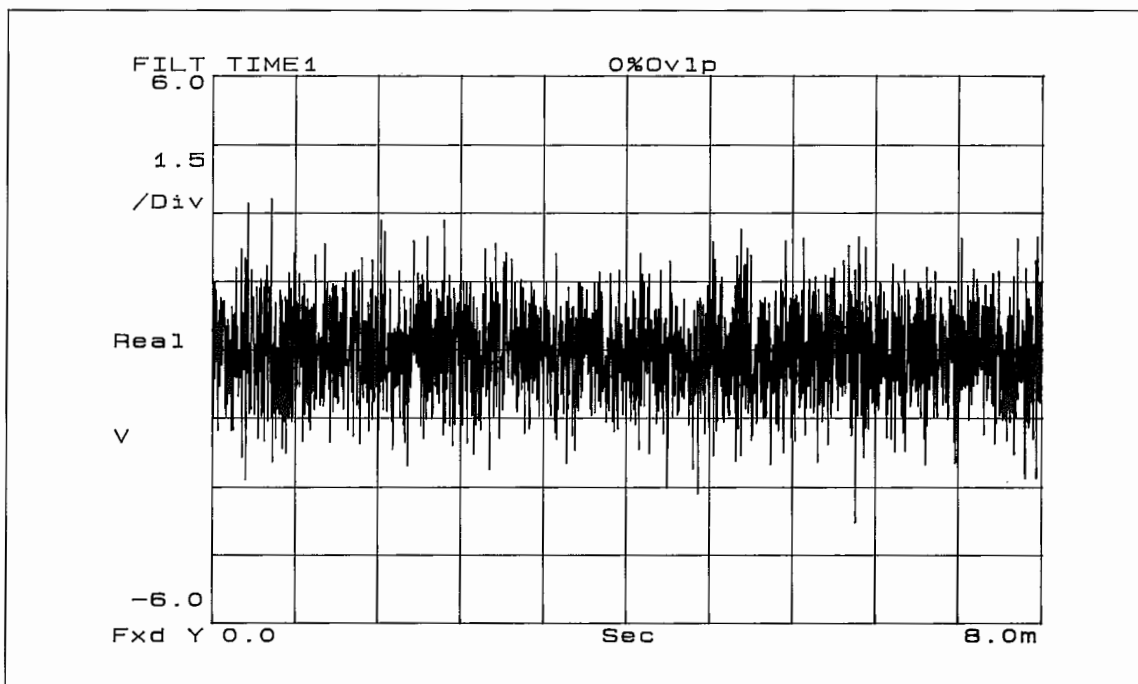


Figure A1-2 Random Noise

If figure A1-2 is correct the following subblock is verified:

Noise Generator

5. The random noise should follow the frequency span as it is changed. The display should appear similar to figure A1-2 as the frequency span is changed. To change frequency spans, press the HP 3562A keys as follows:

```

FREQ ..... FREQ
                SPAN ..... 1 kHz
                ..... 10 kHz
                ..... 50 kHz
    
```

If the random noise follows the frequency span, the following subblock is verified:

Effective Sample Rate Generator

6. Press the HP 3562A keys as follows:

FREQ MAX
SPAN

B

MEAS
DISP FILTRD
INPUT TIME
REC 2

SCALE Y FIXD
SCALE 6, -6 V

A & B

SOURCE BURST
RANDOM

Refer to figure A1-3 to verify result.

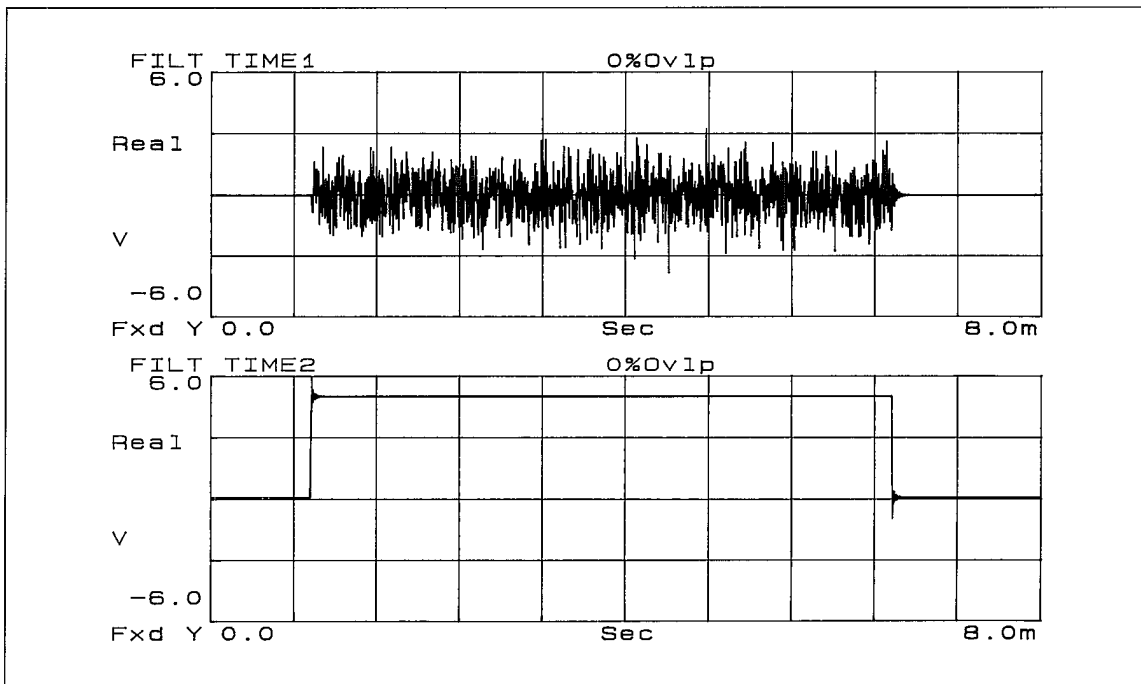


Figure A1-3 Burst Random #1

Press the HP 3562A keys as follows:

```

SOURCE..... BURST
                RANDOM ..... 25 ..... ENTER
    
```

Refer to figure A1-4 to verify result.

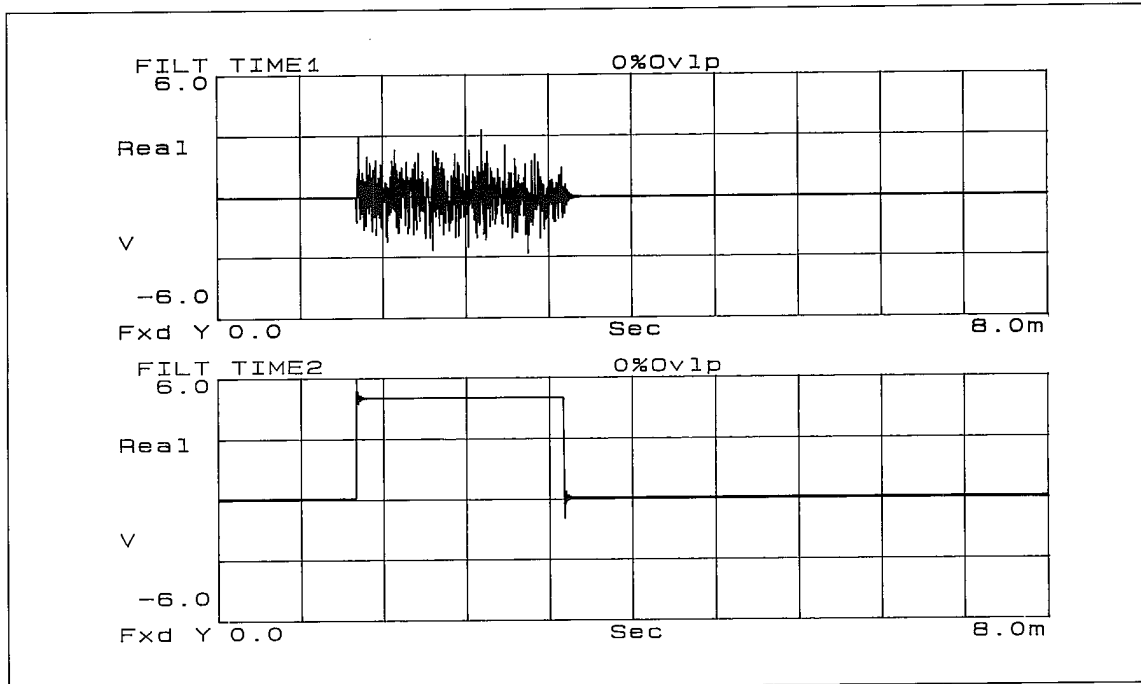


Figure A1-4 Burst Random #2

If figures A1-3 and A1-4 are correct, the following subblock is verified:

Burst Control Circuit

7. Press the HP 3562A keys as follows:

```

SOURCE..... FIXED
                SINE ..... 1 kHz

SELECT
TRIG ..... SOURCE
                TRIG
    
```

The source trigger point may vary on the sine wave, but the trigger point on the SYNC OUT waveform should be the same as displayed in figure A1-5.

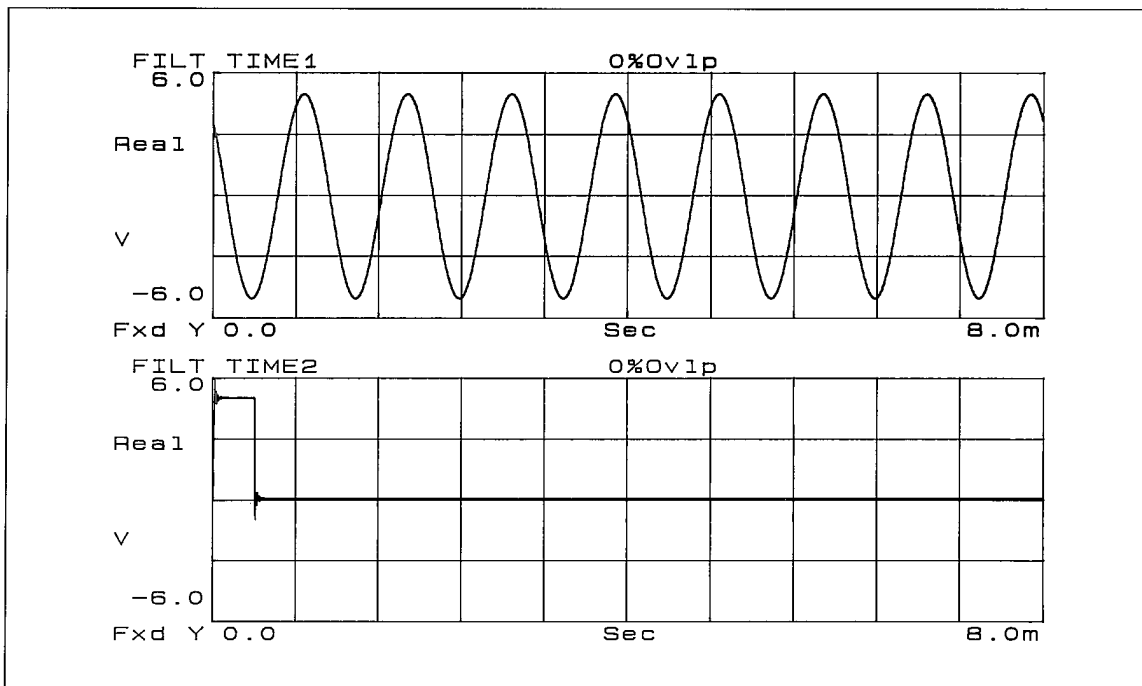


Figure A1-5 Source Trigger

If figure A1-5 is correct, the following subblock is verified:

Phase Resolution Circuit

Table A1-3 Digital Source Failures

| <p>Test Results</p> | <p>Most Likely Cause of Failure Troubleshoot subblocks in order listed.</p> |
|--|--|
| <p>Digital Source Main Test Passes Digital Source Counters Passes</p> <p>Digital Source F/E Interface Fails Bits: 0,1,2,3,7, or 12</p> | <p>Control Registers</p> <p>(Go to part E, step 7)</p> |
| <p>Digital Source F/E Interface Passes Digital Source Counters Pass or Fail</p> <p>Digital Source Main Test Fails Bits: 6,9,10</p> | <p>Timing Control Circuit LO Input Receiver Multiplier</p> <p>(Go to part E)</p> |
| <p>Digital Source F/E Interface Passes Digital Source Counters Pass</p> <p>Digital Source Main Test Fails Bits: 9,10</p> <p>Functions: Sine Output is defective, but Burst Random and SYNC OUT operate</p> | <p>LO Input Receiver</p> <p>(Go to part E)</p> |
| <p>Digital Source F/E Interface Passes Digital Source Counters Pass or Fail</p> <p>Digital Source Main Test Fails Bits: 9,10</p> <p>Functions: Source Output Defective Random Noise Defective</p> | <p>Timing Control Circuit LO Input Receiver Multiplier</p> <p>(Go to part E)</p> |
| <p>Digital Source F/E Interface Passes Digital Source Counters Pass or Fail</p> <p>Digital Source Main Test Fails Bits: 13, 14, or 15</p> | <p>Phase Resolution Circuit</p> <p>(Go to part E)</p> |

Table A1-3 Digital Source Failures cont.

| Test Results | Most Likely Cause of Failure Troubleshoot subblocks in order listed. |
|--|--|
| Digital Source F/E Interface Passes Digital Source Counters Pass or Fail Digital Source Main Test Fails Bits: 6,9,10 and one or more of the following bits: 11, 12, 13, 14, 15 | Programmable Counters Phase Resolution Circuit Timing Control Circuit (Go to part E) |
| Digital Source F/E Interface Fails Digital Source Main Test Fails Bits: Multiple Failures Functions: No functions operate | DS Data Bus System Interface Device Decoder PAL or Buffer Programmable Counters Status Registers Test Registers Control Registers' Latches (Go to part C) |

C. Multiple Failures Test

This test verifies the DS data bus, the system interface, and the device decoder PAL and buffer.

1. Press the line switch off. Place the A1 Digital Source on the 03562-66540 extender board.
2. Use a logic probe to verify the system interface lines are toggling between TTL level high and TTL level Low. Use the following test locations:

U404-19

U403 pins 11, 13 through 18

3. Press the HP 3562A keys as follows:

```

SPCL
FCTN ..... SERVICE
                TEST      ..... LOOP
                                ON
                                ..... TEST
                                SOURCE ..... SOURCE
                                                MAIN
    
```


- To verify the device decoder PAL and buffer, use a logic probe to check the following signals are the correct TTL level:

| | | | | | | | |
|------|-----|----|----------|------|-----|----|----------|
| U303 | pin | 12 | Toggling | U401 | pin | 2 | Toggling |
| | | 13 | Toggling | | | 7 | Toggling |
| | | 14 | Toggling | | | 10 | Toggling |
| | | 15 | Toggling | | | 11 | Toggling |
| | | 16 | Toggling | | | | |
| | | 17 | High | | | | |
| | | 18 | Toggling | | | | |
| | | 19 | Toggling | | | | |

- Press the HP 3562A keys as follows:

```

RETURN..... LOOP
                OFF

                ..... LOOP
                ON          ..... TEST
                               SOURCE          ..... FR END
                                               INTFCE
    
```

- Use a logic probe to verify the following signals are the correct TTL level:

| | | | |
|------|-----|----|----------|
| U303 | pin | 12 | High |
| | | 13 | Toggling |
| | | 14 | High |
| | | 15 | High |
| | | 16 | Toggling |
| | | 17 | Toggling |
| | | 18 | Toggling |
| | | 19 | Toggling |

- Use a logic to verify the DS data lines are toggling (FR END INTFCE in loop mode). Some of the lines will toggle slowly. Use the following test locations:

U406 pins 1 and 11 through 19

U405 pins 11 through 18

- Press A2 S1. After the power-up tests are complete, verify the following signals are the correct TTL level:

| Test Location | Signal Name | TTL Level |
|---------------|-------------|-----------|
| U203-2 | TEST | Low |
| U304-6 | NRSTL | High |
| U304-9 | BRST | High |
| U302-4 | RESETL | High |

- If the fault has not been found, go to part E.

NOTE

When finished with the test, turn the loop mode off by pressing the keys as follows:

RETURN LOOP
OFF

Table A1-6 DS Signature Analysis Test #1

| Source Main Test Source Main Test in loop mode Jumpers in normal (N) position: All jumpers Signature Analyzer Setup: Refer to table A1-5 +5 V Signature = H166 | | | | | |
|---|------|-----------|-----------|------|-----------|
| Component | Pin | Signature | Component | Pin | Signature |
| U1 | 11 | U233 | U7 | 8 | 0000 |
| | 12 | 40C9 | | 9 | H166 |
| | 13 | C9FH | | 10 | 5791 |
| | 14 | 7467 | | 12 | H166 |
| | 15 | PO9H | | 13 | H10F |
| U2 | 11 | 9765 | U8 | 5 | 615F |
| | 12 | 9206 | | 6 | CO3A |
| | 13 | HA1F | | 8 | 006A |
| | 14 | 6P24 | | 9 | H10F |
| | 15 | 41CF | U9 | 5 | F4U5 |
| U3 | 12 | AU9H | | 6 | 1593 |
| | 13 | 460C | | 8 | C88U |
| | 14 | 12C3 | 9 | 69P9 | |
| | 15 | 49H2 | U10 | 3 | 93AH |
| | 16 | C26H | | 4 | 7003 |
| 17 | 2F90 | 5 | | 01H4 | |
| 18 | H166 | 6 | | C93U | |
| 19 | 2FP4 | 10 | | 654A | |
| U4 | 3 | 36UF | | 11 | 0C70 |
| | 6 | H166 | 12 | CF6H | |
| | 8 | OUH3 | 13 | 67P3 | |
| | 11 | HPC5 | U11 | 12 | 5612 |
| U5 | 12 | H10F | | 13 | 2FU6 |
| | 13 | 5791 | | 14 | UHAP |
| | 14 | H10F | | 15 | 858P |
| | 15 | 9AUF | | 16 | 5612 |
| | 16 | 6866 | | 17 | 2FU6 |
| | 17 | 97C4 | 18 | UHAP | |
| U6 | 18 | H166 | U12 | 12 | 127P |
| | 19 | 3486 | | 13 | 8340 |
| | 3 | H10F | | 14 | 7716 |
| | 6 | H10F | | 15 | 43A6 |
| 8 | 21F2 | 16 | | 127P | |
| 11 | H166 | 17 | | 8340 | |
| | | | | 18 | 7716 |

Table A1-6 DS Signature Analysis Test #1 cont.

| Component | Pin | Signature | Component | Pin | Signature | |
|-----------|------|-----------|-----------|---------------------|-----------|------|
| U13 | 13 | 5730 | U111 | 12 | 5612 | |
| U101 | 7 | C2H9 | | 13 | 2FU6 | |
| U102 | 12 | 811H | | 14 | UHAP | |
| | 13 | 8315 | | 15 | 858P | |
| | 14 | C957 | | 16 | 5612 | |
| | 15 | 02PU | | 17 | 2FU6 | |
| | 16 | 5UA9 | | 18 | UHAP | |
| | 17 | PA58 | | 19 | 858P | |
| U103 | 18 | H166 | | U112 Δ Rev. A | 12 | 127P |
| | 19 | H166 | | | 13 | 8340 |
| | 2 | 10AH | 14 | | 7716 | |
| | U105 | 4 | C367 | | 15 | 43A6 |
| 5 | | H166 | 16 | | 127P | |
| 7 | | C367 | 17 | | 8340 | |
| 9 | | 0000 | 18 | | 7716 | |
| U106 | 14 | 0000 | 19 | | 43A6 | |
| | 5 | A75U | U113 | | 12 | 5UPH |
| | 6 | 7639 | U201 | 1 | 31UC | |
| | 8 | 0000 | | 4 | F6P2 | |
| 9 | H166 | 10 | | 304P | | |
| U107 | 9 | H166 | | 13 | 0000 | |
| | 10 | 5791 | U202 | 6 | HPC5 | |
| | 12 | H166 | | 10 | 2C66 | |
| | 13 | H10F | U203 | 2 | H166 | |
| U108 | 9 | H166 | | 6 | 0000 | |
| | 10 | 5791 | | 9 | 47HH | |
| | 12 | H10F | | 12 | 465U | |
| | 13 | H10F | 16 | UA00 | | |
| U109 | 6 | H166 | U204 | 2 | C367 | |
| | 8 | H166 | | 5 | 653U | |
| U110 | 3 | 1AUA | | 15 | P79A | |
| | 4 | C4A8 | 16 | 0000 | | |
| | 5 | 6381 | U209 | 6 | 7H1U | |
| | 6 | 8815 | | U302 | 4 | H166 |
| | 10 | UHHU | 8 | | H166 | |
| | 11 | F73A | 10 | | 2C66 | |
| | 12 | HA48 | | | | |
| | 13 | 54U1 | | | | |

Δ See backdating.

Table A1-6 DS Signature Analysis Test #1 cont.

| Component | Pin | Signature | Component | Pin | Signature |
|-----------|------|-----------|-----------|------|-----------|
| U304 | 1 | H166 | U306 | 6 | H166 |
| | 2 | F11P | U307 | 15 | 465U |
| | 5 | 7557 | | 16 | 47HH |
| | 6 | 5FF3 | U308 | 4 | UA00 |
| | 8 | 47HH | | 7 | 465U |
| | 12 | OUIH3 | | 12 | H166 |
| | 13 | 465U | U407 | 1 | H166 |
| | 16 | HPC5 | | 6 | 47HH |
| | 17 | UA00 | | 7 | 47HH |
| 19 | 1078 | U409 | 12 | H166 | |
| U305 | 2 | | UA00 | 13 | FC55 |
| | 4 | | 465U | 14 | H166 |
| | 5 | | 47HH | 15 | 95C3 |
| | 9 | | A75U | 16 | FAH9 |
| | 10 | | F2HP | 17 | PFH9 |
| | 11 | | 5FF3 | 18 | H9C3 |
| | 13 | | A392 | 19 | 0000 |
| | 14 | | 811H | | |
| | 15 | F6P2 | | | |
| 16 | 811H | | | | |
| 17 | 77P7 | | | | |
| 18 | 304P | | | | |

5. To start signature analysis test #2, perform the following steps:
 - a. Press the line switch off.
 - b. Set A1 J3 to test position.
 - c. Press the line switch on.
 - d. Press the HP 3562A keys as follows:

```

SPCL          .....  SERVIC
FCTN          .....  TEST          .....  LOOP
                                          ON
                                          .....  TEST
                                          SOURCE          .....  SOURCE
                                          MAIN
    
```

NOTE

DS Signature Analysis Test #2 disables the feedback loop between the burst state machine (U102) and the burst control circuit's counters (U305).

Table A1-7 DS Signature Analysis Test #2

| Burst Control Circuit | | | | | |
|--|------|-----------|-----------|-----|-----------|
| Source Main Test in loop mode | | | | | |
| Jumpers in normal (N) position: All jumpers except A1 J3 | | | | | |
| Jumpers in test (T) position: A1 J3 | | | | | |
| Signature Analyzer Setup: Refer to table A1-5 | | | | | |
| +5 V Signature = H166 | | | | | |
| Component | Pin | Signature | Component | Pin | Signature |
| U102 | P75H | | U305 | 13 | 7U6P |
| | 13 | 19C5 | | 17 | PHF6 |
| | 14 | 45C7 | | | |
| | 15 | 02PU | | | |
| | 16 | 5UA9 | | | |
| | 17 | PA58 | | | |
| | 18 | H166 | | | |
| | 19 | H166 | | | |

6. Put jumper A1 J3 in normal (N) position.
7. To start signature analysis test #3, perform the following steps:
 - a. Set A1 J3 in normal (N) position.
 - b. Press A2 S1.
 - c. Press the HP 3562A keys as follows:

```

SPCL
FCTN      .....  SERVIC
                        TEST      .....  LOOP
                                                ON
                                                .....  TEST
                                                SOURCE      .....  FR END
                                                                    INTFCE
    
```

Table A1-8 DS Signature Analysis Test #3

| Front End Interface Test Front End Interface in loop mode Jumpers in normal (N) position: All jumpers Signature Analyzer Setup: Refer to table A1-5 +5 V Signature = 088C | | | | | |
|--|------|-----------|-----------|------|-----------|
| Component | Pin | Signature | Component | Pin | Signature |
| U4 | 6 | H359 | U205 | 11 | 088C |
| U6 | 11 | H359 | | 13 | FC45 |
| U104 | 3 | 6F76 | U206 | 7 | 6574 |
| | 4 | HCH2 | | 9 | 6HUU |
| | 5 | 5289 | U207 | 7 | F472 |
| | 6 | P7CC | | 9 | FFU9 |
| | 8 | 0000 | U208 | 4 | 95HH |
| | 9 | 3U2P | | 5 | 99C5 |
| 10 | 7FP2 | 6 | | UOH8 | |
| 11 | 6H62 | 7 | | UF01 | |
| U106 | 8 | C49A | U302 | 8 | CF11 |
| U109 | 3 | 083A | | | |
| U204 | 1 | 088C | | | |
| | 2 | 0000 | | | |
| | 5 | 8FFP | | | |
| | 6 | OJA9 | | | |
| | 9 | UO39 | | | |
| | 12 | CCC3 | | | |
| 15 | 0000 | | | | |
| 16 | 0000 | | | | |
| 19 | 0000 | | | | |

8. To start signature analysis test #4, perform the following steps:

- a. Press the line switch off.
- b. Connect U311 pin 10 to TP15.
- c. Press the line switch on.
- d. Press the HP 3562A keys as follows:

```

SPCL
FCTN      .....  SERVIC
                        TEST
                                .....  LOOP
                                                ON
                                .....  TEST
                                                SOURCE      .....  SOURCE
                                                                MAIN
    
```

Table A1-9 DS Signature Analysis Test #4

| Random Noise Generator Test Source Main Test in loop mode Jumpers in normal (N) position: All jumpers Connect U311-10 to TP15 Signature Analyzer Setup: Refer to table A1-5 +5 V Signature = H166 | | | | | |
|---|------|-----------|---------------|------|-----------|
| Component | Pin | Signature | Component | Pin | Signature |
| U208 | 9 | C139 | U313 cont. | 14 | 4F13 |
| | 10 | A38A | | 15 | 2F4F |
| | 11 | U732 | | 16 | 09HF |
| | 12 | 34P7 | | 17 | 2F4F |
| | 13 | 12C3 | U410 | 1 | 09FA |
| 14 | 460C | 2 | | 4UH7 | |
| U209 | 6 | 1764 | | 3 | 4UH7 |
| | U210 | | | 4 | 18AC |
| 5 | | | | 18AC | |
| 6 | | | P9P2 | | |
| 7 | | | P9P2 | | |
| 9 | | | 7A61 | | |
| 12 | F2CC | 15 | 09FA | | |
| 15 | 08P1 | U411 | 1 | 09FA | |
| 16 | 4H58 | | 2 | 4UH7 | |
| 19 | 1AA4 | | 3 | 4UH7 | |
| U212 | | | 4 | 18AC | |
| | | | 5 | 18AC | |
| | | 6 | P9P2 | | |
| | | 7 | P9P2 | | |
| 9 | 5FU5 | 15 | 09FA | | |
| U310 | | 2 | CO3A | | |
| | | 5 | 8CO4 | | |
| | | 6 | 05FC | | |
| | | 9 | 6678 | | |
| | | 12 | 9508 | | |
| | | 15 | 2777 | | |
| 16 | 4CP8 | U412 | 1 | 09FA | |
| 19 | HOFU | | 2 | 4UH7 | |
| U311 | | | 2 | 0000 | |
| | | | 3 | A431 | |
| | | | 11 | H166 | |
| U312 | | 1 | 23CH | | |
| | | 4 | 60FC | | |
| | | 10 | 37PF | | |
| | | 13 | UA63 | | |
| U313 | | 9 | 7753 | | |
| | | 10 | HH05 | | |
| | | 11 | 5C09 | | |
| | | 13 | 1PF9 | | |
| U413 | | 7 | P9P2 | | |
| | | 9 | 8200 | | |
| | | 15 | 09FA | | |

F. Oscilloscope Signal Waveforms

The oscilloscope plots are used for troubleshooting the A1 Digital Source. Note that all the measurements are taken with a 10:1 probe. Other notes unique to a measurement are written next to the waveform.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury.

Table A1-10 Digital Source Waveforms

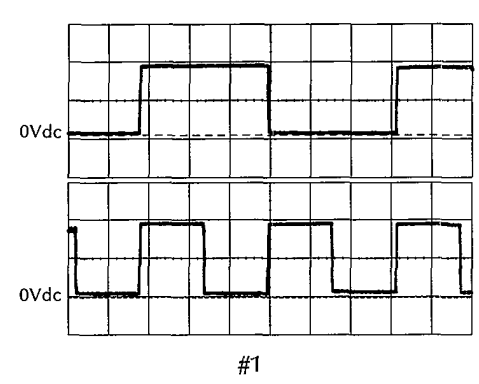
| All jumpers should be in normal position Connect ground to A1 TP1 or A1 TP15 Probe: 10:1 | | |
|---|----------------------|--|
| Press the keys as follows: <div style="display: flex; justify-content: space-around; align-items: center;"> SPCL FCTN SERVIC TEST LOOP ON </div> <div style="display: flex; justify-content: space-around; align-items: center; margin-top: 10px;"> TEST SOURCE FR END INTFCE </div> | | |
| Setup | Important Parameters | Waveform |
| <p>CNTLD and CNTCLK</p> <p>Connect CH1 to A1 TP10 Connect CH2 to A1 TP11</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 20 us/Div Trigger CH1</p> | Time Relationship |  |
| After viewing waveform, press A2 S1. | | |

Table A1-10 Digital Source Waveforms cont.

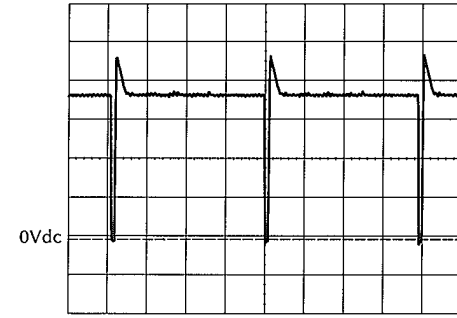
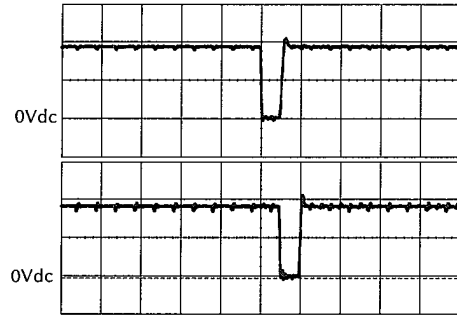
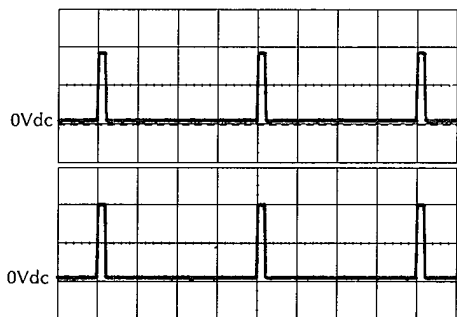
| <p>All jumpers should be in normal position</p> <p>Connect ground to A1 TP1 or A1 TP15</p> <p>Probe: 10:1</p> | | |
|---|--|--|
| Setup | Important Parameters | Waveform |
| <p>LOL</p> <p>Connect CH1 to A1 TP2</p> <p>Oscilloscope:</p> <p>CH1 V/Div 100 mV/Div</p> <p>CH1 Coupling dc</p> <p>Time/Div 1 μs/Div</p> <p>Trigger CH 1</p> | <p>Time</p> |  <p>#2</p> |
| <p>LOL and CLRL</p> <p>Connect CH1 to A1 TP2</p> <p>Connect CH2 to A1 TP3</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div</p> <p>CH2 V/Div 200 mV/Div</p> <p>CH1 Coupling dc</p> <p>CH2 Coupling dc</p> <p>Time/Div 200 ns/Div</p> <p>Trigger CH1</p> | <p>Time Relationship</p> <p>Duty Cycle</p> |  <p>#3</p> |
| <p>NCLK and NSYNC</p> <p>Connect CH2 to A1 J701-3</p> <p>Connect CH2 to A1 U11-2</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div</p> <p>CH2 V/Div 200 mV/Div</p> <p>CH1 Coupling dc</p> <p>CH2 Coupling dc</p> <p>Time/Div 2 ms/Div</p> <p>Trigger CH1</p> | <p>Time Relationship</p> |  <p>#4</p> |

Table A1-10 Digital Source Waveforms cont.

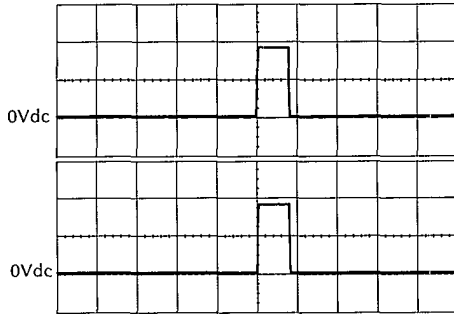
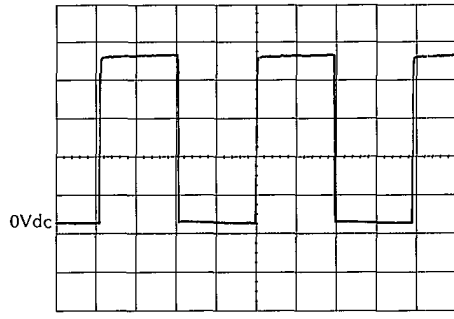
| <p>All jumpers should be in normal position</p> <p>Connect ground to A1 TP1 or A1 TP15 Probe: 10:1</p> | | |
|--|---------------------------|--|
| Setup | Important Parameters | Waveform |
| <p>BSNC and SYNC OUT</p> <p>Connect CH1 to A1 U103-12 Connect CH2 to A1 U301-1</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 500 μs/Div Trigger CH1</p> | <p>Time Relationship</p> |  <p style="text-align: center;">#5</p> |
| <p>Press the keys as follows:</p> <p>FREQ FREQ SPAN 1 kHz</p> | | |
| <p>10x Effective Sample Rate</p> <p>Connect CH1 to A1 TP12</p> <p>Oscilloscope:</p> <p>CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 10 μs/Div Trigger CH1</p> | <p>Time Duty cyle</p> |  <p style="text-align: center;">#6</p> |
| <p>After viewing waveform, press MAX SPAN.</p> | | |

Table A1-10 Digital Source Waveforms cont.

| All jumpers should be in normal position Connect ground to A1 TP1 or A1 TP15 Probe: 10:1 | | |
|---|----------------------|----------|
| Setup | Important Parameters | Waveform |
| Connect the front panel source output to external trigger and channel 1. Press the keys as follows: SOURCE . . . SOURCE LEVEL . . . 5 V . . . FIXED SINE . . . 125 Hz SELECT TRIG . . . EXT | | |
| TRIG Connect CH1 to A1 U5-7 Oscilloscope: CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 2 ms/Div Trigger CH1 | Time Duty Cycle | |

G. After-Repair Adjustments and Tests

Table A1-11 After-Repair Adjustments and Tests

| Perform the following: | Section |
|---|---------|
| Diagnostic Tests: FR END INTFCE SOURCE MAIN TEST ALL | VII |
| Adjustments: None | III |
| Performance Tests: If the noise generator subblock was repaired, perform the Source Energy Measurement test. | II |
| Operational Verification: If the phase resolution circuit was repaired, perform the Signal Channel Phase Accuracy test. If the LO Input Receiver was repaired, perform the Source Amplitude Accuracy and Flatness test. | II |

8-6 A2, A22 SYSTEM CPU/HPIB

The information in this section should be used to isolate faulty subblocks in the A2 and A22 System CPU/HPIB assemblies. All procedures assume the Fault Isolation procedures of Section VII have been used to determine which board has failed, and the Circuit Descriptions of Section VI are understood.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury.

CAUTION

Do not insert or remove any circuit board in the HP 3562A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards.

How to Use This Section

| | |
|---------------------|--|
| Start | Start troubleshooting by using figure A2-1. This procedure diagram describes the best order to perform the troubleshooting tests based on the symptoms observed. |
| Reference | For the component locator and schematic refer to Section IX. For the location of cables and boards refer to figure 4-1 in Section IV. |
| Verify | Use the oscilloscope waveforms in table A2-5 to see correct operation at various test points in the assembly. |
| After-Repair | Use table A2-6 to determine which adjustments and tests need to be done to complete instrument service. |

Troubleshooting Hints

1. Only +5 Vdc and ground are required to troubleshoot the A2 CPU/HPIB assembly. To run the A2 CPU/HPIB assembly without the rest of the instrument, put jumpers A2 J15 and A2 J16 in test (T) position.
2. The A2 CPU/HPIB can be run on an external clock by grounding A2 TP3 and connecting a TTL level, 8 MHz clock to A2 TP4.
3. Undefined failures are most likely caused by stuck bits. This is occurring if the status LEDs (A2 DS2) are a steady state value instead of changing rapidly. Go to the initial conditions test (A).

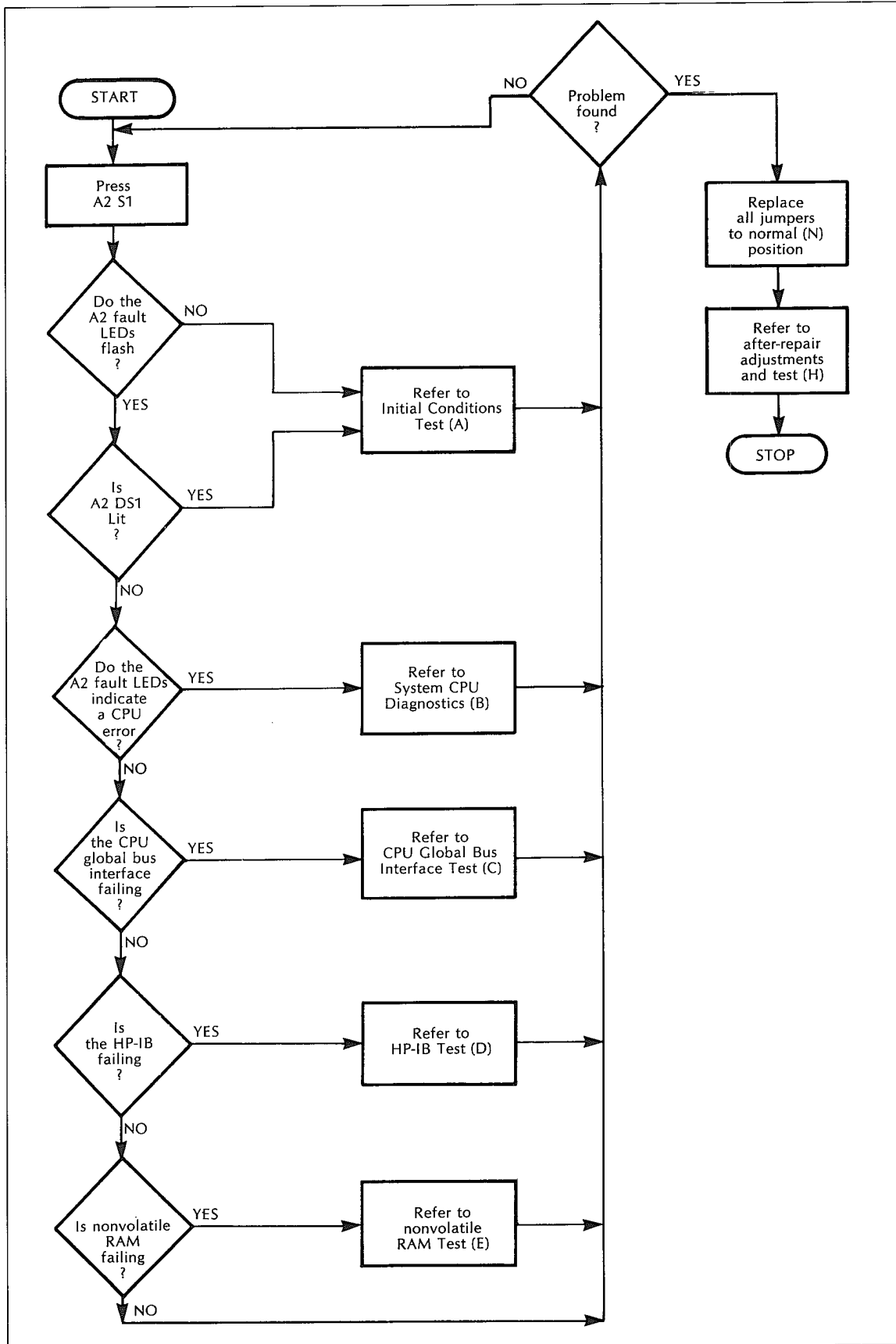


Figure A2-1 Troubleshooting Procedure Diagram

A. Initial Conditions Test

1. Disconnect the power cable from the rear panel and remove the top cover. Place the A2 CPU/HPIB on the 03562-66540 extender board.
2. Connect the power cable and press the line switch on.
3. Check the following for correct value:

| Signal | Location | Value |
|-------------|------------|--------------------------|
| +5S | A2 TP2 | +5 \pm 0.3V |
| PWRUP | A2 J15-2 | TTL logic 1 |
| PWRDNL | A2 J16-2 | TTL logic 1 |
| HALTL | A2 U100-17 | TTL logic 1 |
| RESETL | A2 U100-18 | TTL logic 1 |
| 8 mHz Clock | A2 TP5 | Refer to waveform #1 (G) |

4. If the +5S, PWRUP, or PWRDNL are not the correct values, go to paragraph 8-16, "A18 Power Supply Assembly."
5. If the cause of the failure is still not found, go to the signature tests (F).

B. System CPU Diagnostics

The CPU diagnostics do the following at power up or when the CPU is reset by pressing A2 S1:

1. Flashes the LEDs and then turns each one on starting with DS3-1 (MSB).
2. Clears the test log.
3. Stores address and contents of NVRAM.
4. Check sums the monitor ROM.
5. Exercises several system processor (U100) instructions.
6. Tests the monitor RAM by writing and reading patterns to and from it.
7. If an error was found in the RAM test, the address decoder is exercised by writing addresses to several locations and reading the contents.
8. Tests the NVRAM using a write/read/restore sequence on each memory location.
9. Tests the timer and interrupt circuits.

The CPU diagnostics stop when a fault is found and display the error code on the test LEDs (A2 DS3, A2 DS4). If no error is found on the A2 CPU/HPIB assembly, the power-up sequence continues. Use table A2-1 to determine the most likely failure causing an A2 CPU/HPIB error code.

Table A2-1 System CPU/HPIB Diagnostics

| Hex Error Code | Test Description | Hex Code Explanation | Most Likely Failure |
|-----------------------|-------------------------|---------------------------------------|-----------------------------------|
| Undefined | Initial Power Up | Low level fault | Go to Initial Conditions Test (A) |
| 01 | Monitor Rom Check sum | Upper byte failure, Lower byte passes | A2 U105 |
| 02 | Monitor Rom Check sum | Lower byte failure Upper byte passes | A2 U205 |
| 03 | Monitor Rom Check sum | Both bytes fail | Go to SA (F) |
| 04 | Monitor Rom Check sum | Both bytes pass | Go to SA (F) |
| 05 | Instruction Test | U100 test passes | Go to SA (F) |
| 06 | Instruction Test | U100 test fails | A2 U100 |
| 10 | Monitor RAM Test | High byte, MEM0L fails | A2 U110 |
| 11 | Monitor RAM Test | Low byte, MEM0L fails | A2 U210 |
| 12 | Monitor RAM Test | Both MEM0L bytes fail | A2 U110, U210 |
| 13 | Monitor RAM Test | High byte, MEM1L fails | A2 U109 |
| 14 | Monitor RAM Test | Low byte, MEM1L fails | A2 U209 |
| 15 | Monitor RAM Test | Both MEM1L bytes fail | A2 U109, U209 |
| 16 | Monitor RAM Test | High byte, MEM2L fails | A2 U107 |
| 17 | Monitor RAM Test | Low byte, MEM2L fails | A2 U207 |
| 18 | Monitor RAM Test | Both MEM2L bytes fail | A2 U107, U207 |
| 19 | Monitor RAM Test | Multiple Monitor RAM failures | Go to SA (F) |
| 1A | Monitor RAM Test | NVRAM, high byte fails | A2 U212 |
| 1B | Monitor RAM Test | NVRAM, low byte fails | A2 U211 |
| 1C | Monitor RAM Test | Both NVRAM bytes fail | A2 U212, U211 |
| C"N" | Monitor RAM Test | RAM address test fails | Line A"N" |

Table A2-1 System CPU/HPIB Diagnostics cont.

| Hex Error Code | Test Description | Hex Code Explanation | Most Likely Failure |
|----------------|--------------------------|----------------------------|------------------------|
| 0C | Timer and Interrupt Test | Unexpected timer interrupt | A2 U500, U413 |
| 0D | Timer and Interrupt Test | Timer interrupt failure | A2 U500, U413, A2 U100 |
| 0E | Timer and Interrupt Test | Timer Failure | A2 U413 |
| 0F | HP-IB Test | HP-IB Failure | HPIB subblock |

C. CPU Global Bus Interface Test

1. Press the line switch off.
2. Remove the following assemblies:
 - A5 Digital Filter
 - A7 Floating Point Processor
 - A8 Global RAM/Display
 - A9 Fast Fourier Processor
3. Press the line switch on.
4. Put A2J8, A2J12, A2J13, and A2J17 in test (T) position.
5. Repeatedly press the reset switch S1 while checking for TTL levels of the global bus drivers, latches, and control subblocks.

D. HP-IB Test

1. To test the HP-IB subblock press the HP 3562A keys as follows:

```

SPCL
FCTN      ..... SERVIC
                TEST      ..... TEST
                                   PROC

                                   ..... TEST
                                   CPU      ..... HP-IB
                                                DIAG
    
```

2. If this test passes, all signal paths and the pass through registers (A2 U112, A2 U113) are all right.

- To check the HP-IB connector press the following keys:

```

SPCL
FCTN      ..... SERVIC
                TEST      ..... LOOP ON
                                ..... TEST
                                ..... PROC
                                ..... TEST
                                ..... CPU      ..... HP-IB
                                                ..... CONNEC
    
```

- Using a small jumper, short each of the control pins to the HP-IB connector ground. When a pin is grounded, the corresponding pin shown in the display should have a dot in it.
- If this test passes, the HP-IB connector is functioning properly.

NOTE

Remove the fan (MP209) before attempting to remove the A22 HP-IB board.

E. Nonvolatile RAM Test

- Check the following for correct value:

| Location | Value |
|----------|-------------|
| U211-28 | ≥4.5V |
| U212-28 | ≥4.5V |
| U211-26 | TTL logic 1 |
| U212-26 | TTL logic 1 |

- Press the line switch off. With the power off, U211-28 should be greater than 3V.
- Connect the signature analyzer according to table A2-2.
- Check the signatures of A2 U408-6 and A2 U305-15, they should be the same.

F. CPU Signature Analysis Tests

These tests are used when the previous tests fail to find the problem.

- Disconnect power cable.
- Put the following jumpers in test (T) position:
A2J4, A2J5, A2J6, A2J7, A2J9, A2J10, A2J18
- Put A2 J11 and A2 J14 in position "2".

4. Connect the signature analyzer according to table A2-2.

Table A2-2 CPU Signature Analyzer Setup

| Signal | Polarity | Connection |
|--------|---------------|------------|
| Ground | | A2 J2-1 |
| Clock | Positive edge | A2 J2-3 |
| Stop | Negative edge | A2 J2-4 |
| Start | Negative edge | A2 J2-5 |

5. Connect the power cable and press the line switch on.

Table A2-3 CPU Signature Analysis Test #1

| <p>Address Test Jumpers in test (T) position: A2J4, A2J5, A2J6, A2J7, A2J9, A2J10, A2J18 Jumpers in position "2": A2J11, A2J14 Jumpers in normal (N) position: A2J1, A2J8, A2J17, A2J12, A2J13 Jumpers in either normal or test position: A2J15, A2J16 Signature Analyzer Setup: Refer to table A2-2 +5 V Signature = 0001</p> | | | | | | |
|---|-----|-----------|-----------|------|-----------|------|
| Component | Pin | Signature | Component | Pin | Signature | |
| U100 | 29 | UUUU | U100 | 37 | HC89 | |
| | 30 | 5555 | | 38 | 2H70 | |
| | 31 | CCCC | | 39 | HPPO | |
| | 32 | 7F7F | | 40 | 1293 | |
| | 33 | 5H21 | | 41 | HAP7 | |
| | 34 | OAF8 | | 42 | 3C96 | |
| | 35 | UPFH | | 43 | 3827 | |
| | 36 | 52F8 | | 44 | 755U | |
| <p>Put jumper J1 in position "1". It takes about 10s for each of the following signatures to stabilize. +5 V Signature = 6PCP</p> | | | | | | |
| Component | Pin | Signature | Component | Pin | Signature | |
| U100 | 45 | 2595 | U305 | 14 | 0000 | |
| | 46 | 1F8F | | 15 | HUHA | |
| | 47 | U97F | | 16 | 1582 | |
| | 48 | 5A34 | | 17 | AC4F | |
| | 49 | 6PCP | | 18 | 012U | |
| | 50 | 91FC | | U606 | 13 | 443U |
| | 51 | 3CPF | | | 15 | 6PCP |
| U305 | 52 | A70F | 16 | AP18 | | |
| | 10 | 4CAH | 17 | A52A | | |
| | 11 | 2H3U | 18 | UA2U | | |
| | 12 | 3HFO | | | | |
| | 13 | 807A | | | | |

6. If the signatures in table A2-3 are incorrect, check that A2 U100 pins 12, 13, 21, 22, 23, 24, and 25 are a TTL logic high.
7. Put A2 J1 in position "2". It takes about 10s for each of the signatures in table A2-4 to stabilize.

Table A2-4 CPU Signature Analysis Test #2

| Monitor ROM Test | | | | | |
|--|------------|------------------|------------------|------------|------------------|
| Jumpers in test (T) position: A2J4, A2J5, A2J6, A2J7, A2J9, A2J10, A2J18 | | | | | |
| Jumpers in position "2": A2J1, A2J11, A2J14 | | | | | |
| Jumpers in normal (N) position: A2J8, A2J17, A2J12, A2J13 | | | | | |
| Jumpers in either normal or test position: A2J15, A2J16 | | | | | |
| Signature Analyzer Setup: Refer to table A2-2 | | | | | |
| +5 V Signature = 6PCP | | | | | |
| Component | Pin | Signature | Component | Pin | Signature |
| U105 | 11 | 9UUU | U205 | 11 | 35H3 |
| | 12 | FH2H | | 12 | 6000 |
| | 13 | HHHH | | 13 | 2C18 |
| | 15 | P488 | | 15 | 6300 |
| | 16 | F7CH | | 16 | P9F7 |
| | 17 | H1HA | | 17 | 278F |
| | 18 | CF33 | | 18 | A936 |
| | 19 | F108 | | 19 | 13C9 |

G. Oscilloscope Signal Waveforms

The oscilloscope plots are used for troubleshooting the A2 CPU/HPIB. Note that all the measurements are taken with a 10:1 probe. Other notes unique to a measurement are written next to the waveform.

Table A2-5 CPU Signal Waveforms

| Remove Power Jumpers in normal (N) position: All jumpers Connect ground to A2 TP1 Probe: 10:1 Power On | | |
|---|----------------------|-----------|
| Setup | Important Parameters | Waveform |
| <p>8 MHz Clock</p> <p>Connect CH1 to A2 TP5</p> <p>Oscilloscope: Bandwidth Limit: ON Mode A CH1 V/Div 50 mV/Div</p> <p>CH1 Coupling dc</p> <p>Time/Div 50 ns/Div Trigger CH1</p> | Time Pulse shape | <p>#1</p> |
| Press A2 S1 switch to see the waveform #2. DTACKL and ASL will stop changing for a short time (≈2s). | | |
| <p>DTACKL, ASL</p> <p>Connect CH1 to A2 U100-10 Connect CH2 to A2 U100-6</p> <p>Oscilloscope: Bandwidth Limit: ON Mode A & B CH1 V/Div 100 mV/Div CH2 V/Div 100 mV/Div</p> <p>CH1 Coupling dc CH2 Coupling dc Time/Div 200 ns/Div Trigger CH1</p> | Time relationship | <p>#2</p> |

H. After-Repair Adjustments and Tests**Table A2-6 After-Repair Adjustments and Tests**

| Perform the following: | Section |
|-------------------------------|----------------|
| Diagnostic Tests: TEST ALL | VII |
| Adjustments: None | |
| Performance Tests: None | |

8-7 A3 PROGRAM ROM

The information in this section should be used to isolate faulty subblocks on the A3 Program ROM assembly. All procedures assume that the Fault Isolation procedures of Section VII were used to determine that this board has failed and that the Circuit Descriptions of Section VI are understood.

WARNING

Service procedures described in this section are performed with protective covers removed and power applied. Hazardous voltages in these circuits can cause personal injury if contacted.

CAUTION

Do not insert or remove any circuit board in the HP 3562A while power is on. Power transients caused by insertion or removal may damage the circuit boards.

How to Use This Section

| | |
|---------------------|---|
| Start | Start troubleshooting with part A, Program ROM Diagnostics. |
| Reference | Refer to Section IX for the component locators and schematics. refer to figure 4-1 in Section IV for location of cables and boards. |
| After-Repair | Use table A3-3 to determine which adjustments and tests need to be performed to complete instrument service. |

Troubleshooting Hint

The ROM board is very sensitive to changes in +5 V. Check this voltage before proceeding with the rest of this section.

A. Program ROM Diagnostics

The PROG ROM test runs at turn-on. Table A3-1 lists and explains the A2 LED annunciations of test failures. The test sequence follows:

1. Verifies system bus. This is done by echoing data from the FFT board. If the FFT board is not present, the system bus cannot be verified.
2. Verifies ROM bus. The system CPU reads the contents of two locations in the lowest ROM pair and verifies that they are correct. One number is the complement of the other so that all ROM bus lines are toggled. If this test fails, the LED annunciations also indicate whether the system bus was verified.

3. Verifies check ROM. The correct checksum results for all ROMs are stored at designated locations in the last ROM pair. This step reads and verifies the contents of those locations. If this test fails, one or both of the last ROM pair are the likely cause.
4. Checksums high and low bytes of ROM. The checksum results are compared to the correct values stored in memory.

Table A3-1 A2 LED Display Codes

| Test Failed | LED Bank | Probable Failure | Other Information |
|-------------|----------|---|---------------------------------|
| 1 | 87 | System Bus failure, high byte | |
| 1 | 88 | System Bus failure, low byte | |
| 1 | 89 | System Bus failure, both bytes | |
| 2 | 8A | ROM Bus failure, low byte * | System bus good |
| 2 | 8B | ROM Bus failure, high byte * | |
| 2 | 8C | ROM Bus failure, both bytes * | |
| 2 | 7A | ROM Bus failure, low byte | No information about system bus |
| 2 | 7B | ROM Bus failure, high byte | |
| 2 | 7C | ROM Bus failure, both bytes | |
| 3 | 5A | Check ROM failure, low byte | ROM bus good |
| 3 | 5B | Check ROM failure, high byte | |
| 3 | 5C | Check ROM failure, both bytes | |
| 4 | 40 to 53 | ROM IC failure, low byte ** | |
| 4 | 20 to 33 | ROM IC failure, high byte ** | |
| 4 | 60 to 73 | ROM IC failure, both bytes *** | |
| 4 | 84 | ROM ICs, multiple failures high byte | System bus good |
| 4 | 85 | ROM ICs, multiple failures low byte | |
| 4 | 86 | ROM ICs, multiple failures both bytes | |
| 4 | 8D | No ROM passes checksum, system data bus good; check system address bus. | |
| 4 | 1F | Program ROM and System Bus tests pass. This is a normal annunciation. | |

* This failure code may result from defective A8 U101 or A8 U201 as well as from a ROM data bus problem.

** See table A3-2 to decode IC number.

*** It is unlikely that both ICs in a ROM pair are faulty. The most likely cause of this failure is a faulty IC enable signal.

Table A3-2 ROM Chip Codes

| A2 DS3 | A2 DS4 | Suspect IC | A2 DS3 | A2 DS4 | Suspect IC |
|--------|--------|------------|--------|--------|------------|
| 4 | 0 | U101 | 2 | 0 | U201 |
| | 1 | U102 | | 1 | U202 |
| | 2 | U103 | | 2 | U203 |
| | 3 | U104 | | 3 | U204 |
| | 4 | U105 | | 4 | U205 |
| | 5 | U106 | | 5 | U206 |
| | 6 | U107 | | 6 | U207 |
| | 7 | U108 | | 7 | U208 |
| | 8 | U109 | | 8 | U209 |
| | 9 | U110 | | 9 | U210 |
| | A | U111 | | A | U211 |
| | B | U112 | | B | U212 |
| | C | U113 | | C | U213 |
| | D | U114 | | D | U214 |
| | E | U115 | | E | U215 |
| | F | U116 | | F | U216 |
| 5 | 0 | U117 | 3 | 0 | U217 |
| | 1 | U118 | | 1 | U218 |
| | 2 | U119 | | 2 | U219 |
| | 3 | U120 | | 3 | U220 |

B. After-Repair Adjustments and Tests

Table A3-3 After-Repair Adjustments and Tests

| Perform the following: | Section |
|-------------------------------|---------|
| Diagnostic Tests: Test All | VII |
| Adjustments: None | |
| Performance Tests: None | |

8-8 A4 LOCAL OSCILLATOR

The information in this section should be used to isolate faulty subblocks in the A4 Local Oscillator (LO). All procedures assume the Fault Isolation procedures of Section VII have been used to determine which board has failed, and the circuit descriptions of Section VI are understood.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury.

CAUTION

Do not insert or remove any circuit board in the HP 3562A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards.

How to Use This Section

| | |
|---------------------|---|
| Start | The primary troubleshooting method for the LO assembly is to use the self-tests to determine which subblocks and possible components are failing. Signature analysis is then used to troubleshoot the individual subblocks suspected of failing. Start troubleshooting by using part A, "Local Oscillator Diagnostics". |
| Reference | For the component locator and schematic refer to Section IX. For the location of cables and boards refer to figure 4-1 in Section IV. |
| Verify | Use the oscilloscope waveforms in table A4-5 to see correct operation at various test points in the assembly. |
| After-Repair | Use table A4-6 to determine which adjustments and tests need to be done to complete instrument service. |

Troubleshooting Hints

1. If the LO functional tests pass, but the 'Output Sine Check' (7-8, part E) fails, start troubleshooting with the LO Output Buffer (U54). This output buffer is not tested by the self-tests.

A. Local Oscillator Diagnostics

When the LO FUNCTN key is pressed, the LO functional self-tests cause the phase accumulator and the sine ROMs to output a value to the A2 System CPU. The system CPU compares the value to a known good value. The tests are executed twice. The first execution of the tests substitutes clock signals (Int Clock) generated in the LO assembly for the external clock (Ext Clock) signals SYNC2 and 10.24 MHz. The second execution of the self-tests uses the external clocks. Perform the LO functional test by pressing the HP 3562A keys as follows:

```

SPCL
FACTN  . . . . . SERVIC
                TEST  . . . . . TEST
                                SOURCE . . . . . LO
                                                FUNCTN

```

Use the following descriptions to help isolate the failure:

1. LO Interface Test

This test verifies the System Bus Interface subblock by reading data to and from the PIA (A4 U36). If 'LO Interface Test FAILS' is displayed, start troubleshooting with components A4 U36, U32, U33, U37, and U24 in the System Bus Interface Subblock.

LO Timeout 'messages'

An LO timeout message can be caused by one of several components failing in the system bus interface, control, and timing circuits. However, the probable cause of the failure is A4 U36, and U37 in the system bus interface or A4 U55, U56, U68, U46, U51, and U14 in the control and timing circuits.

2. Internal and External Clocks

The external clock test uses the 10.24 MHz clock from the A31 Trigger and the SYNC2 from the A6 Digital Filter (normal operating clocks). The internal clock test substitutes these clocks for clocks generated on the LO assembly. The internal clocks are significantly slower than the external clock signals.

If the failure message is 'LO Ext Clock Phase Values FAILS', 'LO Ext Clock Output Values FAILS' and the other LO self-tests pass, the external clocks are failing. Start troubleshooting with the SYNC2 and 10.24 MHz input circuits (A4 U75, U68). This failure can also be caused by timing problems throughout the assembly since the external signals are at a higher frequency than the internal signals.

If the failure message is 'LO Int Clock Phase Values FAILS', 'LO Int Clock Output Values Fails' and the other LO self-tests pass, the internal clocks are failing. If this occurs, the possible failing components are A4 U32 and U36 in the system bus interface, A4 U68, U72, U74, and U75 in the control and timing circuits.

If the LO Interface Test passes and both the external and internal clock tests fail, the problem is probably not in the system bus interface or the control and timing circuits.

3. Phase Value Failures

The phase value is read from the phase latches (A4 U23, U27). If the phase value fails, the output value is probably failing too. (However, if the failure message is 'LO Int Clock Phase Values FAILS', 'LO Ext Clock Phase Values FAILS' and the other LO self-tests pass, the possible cause of the failure is the phase latches A4 U23 and U27, or A4 U47, U52, U32, U36 in the system bus interface.) If the phase value fails, use signature analysis patterns LO DSA PATT 1 and LO DSA PATT 2 (in part B) as follows to isolate the failure:

LO DSA PATT 1

- a. Start by checking the phase accumulator outputs (A4 U5).
- b. If the phase accumulator output signatures are correct, check A4 U22 and U26.
- c. Check A4 U68, U56, and U58 in the control and timing circuits. Then check A4 U19, U31, and U36 pins 2, 3, 4, 10 through 19 in the system bus interface.
- d. If any of the signatures in step c are wrong, check the input signals to the components. If the inputs to the components are correct, the failure is most likely caused by the phase accumulator.

LO DSA PATT 2

The phase accumulator feeds its output back to the input. LO DSA PATT 2 breaks this feed back loop. Start by checking the signatures of A4 U11 and U16. Check the signatures of the other components in the phase accumulator by moving forward and back from A4 U11 and U16.

4. Output Value Failures

The output value in the exclusive OR of the SINE and COS outputs which are shifted into the LO output buffers (A4 U41, U42). If the failure message is 'LO Int Clock Output Values FAILS', 'LO Ext Clock Output Values FAILS', and the other LO functional tests pass, the probable cause of the failure is in the sine ROM, interpolator and adder, or the LO output buffers. Check the signatures at the following points using LO DSA PATT 1:

- a. A4 TP16 (NDAT), A4 TP23 (SINE), A4 TP24 (COS)
- b. Adder Outputs: A4 U39 pins 8, 9, 11, and 12.
- c. Sine ROM Outputs: A4 U39 pins 2, 4, 16, and 18
- d. Interpolator Outputs: A4 U39 pins 1, 3, 17, 19

NOTE

If the LO functions properly in all modes but fails the output value test, the test circuits may be failing. Check A4 U41, U42, U48, U59, and U69.

B. A4 Signature Analysis Tests

Use these tests to isolate a failure on the LO assembly. Only the components in failing subblocks need to be tested. The symbol '(T)' refers to a signal continually changing between TTL level high and TTL level low.

1. Press the line switch off.
2. Connect the Signature Analyzer as follows:

Table A4-1 A4 Signature Analyzer Setup

| Signal | Polarity | Connection |
|--------|---------------|------------|
| Ground | | A4 J1-1 |
| Clock | Positive edge | A4 J1-3 |
| Stop | Negative edge | A4 J1-4 |
| Start | Positive edge | A4 J1-5 |

3. Press the line switch on.
4. Signature Analysis Test -1 Setup:
 - a. Press the keys as follows:

```

SPCL
FCTN      ..... SERVICE
          TEST          ..... LOOP
                              ON
                              ..... TEST
                              SOURCE ..... LO DSA
                                      PATT 1
    
```

Table A4-2 A4 Signature Analysis Test #1

| LO DSA PATT 1 | | | | | |
|---|------|-----------|-----------|------|-----------|
| Signature Analyzer Setup: Refer to table A4-1 | | | | | |
| +5 V Signature = P43F | | | | | |
| Component | Pin | Signature | Component | Pin | Signature |
| TP16 | — | 732U | Δ U20 | 11 | P1A2 |
| TP23 | — | CP34 | | 12 | 9149 |
| TP24 | — | OHC3 | | 13 | P43P |
| | | | | 15 | 9C68 |
| U5 | 2 | 649U | 16 | 12C0 | |
| | 5 | 5101 | 17 | 2H8P | |
| | 6 | 2806 | 18 | 6C7P | |
| | 9 | 1197 | 19 | 6PA1 | |
| | 12 | 3FFA | | | |
| | 15 | 9HPU | | | |
| U13 | 16 | 9H32 | U21 | 12 | 4373 |
| | 17 | PHHC | | 13 | U981 |
| | 1 | OCP9 | | 14 | 7F65 |
| | 2 | 66PC | | 15 | 0097 |
| | 3 | 1F81 | | 16 | OPF4 |
| | 4 | 3PA1 | 17 | ASAP | |
| | 5 | 37C8 | 18 | P32O | |
| | 6 | O42H | 19 | 8197 | |
| | 7 | O3AO | | | |
| | 11 | A35C | U22 | 12 | 9148 |
| 12 | 882A | 13 | | 6303 | |
| 13 | 3P1H | 14 | | 46FU | |
| 14 | A13P | 15 | | 3CC9 | |
| 17 | 756P | 16 | | FF39 | |
| | | 17 | | 4795 | |
| U19 | 2 | OFO6 | U24 | 18 | 8964 |
| | 3 | 392U | | 19 | 0U64 |
| | 4 | 06UC | | 11 | P83A |
| | 5 | 3CP5 | | 12 | HH13 |
| | 6 | 34H8 | | 13 | P2F7 |
| | 7 | 9631 | | 14 | HUH9 |
| | 8 | 45FP | | 15 | HOP4 |
| | 9 | C4A9 | | 16 | 72OH |
| | 12 | 6022 | 17 | A1U2 | |
| | 13 | 14U8 | 18 | 5O95 | |
| | 14 | 698A | U25 | 15 | 5A75 |
| | 15 | AC37 | | 16 | H2F9 |
| | 17 | F792 | | 18 | FHH7 |
| | 18 | U534 | | 19 | 69AO |
| 19 | AC37 | | | | |

Δ See backdating.

Table A4-2 A4 Signature Analysis Test #1 cont.

| Component | Pin | Signature | Component | Pin | Signature | |
|-----------|----------|-----------|-----------|----------|-----------|----------|
| U26 | 12 | 0C91 | U36 | 2 | 3UAH | |
| | 13 | 3069 | | 3 | 19H7 | |
| | 14 | 2271 | | 4 | A616 | |
| | 15 | 4C74 | | 6 | 1903 | |
| | 16 | UUH4 | | 7 | H1F3 | |
| | 17 | 199A | | 8 | 5263 | |
| | 18 | 2278 | | 9 | 9AA3 | |
| | 19 | 14UC | | 10 | 111U | |
| | U28 | 11 | | U793 | 11 | P43F (T) |
| 12 | | PFH8 | | 12 | CCHF | |
| 13 | | HPF8 | | 13 | 5UP0 | |
| 14 | | 6OH9 | | 14 | 23H0 | |
| 15 | | 1195 | | 15 | 4C0A | |
| 16 | | 34H7 | | 16 | 93A8 | |
| 17 | | 8H5H | | 18 | 8053 | |
| 18 | | 5H46 | | 19 | 23HO | |
| Δ U29 | 11 | UH9P | | U39 | 1 50CA | |
| | 12 | HF11 | | | 2 | A00F |
| | 13 | 11C0 | | | 3 | CH44 |
| | 15 | 6582 | 4 | | 1C6P | |
| | 16 | P104 | 5 | | 6FF9 | |
| | 17 | 4791 | 8 | | 7U57 | |
| | 18 | 09AF | 9 | | A5U0 | |
| U31 | 3 | 8HC6 | 11 | | U9U7 | |
| | 6 | 8U6F | 12 | | 911F | |
| | 10 | 4U0C | 13 | | CU33 | |
| | 15 | 1622 | 14 | | APUA | |
| U32 | 11 | U21P | 15 | | 5188 | |
| | 12 | 0000 (T) | 16 | | F68U | |
| | 13 | 0000 (T) | 17 | | 2139 | |
| | 14 | P43F (T) | 18 | | P44H | |
| | 15 | P43F (T) | 19 | | 4756 | |
| | 16 | P43F (T) | U41 | | 1 45FP | |
| | 17 | 0000 (T) | | | 2 | 9631 |
| 18 | 0000 (T) | 3 | | | 34H8 | |
| U33 | 11 | P43F (T) | | 4 | 3CP5 | |
| | 12 | P43F (T) | | 5 | 06UC | |
| | 13 | 0000 (T) | | 6 | 392U | |
| | 14 | 0000 (T) | | 7 | OFO6 | |
| | 15 | P43F (T) | | 11 | P43F (T) | |
| | 16 | P43F (T) | | 12 | 0000 (T) | |
| 17 | 0000 (T) | 13 | | 0000 (T) | | |
| | | | | 14 | HFP1 | |
| | | | | 15 | C4A9 | |

Δ See backdating.

Table A4-2 A4 Signature Analysis Test #1 cont.

| Component | Pin | Signature | Component | Pin | Signature | |
|-----------|------|-----------|-----------|------|-----------|------|
| U42 | 1 | 6961 | U55 | 1 | 8956 | |
| | 2 | HOPC | | 2 | 2278 | |
| | 3 | U5A9 | | 3 | 9398 | |
| | 4 | 84P5 | | 4 | 96A7 | |
| | 5 | 3AU4 | | 5 | O6A8 | |
| | 6 | O8P4 | | 6 | OF8F | |
| | 7 | 13AU | | 7 | 2AU6 | |
| | 14 | C387 | | 9 | 14UC | |
| 15 | C97A | 11 | | 4COA | | |
| U43 | 12 | AF9P | | 13 | 373H | |
| | 13 | FH7P | | 14 | 7261 | |
| | 14 | 9UO8 | | 15 | C1PO | |
| | 15 | 4AP2 | | 16 | 8944 | |
| | 16 | 3422 | | U56 | 1 | 96A7 |
| | 17 | 16H3 | | | 2 | 9398 |
| | 18 | 4U84 | | | 3 | 2AU6 |
| 19 | A53U | 4 | 0F8F | | | |
| U44 | 12 | AA1H | 5 | | 06A8 | |
| | 13 | 6HHH | 6 | | 4C0A | |
| | 14 | OF89 | 7 | | H6UC | |
| | 15 | 6UH9 | 8 | | 8956 | |
| | 16 | 2157 | 12 | | 8053 | |
| | 17 | OA73 | 13 | | 1H3U | |
| | 18 | 84AO | 14 | | 1625 | |
| 19 | 7U65 | 15 | 8P75 | | | |
| U48 | 12 | OA5H | 16 | | 5P6P | |
| | 13 | A39C | 17 | | 280C | |
| | 14 | 52PH | 18 | | U192 | |
| | 15 | C7AP | 19 | | 165H | |
| | 16 | OHUU | U58 | | 2 | 9398 |
| | 17 | OAA9 | | | 3 | 96A7 |
| | 18 | F6UH | | | 4 | 648H |
| 19 | 7874 | 5 | | P732 | | |
| U49 | 12 | 553C | | 6 | 4UAF | |
| | 13 | 569U | | 7 | 4331 | |
| | 14 | 2FF3 | | 8 | HH5P | |
| | 15 | 22A3 | | 9 | 64C9 | |
| | 16 | 7FPF | | 12 | A451 | |
| | 17 | AAAC | | 13 | 5271 | |
| | 18 | OOU4 | | 14 | A1C7 | |
| 19 | UP9H | 15 | | 0P31 | | |
| U53 | 5 | A451 | | 16 | C6UU | |
| | 6 | UFAC | | 17 | 6217 | |
| U54 | 2 | OP31 | | 18 | 9C28 | |
| | 5 | A1C7 | | 19 | PUP2 | |
| | 6 | 732U | | U62 | 5 | 5271 |
| | | 6 | | | 64CO | |

Table A4-2 A4 Signature Analysis Test #1 cont.

| Component | Pin | Signature | Component | Pin | Signature |
|-----------|------|-----------|-----------|------|-----------|
| U63 | 2 | 9C28 | U71 | 2 | 64C0 |
| | 3 | 64C9 | | 3 | P43F |
| | 6 | 6217 | | 5 | CP34 |
| U68 | 2 | 9398 | | 9 | OHC3 |
| | 3 | 96A7 | | 11 | P43F (T) |
| | 4 | 64C9 | 12 | UFAC | |
| | 12 | FU1H | U72 | 1 | A7A3 |
| | 13 | 2UF6 | | 2 | P43F |
| | 14 | 101U | | 5 | 4PUP |
| | 15 | 648H | U75 | 5 | A1C7 |
| | 16 | P732 | | 7 | OP31 |
| | 17 | 4UAF | | 9 | C6AH |
| | 18 | 4331 | | | |
| 19 | HH5P | | | | |

6. Signature Analysis Test -2 Setup:

a. Press the keys as follows:

```

SPCL
FCTN      ..... SERVICE
           TEST           ..... LOOP
                               ON
                               ..... TEST
                               SOURCE ..... LO DSA
                                       PATT 2
    
```

Table A4-3 A4 Signature Analysis Test #2

| LO DSA PATT 2 Signature Analyzer Setup: Refer to table A4-1 +5 V Signature = AFA7 | | | | | |
|---|------|-----------|-----------|------|-----------|
| Component | Pin | Signature | Component | Pin | Signature |
| U1 | 2 | 0831 | U8 | 5 | 4F8H |
| | 5 | A46A | | 7 | 28F8 |
| | 6 | A143 | | 9 | 035U |
| | 9 | 8F4A | | 11 | APAC |
| | 12 | 988F | | | |
| U2 | 15 | 56P6 | U9 | 4 | 6494 |
| | 16 | 5PCA | | 7 | P380 |
| | 19 | 8F4A | | 9 | 83UC |
| | | | | 12 | P27U |
| U3 | 3 | AFA7 (T) | U10 | 5 | 1PCC |
| | 5 | F346 | | 7 | 1A75 |
| | 7 | 16CP | | 9 | U699 |
| | 9 | ACH5 | | 11 | 14H2 |
| | 11 | 7F34 | U11 | 1 | A143 |
| | 14 | 8627 | | 4 | C2P2 |
| 15 | 25FA | 9 | 161P | | |
| U4 | 5 | U3CA | 10 | 897A | |
| | 7 | 7H68 | 13 | 0U63 | |
| | 9 | 48A0 | U16 | 1 | A037 |
| | 11 | 7F34 | | 4 | 2A68 |
| | | 9 | | 06PH | |
| | | 10 | | 485A | |
| U5 | 4 | APU2 | 13 | 3HFA | |
| | 7 | 52C8 | U19 | 12 | 1CO6 |
| | 9 | 94AP | | 13 | U75F |
| | 12 | P27U | | 14 | 8U5C |
| | | 15 | | OHOF | |
| | | 17 | | 0043 | |
| | | 18 | | CUA7 | |
| | | 19 | | OHOF | |
| U6 | 2 | 0UHU | | U57 | 4 |
| | 5 | 356P | 7 | | 25FA |
| | 6 | 9P67 | 9 | | PUFH |
| | 9 | 3845 | 12 | 8PUA | |
| | 12 | F6F8 | U65 | 13 | 8627 |
| | 15 | 6HF1 | | 14 | A57H |
| | 16 | 60PA | | | |
| | 19 | 3845 | | | |
| | | | | | |
| U7 | 5 | U824 | | | |
| | 7 | 5966 | | | |
| | 9 | 8051 | | | |
| | 11 | APAC | | | |

C. Oscilloscope Signal Waveforms

The oscilloscope plots are used for troubleshooting the A4 Local Oscillator. Note that all the measurements are taken with a 10:1 probe. Other notes unique to a measurement are written next to the waveform.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury.

Table A4-4 LO Signal Waveforms

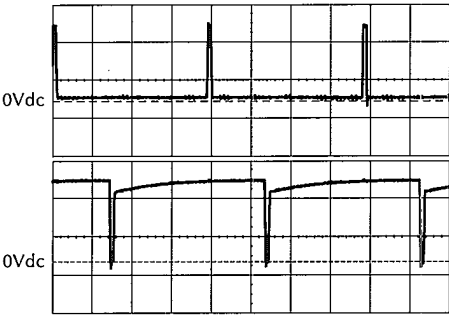
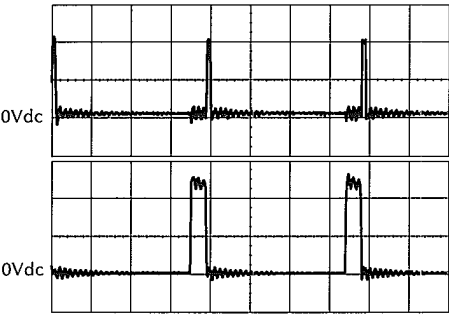
| Probe: 10:1 | | |
|--|--|--|
| Setup | Important Parameters | Waveform |
| <p>SYNC2 and COS</p> <p>Connect CH1 to A4 TP8 Connect CH2 to A4 TP24</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div</p> <p>CH1 Coupling dc CH2 Coupling dc Time/Div 1 μs/Div Trigger CH1</p> | <p>Time relationship</p> <p>Pulse shapes</p> |  <p style="text-align: center;">#1</p> |
| <p>SYNC2 and NLD</p> <p>Connect CH1 to A4 TP8 Connect CH2 to A4 TP17</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div</p> <p>CH1 Coupling dc CH2 Coupling dc</p> <p>Time/Div 1 μs/Div Trigger CH1</p> | <p>Time relationship</p> |  <p style="text-align: center;">#2</p> |

Table A4-4 LO Signal Waveforms cont.

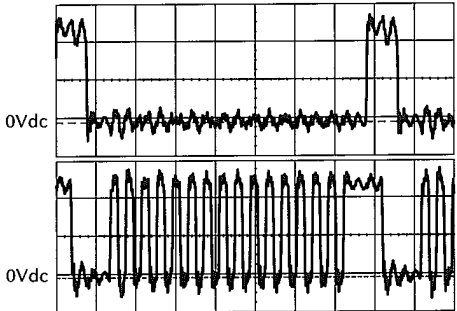
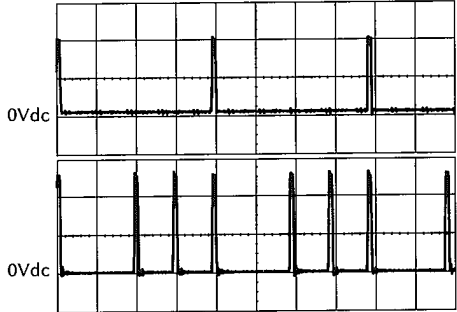
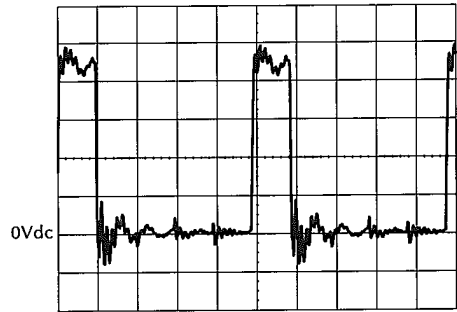
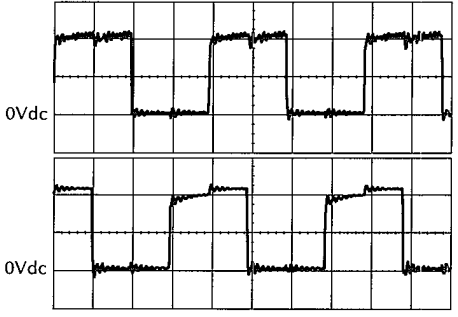
| Probe: 10:1 | | |
|--|--------------------------|--|
| Setup | Important Parameters | Waveform |
| <p>NLD and NDCK</p> <p>Connect CH1 to A4 TP17 Connect CH2 to A4 TP14</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div</p> <p>CH1 Coupling dc CH2 Coupling dc Time/Div 500 ns/Div Trigger CH1</p> | <p>Time relationship</p> |  <p>#3</p> |
| <p>SYNC2 and LDOUT</p> <p>Connect CH1 to A4 TP8 Connect CH2 to A4 TP11</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div</p> <p>CH1 Coupling dc CH2 Coupling dc</p> <p>Time/Div 1 μs/Div Trigger CH1</p> | <p>Time relationship</p> |  <p>#4</p> |
| <p>E</p> <p>Connect CH1 to A4 TP2</p> <p>Oscilloscope:</p> <p>CH1 V/Div 100 mV/Div CH1 Coupling dc Time/Div 200 ns/Div Trigger CH1</p> | <p>Time</p> |  <p>#5</p> |

Table A4-4 LO Signal Waveforms cont.

| <i>Probe: 10:1</i> | | |
|---|--------------------------|--|
| Setup | Important Parameters | Waveform |
| <p>S1 and S2</p> <p>Connect CH1 to A4 TP21 Connect CH2 to A4 TP22</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div</p> <p>CH1 Coupling dc CH2 Coupling dc</p> <p>Time/Div 1 μs/Div</p> <p>Trigger CH1</p> | <p>Time relationship</p> |  <p style="text-align: center;">#6</p> |

D. After-Repair Adjustments and Tests

Table A4-5 After-Repair Adjustments and Tests

| Perform the following: | Section |
|---|------------|
| <p>Diagnostic Tests:</p> <p style="padding-left: 40px;">LO FUNCTN</p> <p style="padding-left: 40px;">TEST ALL</p> | <p>VII</p> |
| <p>Adjustments:</p> <p style="padding-left: 40px;">None</p> | <p>III</p> |
| <p>Performance Tests:</p> <p style="padding-left: 40px;">None</p> | <p>II</p> |
| <p>Operational Verification:</p> <p style="padding-left: 40px;">None</p> | <p>II</p> |

8-9 A5, A6 Digital Filter and Digital Filter Controller

The information in this section should be used to isolate faulty subblocks in the A5 Digital Filter and the A6 Digital Filter Controller. These two boards, referred to as the Digital Filter Assembly (DFA), work together to filter the input signal before it is stored in Global RAM. All procedures assume the Fault Isolation procedures of Section VII have been used to determine which board has failed and the Circuit Descriptions of Section VI are understood.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury.

CAUTION

Do not insert or remove any circuit board in the HP 3562A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards.

How to Use This Section

| | |
|---------------------|---|
| Start | Begin with troubleshooting hint -1. If the failure is determined to be on the DFA, perform the DFA diagnostic self-tests while keeping track of the subblocks that are verified and the signals that are failing. |
| Procedure | Check the clocks and signals listed in the 'Signal Verification' paragraph. After determining the possible defective subblocks, use signature analysis to isolate the failure. |
| Reference | Refer to Section IX for the component locator and schematic. Refer to figure 4-1 in Section IV for the location of cables and boards. |
| After-Repair | Use table A5-8 to determine which adjustments and tests need to be done to complete instrument service. |

Troubleshooting Hints

- Jumpers are provided to cross-connect the incoming serial bit streams from the ADC boards. Refer to the A5 schematic in Section IX. When A5 J2 and A5 J3 are placed in their test position (T), input data from ADC1 is routed to the channel two digital filter block and input data from ADC2 is routed to the channel one digital filter block. These jumpers may be used to aid in fault isolation.
- If a channel is continuously overloading, start troubleshooting the Overload Detect subblock on the A5 assembly.

3. If full-span functions correctly but zoom mode fails on both channels, start troubleshooting the LO Signal/Constant Select subblock.
4. If freerun measurements operate correctly, but triggered measurements do not, start troubleshooting the Trigger Control PAL (A6 U409) and the Start/Stop Control PLA (A6 U309).
5. If all the DFA diagnostic tests indicate no failure, yet the instrument still has a problem making a measurement, run the ADC diagnostic called DIGITAL TEST. This test provides data to the DFA from the instrument front end, performs a measurement, and analyzes the results. This allows you to test the input data bit stream from the ADC boards. The key strokes used to access this diagnostic are:

```

PRESET  ..... RESET

SPCL FCTN
          ..... SERVIC
                TEST  ..... TEST
                          INPUT ..... ADC ..... DIGITAL
                                                    TEST
    
```

A. DFA Diagnostics

The diagnostic tests for the Digital Filter Assembly allow you to test groups of circuits to further isolate a problem. A subset of the DFA diagnostic tests run when the instrument power is turned ON, during SELF TEST, and during TEST ALL. Display the DFA diagnostic test menu using the following sequence of keystrokes:

```

PRESET  ..... RESET

SPCL FCTN
          ..... SERVIC
                TEST  ..... TEST PROC
                          ..... TEST DFA
    
```

The menu now contains the following entries of DFA diagnostics:

```

DFA FUNCTN
FILTER TEST
LOCAL BUS
DMA BUS
FILTER BUS
DFA PATT 1
DFA PATT 2
    
```

Details of each test follow:

DFA FUNCTN

The DFA function test should be used to test the overall health of the digital filter assembly (A5 & A6). Other diagnostic tests should be used to further isolate problems as described in the following paragraphs.

The DFA functional test performs a zoom measurement on data created by the system CPU and stored in global RAM. The test simulates measuring a 16 kHz square wave with a zoom window 10 kHz wide, centered at 16.5 kHz. The results are processed by the FFT and FPP boards to create a power spectrum. The power spectrum is checked for proper amplitude of the fundamental and noise floor.

This test exercises all circuitry in the DFA except the trigger circuitry in the measurement state machine block and the trigger LED control block on the A6 board. Prior to performing this measurement, the interrupts used to indicate the end of measurement are tested. If either of the two interrupt tests fail, the zoom measurement is not performed. This protects against failure of the program to run to completion. When the interrupts are inoperable, the DFA cannot signal the CPU that the measurement is complete and the program waits indefinitely.

If the DFA function passes, the following messages are displayed:

| | |
|-------------------------------|--------|
| DFA Filtered Chan Interrupt | Passes |
| DFA Unfiltered Chan Interrupt | Passes |
| DFA Functional Test | Passes |

The filtered and unfiltered interrupt tests refer to the types of interrupts used to perform the measurement. Data is transferred from global RAM into the digital filter controller, where it may or may not be filtered, depending on the type of measurement required. There is an interrupt indicating end of measurement for each of the two cases.

If either of the interrupt tests fail, test the local bus (first) and then the DMA bus with the diagnostic tests of the same name. The descriptions of these tests appear later in this section.

If the DFA functional test fails, begin troubleshooting by running the local bus test; it has to function correctly before anything else can be tested.

If the DFA function test passes, the A5, A6 assemblies are probably functioning correctly with two exceptions: neither the trigger circuitry in the measurement state machine block nor the circuitry in the trigger LED control block on the A6 board are exercised by this test.

If the trigger is failing and the problem has been isolated to the A5, A6 assemblies, start troubleshooting the Trigger Control PAL (A6 U409) and the Start/Stop Control PAL (A6 U309). Other possible problem areas include the AM9513 counter (A6 U109) and the trigger interrupt flag (A6 U303).

If the 'TRIGGERING' or 'MEASURING' LEDs are not functioning correctly, start troubleshooting the Trigger LED Control Subblock.

If at least one channel's functional test passes, the following circuits are probably functioning correctly:

- Global Data Bus Interface for the channel passing the test.
- Global Bus DMA Control except the DMA Controller (A5 U307, U309) for the failing channel.
- The Address Output Registers for the channel passing the test.
- The Digital Filter subblock and associated subblocks on the A5 assembly for the channel passing the test.
- The Parallel Input Control lines associated with the channel passing the test.
- The LO Signal/Constant Select lines associated with the passing channel.
- The A6 assembly except the Command Register and the Start/Stop Control PLA.

FILTER TEST

The filter test should be used, after the DFA functional test is performed, to isolate problems associated with the digital filter blocks on the A5 board. The measurement interrupts are not tested prior to performing this test and the instrument will hang if they do not work correctly.

This test performs the same measurement on the same data as described for the DFA functional diagnostic test except that it uses a constant signal instead of the LO signal for the zoom process. This means that the fundamental signal is outside the zoom window (subharmonics are all that are measured), but the measurement results are predictable to the point that individual bits may be checked .

The results of the filtering are stored in global RAM. The system CPU then performs a checksum on the data and compares it to known values. Errors are reported for bad data from blocks processed by the real and imaginary filter ICs in channels one and two.

If only one of the following fails, start troubleshooting the associated IC in the CHAN 1 Digital Filter or CHAN 2 Digital Filter subblock:

- DFA Chan 1 Real Filter
- DFA Chan 1 Imag Filter
- DFA Chan 2 Real Filter
- DFA Chan 2 Imag Filter

If both real and imaginary fail for a given channel, troubleshoot the controller chip or the filter bus interface chip associated with it. The three ICs in the digital filter block of each channel are mounted in sockets and may be switched to verify operation. However, further use of the diagnostic tests is recommended before you begin switching ICs.

If both real or both imaginary filter tests fail, troubleshoot the LO signal selection block on the A5 board.

LOCAL BUS

The local bus test should be used to test the operation of the local data bus and the AM9513 counter in the data point counter block. The local data bus is used by the system CPU to communicate with blocks on both DFA boards. See the block diagrams for the A5, A6 boards in Section VI. On the A6 board these blocks are the interrupts block, the measurement state machine block, and the data pointer block. On the A5 board this bus interfaces to both digital filter busses and the DMA bus.

This test must pass before any other DFA diagnostic self-test can pass. The local bus test uses the AM9513 counter (A6 **U109**) to echo data on the local data bus (LD0 to LD15) through the system data bus interface. The test echos data several times, using a different register in the counter each time. Therefore, the test can tell a bus failure from a counter failure.

Note that, since both DFA blocks exercised in this test (the system interface and the counter) are on the A6 board, the A5 board is not involved in this test other than to demonstrate that bus interface circuits on the A5 board are not inhibiting the bus.

If this test fails, remove the A5 Digital Filter assembly and repeat the test. If the test still fails, start troubleshooting the system data bus interface and data point counter block on the A6 board. If the test passes with the A5 board removed, the failure is on the A5 assembly; replace the A5 assembly and continue with the diagnostic tests.

If a bit passes any of the echos tests, the bus line transmitting that bit is good. If that bit is bad on every test, the bus line is probably defective. Any bit that passes some but not all of the tests indicates a defective counter register.

If this test passes, the following subblocks are probably functioning correctly:

- Data Point Counter
- System Data Bus Interface
- System Address Decoder

DMA BUS

The DMA bus test should be used, after the operation of the local data bus is verified, to test the operation of the interface between the local data bus and the DMA bus and the DMA controller ICs.

This test is similar to the local bus test described previously except that the DMA controller ICs are used to echo data from the system CPU instead of the counter on the A6 board. Refer to the block diagrams in Section VI to visualize the data path. The circuits exercised are the system data interface on the A6 board and the local data/DMA bus interface and DMA controllers on the A5 board.

If this test passes, the following are probably functioning correctly:

- Local Data Bus
- DMA Bus
- Local Data/DMA Bus Interface
- DMA controllers

If this test fails and the local bus test passes, the failure is probably in the Global Bus DMA Control or Local Data/DMA Bus Interface. The test message displayed on the screen identifies which of the two should be investigated along with information describing which bit has failed.

FILTER BUS

The filter bus test should be used, after the operation of the local data bus is verified, to test the transfer of data between the digital filter blocks and global RAM.

The filter bus test transfers one word from global RAM, through the digital filter bus, into the digital filter controller IC, and then transfers it back to global RAM. Refer to the block diagrams in Section VI to visualize the data path. This sequence is performed once for each of the two channels. The test checks for either incorrect words or failure to write anything at all.

Failure to write anything, denoted by the message "DFA Chan x Write," indicates a problem with measurement control circuits on A6 or the digital filter control IC corresponding to the channel that failed (the measurement failed to set up). Writing wrong data causes the message "DFA Filter Bus x" to be displayed and indicates a problem with the interface IC associated with the failing channel.

If the filter bus test passes, the following circuits and processes are probably functioning correctly:

- Parallel Input Control
- Global Bus DMA Control
- Global Data Bus Interface
- Address Output Registers
- Unfiltered channel output of the CHAN 1 and CHAN 2 Filter Controls

NOTE

The message "DFA Filter Bus 1" corresponds to the Chan 1 Digital Filter Data Bus and "DFA Filter Bus 2" corresponds to the Chan 2 Digital Filter Data Bus.

DFA PATT 1

The digital filter pattern test #1 is used for two purposes: with the loop mode off, it is a diagnostic self-test of the digital filter blocks with no inputs; with the loop mode on, it is a signature test for the digital filter data busses and the global data bus interface block. It is intended to be used as follows:

1. Run the diagnostic (loop mode off).
2. If Transient Test #1 fails, perform the test with loop mode on and use the signatures to isolate problems in the output path (from the filter controller IC through the global data bus interface).

3. If Transient Test #1 passes and other transient tests fail, the problem is probably one of the filter ICs. The signature tests cannot be used to verify this, as is explained later in this discussion.
4. Perform the Filter Bus test. If it passes, the problem is probably in a filter IC; switch filter ICs between channels to see if the problem changes channels.

When the test is run **with loop mode off**, the filter ICs execute a test routine that generates five different signals (called transients) within the IC on which measurements are performed. Measurement data is transferred to global RAM through the digital filter busses and the global data bus interface block. The system CPU performs a signature analysis on the data and reports any line with an incorrect signature.

This test allows you to isolate the measurement and data storage processes from the input process. The first four measurements are zoomed (real and imaginary data) and the fifth is baseband (real data, only). Failure messages tell you three things: which of the five tests fail (these are called DFA Transient Tests), which channel and filter IC fail (e.g., CH1 Real Filt), and which bits fail. The filter ICs are duplicate parts mounted in sockets allowing you to switch parts between channels to verify failures.

When the test is run **with loop mode on**, the first transient test (only) is performed, repetitively, so that digital signature analysis may be used to isolate problems in the output path from the filter ICs through the global bus interface to the global bus.

To activate the DFA PATT 1 diagnostic test, move jumper A5 J7 to its test position and press the softkey titled DFA PATT 1.

If this test passes, the following subblocks are probably functioning correctly:

- Global Bus DMA Control
- Address Output Registers
- Global Data Bus Interface
- CHAN 1 Digital Filter Data Bus
- CHAN 2 Digital Filter Data Bus
- CHAN 1 Digital Filter
- CHAN 2 Digital Filter

DFA PATT 2

The digital filter pattern #2 diagnostic is a digital signature analysis test. It is used to test the measurement and control circuits on the A6 board. Its use is explained in the signature tables.

B. Signal Verification

Verify the following signals and supply voltages:

1. Check the +5V level at A5 TP5 and the +8V level at A5 U101-7 and A5 U114-7.
2. The phase clocks for channel 1 and channel 2 and their test locations are:

CH1 ϕ 1 A5 TP1
CH1 ϕ 2 A5 TP2
CH2 ϕ 1 A5 TP3
CH2 ϕ 2 A5 TP4

Compare the phase clocks as follows:

- a. The two clocks for each channel should vary between 0 and +8V and should be 90° out of phase. See waveform #1, table A5-1.
 - b. Phase clock CH1 ϕ 1 should be in phase with CH2 ϕ 1. See waveform #2, table A5-1.
 - c. Phase clock CH1 ϕ 2 should be in phase with CH2 ϕ 2.
3. Verify the signals CH1SHIFT1 (A5 U401-19) and CH2SHIFT1 (A5 U415-19). (See waveform #3, table A5-1). If each of these signals is a 200 ns pulse at a 256 kHz rate, then the channel 1 and channel 2 digital filters are accepting data. If the digital filters are not accepting data, the pulses occur at a 512 kHz rate.
 4. Verify the SYNC2 signal at A5 U401-20 and A5 U415-20 (waveform #4, table A5-1). The SYNC2 signals are only active when the digital filter has accepted a data point.
 5. Verify the following bus requests from the filter controls (see waveform #5, table A5-1):

CH1BR2 A5 U401-47
CH1BR3 A5 U401-34
CH2BR2 A5 U415-47
CH2BR3 A5 U415-34

If these signals are correct, the filters are asking for the bus.

6. Verify that the MCLK signal (A5 TP20) is changing between TTL levels. This indicates that channel 1 and channel 2 digital filter circuits are being synchronized.
7. Verify that signal CH1IOEN is correct (waveform #6, table A5-1). Verify that signal CH2IOEN is a similar but non-periodic pulse.
8. Verify that signal IRQT5L (A6 U401-6) is changing between TTL levels. This indicates that the interrupt circuits are passing data.

C. Oscilloscope Signal Waveforms

The following table of illustrations are oscilloscope plots of signals to be verified on the A5 and A6 boards. Note that all measurements are taken with a 10:1 probe. Other notes unique to a measurement are written next to the waveform.

Table A5-1 Oscilloscope Signal Waveforms

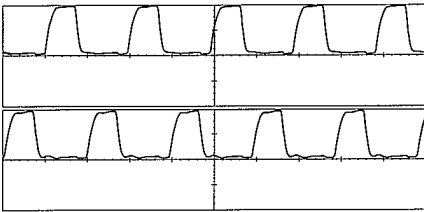
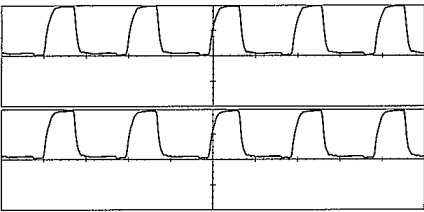
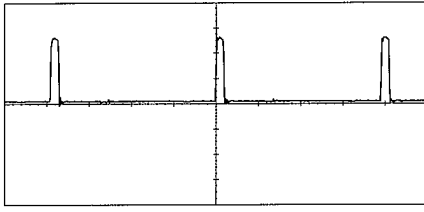
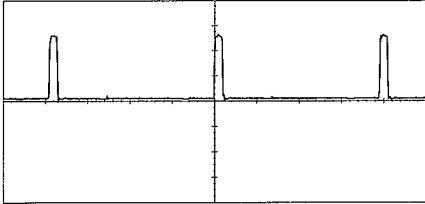

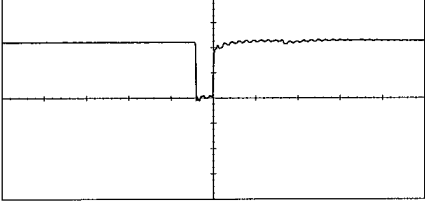
| Setup | Important Parameters | Waveform |
|---|--|--|
| <p>CH1ϕ1/CH2ϕ2, CH1ϕ2/CH2ϕ2</p> <p>Channel 1: Connect Ch 1 to A5 TP1 Connect Ch 2 to A5 TP2</p> <p>Channel 2:</p> <p>Scale 4 V/div Timebase 100 ns/div Offset 0 V Coupling dc</p> | <p>Time</p> <p>Phase</p> <p>Levels</p> |  <p>#1</p> |
| <p>CH1ϕ1, CH2ϕ1</p> <p>Connect Ch 1 to A5 TP1 Connect Ch 2 to A5 TP3</p> <p>Scale 4 V/div Timebase 100 ns/div Offset 0 V Coupling dc</p> | <p>Time</p> <p>Phase</p> <p>Levels</p> |  <p>#2</p> |
| <p>CH1SHIFT1/CH2SHIFT1</p> <p>Channel 1: Connect Ch 1 to A5 U401-19</p> <p>Channel 2: Connect Ch 1 to A5 U415-19</p> <p>Scale 2 V/div Timebase 1 μs/div Offset 0 V Coupling dc</p> | <p>Time</p> |  <p>#3</p> |

Table A5-1 Oscilloscope Signal Waveforms cont.

| Setup | Important Parameters | Waveform |
|--|----------------------|--|
| <p>SYNC2</p> <p>Connect Ch 1 to A5 U401-20</p> <p>Scale 2 V/div</p> <p>Timebase 1 μs/div</p> <p>Offset 0 V</p> <p>Coupling dc</p> | |  <p>#4</p> |
| <p>CH1BR2/CH2BR2, CH1BR3/CH2BR3</p> <p>Channel 1: Connect Ch 1 to A5 U401-34 or -47</p> <p>Channel 2: Connect Ch 1 to A5 U415-34 or -47</p> <p>Scale 2 V/div</p> <p>Timebase 100 ns/div</p> <p>Offset 0 V</p> <p>Coupling dc</p> | <p>Time</p> |  <p>#5</p> |
| <p>CH1IOEN</p> <p>Connect Ch1 to A5 TP18</p> <p>Scale 2 V/div</p> <p>Timebase 1 μs/div</p> <p>Offset 0 V</p> <p>Coupling dc</p> | <p>Time</p> |  <p>#6</p> |

D. Signature Analysis Tests

The following six signature analysis tests are designed to test circuit blocks of the digital filter assembly. Perform the following steps to configure the 3561A for any of the six tests:

- Disconnect the power cable.
- Put the board under test on an extender card. All jumpers should be in the normal (N) position.
- Connect and configure the signature analyzer as described at the beginning of the test you wish to perform.
- Move jumpers as instructed at the beginning of the test.
- Connect the power cable and turn on power.
- Initiate the DFA PATT test as instructed at the beginning of the test. To put a test in the loop mode, press the SPCL FCTN key, select SERVIC TEST, and press the LOOP menu key to light up ON.

1. Signature Analysis Test A5 #1 System Interface & Control

- a. Put A5J5 and A5J4 in test position. Put A6J2 in test position.
- b. Connect the signature analyzer as follows:

| Signal | Polarity | Connection |
|--------|----------|------------|
| GND | | A5 TP8 |
| START | + | A5 TP13 |
| STOP | - | A5 TP13 |
| CLOCK | + | A5 TP5 |

- c. Put DFA PATT 1 in Loop Mode
- d. Check the signatures in table A5-2.

Table A5-2 DFA Signature Analysis Test #1

| Component | Pin | Signature | Component | Pin | Signature | | |
|-----------|------|-----------|-----------|------|-----------|------|--|
| +5 v | | 4CB3 | U207 | 12 | 81C0 | | |
| U505 | 11 | 8071 | | 14 | HF13 | | |
| | 12 | AP0A | 16 | HF13 | | | |
| | 13 | 81C0 | 17 | 16F0 | | | |
| | 14 | FF7H | U209 | 12 | AP0A | | |
| | 15 | 16F0 | | 14 | 2914 | | |
| U406 | 2 | U7C6 | | 16 | 2914 | | |
| | 3 | U355 | 15 | FF7H | | | |
| | 4 | 9232 | U208 | 13 | FF7H | | |
| | 5 | 4709 | | 14 | 4C63 | | |
| | 6 | 8P7A | | 15 | CP64 | | |
| | 7 | 4C18 | | 16 | 16F0 | | |
| | 8 | 1845 | | 17 | 4C63 | | |
| | 9 | 1845 | | 18 | 16F0 | | |
| | 11 | 87AP | | U311 | 14 | FC21 | |
| | 12 | 87AP | | | 15 | 53H9 | |
| | 13 | 9140 | 16 | | 7C0C | | |
| | 14 | 87AP | 17 | | P4AU | | |
| | 15 | 87AP | 18 | | 1A0C | | |
| | 16 | 8325 | 19 | | 2989 | | |
| | 17 | 87AP | 20 | | 782H | | |
| | 18 | 83A4 | 21 | | 4764 | | |
| | 19 | 16F0 | 22 | | 4U19 | | |
| | U411 | 2 | 9FAU | | | | |
| | | 3 | 08A9 | | | | |
| 4 | | 06U2 | | | | | |
| 5 | | C970 | | | | | |
| 6 | | 44UC | | | | | |
| 7 | | 65C1 | | | | | |
| 8 | | F0A9 | | | | | |
| 9 | | 4C59 | | | | | |
| 11 | | A826 | | | | | |
| 12 | | A826 | | | | | |
| 13 | | PH9H | | | | | |
| 14 | | PH9H | | | | | |
| 15 | | A826 | | | | | |
| 16 | | AA63 | | | | | |
| 17 | | A826 | | | | | |
| 18 | | AA23 | | | | | |
| 19 | | FF7H | | | | | |

- e. Turn off power. Return all jumpers to normal (N) position.
- 2. Signature Analysis Test A5 #2 Channel 1 Digital Filters
 - a. Put J7 in Test Position.
 - b. Connect the signature analyzer as follows:

| Signal | Polarity | Connection |
|--------|----------|-----------------|
| GND | | TP8 |
| START | + | A5 TP13 (DSASS) |
| STOP | + | A5 TP13 (DSASS) |
| CLOCK | + | A5 U404-1 |

- c. Put DFA PATT 1 in Loop Mode.
- d. Check the signatures in table A5-3.

Table A5-3 DFA Signature Analysis Test #2

| Component | Pin | Signature |
|-----------|------|-----------|
| +5 v | | 6PCP |
| U401 | 23 | 54CA |
| | 24 | 3C53 |
| | 25 | 911P |
| | 26 | 7207 |
| | 27 | CP64 |
| | 28 | 76H1 |
| | 29 | 0738 |
| | 30 | 17C5 |
| | 31 | 34P4 |
| | 32 | F15P |
| | 45 | 2595 |
| | 53 | A0U7 |
| | 54 | 7P05 |
| | 55 | 30P1 |
| | 56 | C6PF |
| | 57 | 25AU |
| 59 | 2595 | |
| 60 | 2595 | |
| 61 | 2595 | |
| 62 | 2595 | |

- e. Return all jumpers to the normal (N) position.
3. Signature Analysis Test A5 -3 Channel 2 Digital Filter
- a. Put J7 in Test Position
 - b. Connect the signature analyzer as follows:

Table A5-4 DFA Signature Analysis Test #3

| Component | Pin | Signature |
|-----------|------|-----------|
| +5 V | | 6PCP |
| U415 | 23 | 54CA |
| | 24 | 3C53 |
| | 25 | 911P |
| | 26 | 7207 |
| | 27 | CP64 |
| | 28 | 76H1 |
| | 29 | 0738 |
| | 30 | 17C5 |
| | 31 | 34P4 |
| | 32 | F15P |
| | 45 | 2595 |
| | 53 | A0U7 |
| | 54 | 7P05 |
| | 55 | 30P1 |
| 56 | C6PF | |
| 57 | 25AU | |
| 59 | 2595 | |
| 60 | 2595 | |
| 61 | 2595 | |
| 62 | 2595 | |

- e. Return all jumpers to normal (N) position.
4. Signature Analysis Test A5 -4 Channel 1 Global Data Bus Interface
- a. Put J7 in test position
 - b. Connect the signature analyzer as follows:

| Signal | Polarity | Connection |
|--------|----------|------------|
| GND | | TP8 |
| START | + | A5 TP13 |
| STOP | - | A5 TP13 |
| CLOCK | + | A5 TP21 |

- c. Put DFA PATT 1 in Loop Mode.
- d. Check the signatures in table A5-5.

Table A5-5 DFA Signature Analysis Test #4

| Component | Pin | Signature | Component | Pin | Signature |
|-----------|-----|-----------|-----------|-----|-----------|
| +5 V | | 6PCP | U404 | 13 | UUA0 |
| U304 | 14 | AUP0 | | 14 | 55PH |
| | 15 | 5A5A | | 15 | 3A04 |
| | 16 | 790C | | 16 | 5P5U |
| | 17 | 6986 | | 17 | H852 |
| | 18 | 186U | | 18 | 10CC |
| | 19 | H0HA | | 19 | 4C11 |
| | 20 | 1FC9 | | 20 | FP49 |

- e. Return all jumpers to normal (N) position.
5. Signature Analysis Test A5 -5 Channel 2 Global Data Bus Interface
- a. Put J7 in test position
 - b. Connect the signature analyzer as follows:

| Signal | Polarity | Connection |
|--------|----------|------------|
| GND | | TP8 |
| START | + | A5 TP13 |
| STOP | - | A5 TP13 |
| CLOCK | + | A5 TP22 |

- c. Put DFA PATT 1 in Loop Mode.
- d. Check the signatures in table A5-6.

Table A5-6 DFA Signature Analysis Test #5

| Component | Pin | Signature | Component | Pin | Signature |
|-----------|-----|-----------|-----------|-----|-----------|
| +5 V | | 6PCP | U413 | 13 | UUA0 |
| U313 | 14 | AUP0 | | 14 | 55PH |
| | 15 | 5A5A | | 15 | 3A04 |
| | 16 | 790C | | 16 | 5P5U |
| | 17 | 6986 | | 17 | H852 |
| | 18 | 186U | | 18 | 10CC |
| | 19 | H0HA | | 19 | 4C11 |
| | 20 | 1FC9 | | 20 | FP49 |

- e. Return all jumpers to normal (N) position.

6. Signature Analysis Test A6 -1 Digital Filter Control
 - a. Put J2 in Test (T) position.
 - b. Connect the signature analyzer as follows:

| Signal | Polarity | Connection |
|---------------|-----------------|-------------------|
| GND | | A6 TP3 |
| START | + | A6 TP7 |
| STOP | + | A6 TP7 |
| CLOCK | + | A6 TP5 |

- c. Put DFA PATT 2 in Loop Mode.
 - d. Check the signatures in table A5-7.

Table A5-7 DFA Signature Analysis Test #6

| Component | Pin | Signature | Component | Pin | Signature | |
|-----------|------|-----------|-----------|------|-----------|------|
| + 5 V | | HUHC | U107 | 1 | 0H95 | |
| U304 | 1 | Toggle | | 2 | Toggle | |
| | 2 | UF43 | | 3 | Toggle | |
| | 3 | 0H95 | | 4 | H24P | |
| | 4 | 12P1 | | 5 | Toggle | |
| | 5 | 648A | | 6 | Toggle | |
| | 6 | Toggle | | 7 | Toggle | |
| | 7 | Toggle | | 9 | Toggle | |
| | 8 | 56A4 | | 10 | 0H95 | |
| | 9 | Toggle | | 11 | H24P | |
| | 11 | H24P | | 12 | 0H95 | |
| | 12 | Toggle | | 13 | 0H95 | |
| | 13 | 2398 | | 14 | H24P | |
| | 14 | 0H95 | | 15 | 0H95 | |
| | 15 | 3179 | | U202 | 9 | 21C4 |
| | 16 | 49A3 | 13 | | 0AP1 | |
| | 18 | 56H7 | U203 | 5 | C9FP | |
| | U406 | 1 | | 56A4 | U305 | 5 |
| | | 2 | AFFF | U207 | | 6 |
| 3 | | AFFF | 10 | | P5UU | |
| 4 | | FH76 | 15 | | H28U | |
| 5 | | 447C | U206 | 3 | 07C5 | |
| 6 | | AFFF | | 6 | 0AP1 | |
| 7 | | AFFF | | 8 | H28U | |
| 8 | | AFFF | U307 | 6 | P884 | |
| 9 | | AFFF | | 9 | U01U | |
| U405 | 1 | 56A4 | | 16 | U576 | |
| | 2 | 8HU8 | U306 | 2 | P5UU | |
| | 3 | 456C | | 3 | U576 | |
| | 4 | 76H2 | | 4 | U01U | |
| | 5 | 07HP | | 5 | C9FP | |
| | 6 | H75A | | 6 | 1604 | |
| | 7 | 37F7 | | 7 | 8A3C | |
| | 8 | 1C90 | | 8 | C0HH | |
| | 9 | U974 | | 12 | 2726 | |
| U109 | 2 | 7203 | | 13 | 07C5 | |
| | 3 | 4946 | 14 | 2P68 | | |
| | 4 | 0AP1 | 15 | 0AP1 | | |
| | 5 | Toggle | 16 | 6APF | | |
| | 6 | Toggle | 17 | 6PU9 | | |
| | 7 | Toggle | 18 | H941 | | |
| | 8 | 648A | 19 | 67U5 | | |
| | 9 | Toggle | | | | |
| | 10 | H24P | | | | |
| | 11 | 897U | | | | |
| | 34 | 0AP1 | | | | |
| | 35 | 0AP1 | | | | |
| 37 | C22H | | | | | |
| 38 | 6AU7 | | | | | |
| 40 | 255C | | | | | |

Table A5-7 DFA Signature Analysis Test #6 cont.

| Component | Pin | Signature | Component | Pin | Signature |
|-----------|------|-----------|-----------|-----|-----------|
| U309 | 1 | 0AP1 | U303 | 9 | F474 |
| | 4 | 255C | | 14 | 49A3 |
| | 5 | 7203 | U203 | 9 | 3048 |
| | 8 | H941 | | 13 | 49A3 |
| | 9 | 07C5 | U104 | 6 | 49A3 |
| | 12 | 8169 | | 8 | 49A3 |
| | 13 | 8A3C | | 11 | 49A3 |
| | 14 | H28U | | | |
| | 15 | 16P9 | | | |
| | 16 | H28U | | | |
| | 17 | 8278 | | | |
| | 18 | CHCH | | | |
| | 19 | 216U | | | |
| | U308 | 12 | 447C | | |
| 13 | | FH76 | | | |
| 14 | | 1C90 | | | |
| 15 | | 37F7 | | | |
| 16 | | H75A | | | |
| 17 | | 07HP | | | |
| 18 | | 76H2 | | | |
| 19 | 8HU8 | | | | |

e. Return all jumpers to normal (N) position.

E. After-Repair Adjustments and Tests

Table A5-8 After-Repair Adjustments and Tests

| Perform the following: | Section |
|-------------------------------|---------|
| Diagnostic Tests: Test All | VII |
| Adjustments: None | |
| Performance Tests: None | |

8-10 A7 FLOATING POINT PROCESSOR

The information in this section should be used to isolate faulty subblocks in the A7 Floating Point Processor (FPP). All procedures assume the fault isolation procedures of Section VII have been used to determine which board has failed, and the circuit descriptions of Section VI are understood.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Hazardous voltage and energy available at many points can, if contacted, result in personal injury.

CAUTION

Do not insert or remove any circuit board in the HP 3562A with the line power turned on. Power transients caused by insertion or removal may damage the circuit boards.

How to Use This Section

| | |
|---------------------|---|
| Start | Start troubleshooting by performing part A, "Initial Conditions Test". The primary troubleshooting method for the FPP is to use the self-tests to determine which subblocks are operating correctly. Signature analysis is then used to troubleshoot individual subblocks suspected of failing. |
| Reference | For the component locator and schematic refer to Section IX. For the location of cables and boards refer to figure 4-1 in Section IV. |
| Verify | Use the oscilloscope waveforms in table A7-8 to verify correct operation at various test points in the assembly. |
| After-Repair | Use table A7-9 to determine which adjustments and tests need to be done to complete instrument service. |

Troubleshooting Hints

1. After the power-up tests or reset (A2 S1), the FPP status LEDs should be changing rapidly. If the LEDs are off or the FPP does not respond to any self-tests, the problem is most likely the sequencer, the microcode memory, the ALUs control logic, or the control PALs. Use signature analysis test #4 to isolate the failure (after performing part A).

2. If any board in the HP 3562A has been pulled out of its card nest with the power on, check A7 U504.

A. Initial Conditions Test

1. Disconnect the power cable from the rear panel and remove the top cover. Place the A7 FPP on the 03562-6640 extender board.
2. Connect the power cable and press the line switch on.
3. Check the following for correct value:

| Signal | Location | Value |
|---------------|-----------------|--------------------------|
| +5S | A7 TP7 | +5 \pm 0.3V |
| 8 MHz | A7 TP3 | Refer to waveform #1 (E) |
| 4 MHz | A7 J5-3 | Refer to waveform #1 (E) |

4. If the +5S is not the correct value, go to paragraph 8-16, "A18 Power Supply Assembly".
5. If the cause of the failure is still not found, go to part B.

B. FPP Diagnostics

The FPP is tested using several self-tests. When a test is initiated, the A2 System CPU loads test data and FPP instructions into the A8 Global RAM (except in the Reset FPP test) and commands the FPP to perform the test. After completing the test, the FPP sends the test results to global RAM and an interrupt (IRQT3L) to the system CPU. Any failed bits and the status of the interrupt are annunciated on the display. Several of these tests are also used in loop mode for signature analysis patterns. Refer to part C for a description of each self-test.

1. To perform the FPP self-tests, press the HP 3562A keys as follows:

```

PRESET      ..... RESET

SPCL FCTN   ..... SERVIC
                TEST      ..... TEST
                                PROC      ..... TEST
                                                    FPP

                                                    ..... FPP
                                                    FUNCTN

                                                    ..... COMAND
                                                    POINTR

                                                    ..... BLOCK
                                                    SET

                                                    ..... ALU
                                                    TEST A

                                                    ..... ALU
                                                    TEST B

                                                    ..... RESET
                                                    FPP
    
```

NOTE

If a test does not terminate (no message is displayed), press A2 S1 to reset the FPP and continue with the self-tests.

2. If the command pointer test (COMAND POINTR) does not complete, press A2 S1. When the power-up tests are completed, set jumper A7 J2B to test position. Press the HP 3562A keys as follows:

```

SPCL FCTN   ..... SERVIC
                TEST      ..... TEST
                                PROC      ..... TEST
                                                    FPP

                                                    ..... JUMPER
                                                    ECHO

                                                    ..... JUMPER
                                                    ECHO
    
```

The FPP status LEDs should display 0000 0001 (0=off, 1=on).

3. Use table A7-1 to determine which signature analysis tests to perform.

Table A7-1 FPP Diagnostics

| Test Messages | Passes Subblocks verified | Fails Perform Signature Analysis Tests (D) in order listed |
|---|---|---|
| FPP Function Test: Floating Point Processor | All subblocks of the FPP are exercised. If this test passes but an FPP function is failing, perform SA test #2 and #4. | Continue with self-tests |
| Command Pointer Test: FPP Command Pointer Test Bits correspond to B bus 0 to 15 and Y bus 0 to 23 | Command Pointer Registers DTACK Circuit FPP Interrupt Circuit Global Data Bus Output Registers Partial verification of ALUs | SA #1 SA #2 SA #3 SA #4 |
| FPP Interrupt Test | FPP Interrupt Circuit | The FPP did not return IRQT3 to the CPU after running a test. Continue with self-tests. |
| Jumper Echo Test: FPP Jumper Echo Bits correspond to B bus 0 to 15 and Y bus 0 to 23 | Command Pointer Registers DTACK Circuit FPP Interrupt Circuit Global Data Bus Output Registers Partial verification of ALUs | SA #1 SA #2 SA #3 SA #4 |
| Block Set Test: FPP Address Test Bits correspond to B bus 0 to 15 | Global Address Registers Global Data Bus Input Registers | SA #1 SA #4 |
| ALU Test A: FPP ALU Test A Bits correspond to Y bus 0 to 23 | Partial verification of ALUs | SA #2 SA #3 SA #4 |
| ALU Test B: FPP ALU Test B Bits correspond to Y bus 0 to 23 | ALUs Carry Look-ahead subblock Shift PAL (U212) Status Multiplexer (U201) Sequencer | SA #2 SA #3 SA #4 |
| Reset FPP Test: FPP RESET Test | Pipeline Data Bus Partial verification of Sequencer | SA #3 SA #4 |
| If all the self-tests fail, start with signature analysis test #1. | | |

C. FPP Diagnostics Descriptions

The FPP diagnostics perform the following functions:

1. FPP Function Test

When the FPP FUNCTN key is pressed, the A2 System CPU loads test data into the A8 Global RAM. The system CPU then commands the FPP to perform a floating point complex multiplication.

2. Command Pointer Test

The COMAND POINTR key initiates an echo test between the command pointer registers (U505, U506) and the FPP status stored in global RAM. This test verifies the command pointer registers, the DTACK circuit, the FPP interrupt and the global data output registers (U412, U414, U512, U514).

The system CPU sets up a command stack containing the echo instruction in global RAM. The system CPU then writes the address where the command stack is stored into the command pointer registers. The FPP sends the same address to global Ram using the ALUs and global bus interface circuits. When the FPP is finished with the operation, it sends an interrupt (IRQT3L) to the system CPU. The system CPU tests the FPP status in global RAM and any errors in the status are displayed.

If the interrupt is not received by the system CPU before a countdown loop is completed, the system CPU tests the FPP status in global RAM. Any errors in the status and an FPP interrupt failure are displayed.

3. Jumper Echo Test

The jumper echo test is used when the command pointer test does not terminate (no message is displayed). The jumper echo test performs the same test as the command pointer test except the A2 CPU does not load test data in the A8 Global RAM. The jumper echo test is invoked by setting A7 J2B to test position (with the power on) and resetting the FPP. The jumper echo test forces the FPP to perform the echo command. If the command pointer test fails to function, the jumper echo test may function.

4. Block Set Test

This test uses the 'set constant command' of the FPP to test the global address registers (U510, U511). Complementary patterns are written to global RAM at address locations which differ by one address bit. The system CPU verifies the result. For this test, the global data bus output registers (U412, U414, U512, U514) are assumed to be operating correctly.

5. ALU Test A

When the ALU Test A key is pressed, patterns are written to the ALUs (U303, U304, U305, U307, U308, U310) and shift PAL (U212). The FPP outputs data to the global RAM which is verified by the system CPU. This test can be run in loop mode by setting A7 J2A and A7 J2B to test position.

6. ALU Test B

When the ALU Test B key is pressed, the ALUs are thoroughly tested along with the carry look-ahead subblock (U211, U302), the shift PAL (U212), the status multiplexer (U201), and the sequencer (U103).

D. A7 Signature Analysis Tests

Use these tests to isolate a failure on the FPP assembly. Only the components in failing subblocks need to be tested. The term 'togglng' refers to a signal continually changing between TTL level high and TTL level low.

1. Press the line switch off.
2. Put all jumpers in normal (N) position.
3. Connect the Signature Analyzer as follows:

Table A7-2 A7 Signature Analyzer Setup #1

| Signal | Polarity | Connection |
|--------|---------------|------------|
| Ground | | A7 J5-1 |
| Clock | Positive edge | A7 J5-3 |
| Stop | Negative edge | A7 J5-4 |
| Start | Positive edge | A7 J5-5 |

4. Press the line switch on.
5. Signature Analysis Test #1 Setup:
 - a. Put jumper A7 J2B in test position with the power on.
 - b. Press A2 S1 (reset switch on the A2 CPU). The FPP status LEDs should read 0000 0001 (1 = on, 0 = off). If this test is not stable, use signature analysis tests #3 and #4.

Table A7-3 A7 Signature Analysis Test #1

| Jumper Echo Test Jumpers in test (T) position: A7 J2B Jumpers in normal (N) position: A7 J1, A7 J2A, A7 J3A, B, C, D, A7 J4, A7 J6A, B, A7 J7, A7 J8, A7 J9A, B Signature Analyzer Setup: Refer to table A7-2 +5 V Signature = 9515 | | | | | | |
|---|-----------|-----------|---------------|-----------|-----------|------|
| Component | Pin | Signature | Component | Pin | Signature | |
| U201 | 19 | Toggleing | U506 cont. | 14 | 06A7 | |
| U209 | 6 | 67H9 | | 15 | U315 | |
| | 7 | 55FA | | 16 | 5915 | |
| | 8 | 6FH9 | | 17 | 0H15 | |
| | 9 | 6FH9 | | 18 | A515 | |
| | 11 | 3913 | 19 | U515 | | |
| U215 | 12 | 3913 | U507 | 19 | Toggleing | |
| | 14 | 3913 | U412 | 1 | Toggleing | |
| | 5 | 0000 | | 2 | 1472 | |
| | U313 | 12 | | Toggleing | 3 | U517 |
| 13 | | AF06 | | 4 | A517 | |
| 14 | | 9515 | 5 | 0H17 | | |
| 15 | | Toggleing | 6 | 5917 | | |
| 17 | | Toggleing | 7 | U316 | | |
| U314 | 18 | 0001 | 8 | 06A5 | | |
| | 19 | 9514 | 9 | 5FFP | | |
| | U401 | 13 | 9514 | 11 | 9514 | |
| | | 14 | 9514 | U414 | 2 | UCAP |
| | | 15 | 9515 | | 3 | 2H36 |
| 16 | | 9515 | 4 | | F67C | |
| 17 | | Toggleing | 5 | | C3HH | |
| 18 | Toggleing | 6 | 890P | | | |
| U401 | 19 | Toggleing | 7 | 9465 | | |
| | 12 | 55FA | 8 | 9AH3 | | |
| | 13 | 0A56 | 9 | 9H89 | | |
| | 14 | 9517 | U510 | 11 | 0001 | |
| | 15 | 55FC | | U512 | 2 | 2H35 |
| 16 | Toggleing | 3 | | | F67C | |
| 17 | 9515 | 4 | | | C3HH | |
| 18 | Toggleing | 5 | | | 890P | |
| 19 | Toggleing | 6 | 9467 | | | |
| U505 | 1 | FA8A | 7 | 9AH0 | | |
| | 12 | 1471 | 8 | 9H89 | | |
| | 13 | 97HF | 9 | 1P24 | | |
| | 14 | F54F | U514 | 2 | A431 | |
| | 15 | 9P32 | | 3 | 2761 | |
| | 16 | 835C | | 4 | FF2F | |
| | 17 | C988 | | 5 | C98A | |
| | 18 | FF2P | | 6 | 8359 | |
| 19 | 72AA | 7 | | FCUA | | |
| U506 | 12 | U1U9 | | 8 | 9084 | |
| | 13 | 5FFF | | 9 | 97HP | |

6. Put all jumpers in normal (N) position.

7. Signature Analysis Test #2 Setup:

- a. Put jumpers A7 J2A and A7 J2B in test (T) position with the power on.
- b. Press A2 S1. The FPP status LEDs should read 10101010 (1=on, 0=off).

Table A7-4 A7 Signature Analysis Test #2

| ALUs Test A Jumpers in test (T) position: A7 J2A, A7 J2B Jumpers in normal (N) position: A7 J1, A7 J3A, B, C, D, A7 J4, A7 J6A, B, A7 J7, A7 J8, A7 J9A, B Signature Analyzer Setup: Refer to table A7-2 +5 V Signature = 5C86 | | | | | |
|--|------|-----------|---------------|------|-----------|
| Component | Pin | Signature | Component | Pin | Signature |
| U212 | 1 | 0001 | U303 cont. | 30 | 4FUF |
| | 2 | AC6P | | 31 | 0000 |
| | 3 | F273 | | 32 | 0001 |
| | 4 | 85AU | | 33 | AC6P |
| | 5 | U484 | | 34 | F273 |
| | 6 | AC6P | | 35 | 85AU |
| | 7 | 3HAH | | 37 | 47HH |
| | 8 | C807 | | 38 | CC23 |
| | 9 | A84C | | 40 | 47HH |
| | 11 | UFFP | | 41 | C807 |
| | 12 | 97F3 | | 42 | A84C |
| | 13 | OU3P | | 44 | 3U2A |
| | 14 | A457 | | 45 | 912A |
| | 15 | 5C87 | | 46 | 0F67 |
| | 16 | U0P8 | | 47 | A94C |
| | 17 | 5C86 | | 48 | U421 |
| | 18 | 0000 | | | |
| | 19 | 0000 | | | |
| | U303 | 1 | | 97F3 | U304 |
| 2 | | 85AC | 4 | 0P75 | |
| 3 | | 618U | 5 | 618C | |
| 4 | | 0P75 | 6 | 0P75 | |
| 5 | | 618C | 10 | 8133 | |
| 6 | | 0P75 | 12 | 2026 | |
| 7 | | 3HAH | 14 | HAC5 | |
| 8 | | 6CPA | 16 | 17FA | |
| 9 | | 7CA6 | 17 | 46C9 | |
| 12 | | 2020 | 18 | 17FA | |
| 14 | | HAC5 | 19 | 46C9 | |
| 15 | | 85AC | 21 | 0U38 | |
| 16 | | 17F8 | 22 | UFFP | |
| 17 | | 46C9 | 23 | H51C | |
| 18 | | 17FA | 24 | C270 | |
| 19 | | 46C9 | 25 | H51C | |
| 20 | | 0U3P | 26 | C270 | |
| 21 | | 0U38 | 48 | U421 | |
| 22 | | UFFP | | | |
| 23 | | A35U | | | |
| 24 | | C270 | | | |
| 25 | | H51C | | | |
| 26 | | C270 | | | |
| 27 | | 160P | | | |
| 28 | | 76P8 | | | |
| 29 | | 5HA2 | | | |

Table A7-4 A7 Signature Analysis Test #2 cont.

| Component | Pin | Signature | Component | Pin | Signature |
|-----------|------|-----------|-----------|-----------|-----------|
| U305 | 3 | 6189 | U308 | 10 | 8133 |
| | 4 | U782 | | 12 | 2020 |
| | 5 | 6189 | | 14 | 6197 |
| | 6 | U782 | | 16 | 6189 |
| | 10 | 8133 | | 17 | U782 |
| | 12 | 2026 | | 18 | 6189 |
| | 14 | 6197 | | 19 | U782 |
| | 16 | 618U | | 21 | 0U38 |
| | 17 | 0P75 | | 22 | UFFF |
| | 18 | 618C | | 23 | 5AAA |
| | 19 | 0P75 | | 24 | 99A5 |
| | 21 | 0U38 | | 25 | 5AAA |
| | 22 | UFFF | | 26 | 99A5 |
| | 23 | 2FPP | | 39 | P0A5 |
| | 24 | PUP1 | | 40 | 5C86 |
| | 25 | 2FPP | | 48 | U421 |
| | U307 | 3 | | 6189 | U310 |
| 4 | | U782 | 11 | Toggleing | |
| 5 | | 6189 | 12 | 0000 | |
| 6 | | 53H5 | 14 | U484 | |
| 10 | | 3A11 | 16 | 6189 | |
| 12 | | 2026 | 17 | U782 | |
| 14 | | 6197 | 18 | 6189 | |
| 16 | | 618C | 19 | 53H5 | |
| 17 | | 0P75 | 21 | 5C87 | |
| 18 | | 618C | 22 | UFFF | |
| 19 | | 0P75 | 23 | 5AAA | |
| 21 | | 0U38 | 24 | 99A5 | |
| 22 | | UFFF | 25 | 5AAA | |
| 23 | | 2FPP | 26 | 4C8P | |
| 24 | | PUP1 | 48 | A457 | |
| 25 | | 2FPP | | | |
| 26 | | PUP1 | | | |
| 48 | U421 | | | | |

8. Put all jumpers in normal (N) position.
9. Signature Analysis Test #3 Setup:
 - a. Put jumper A7 J2A in test position with the power on.
 - b. Press A2 S1. The FPP status LEDs should read 1111 0000 (1= on, 0= off).
 - c. Put jumpers A7 J1 and A7 J4 in test position. The FPP status LEDs should now read 0011 1111.

Table A7-5 A7 Signature Analysis Test #3

| <p>MAP PROM Test Jumpers in test (T) position: A7 J2A, A7 J1, A7 J4 Jumpers in normal (N) position: A7 J2B, A7 J3A, B, C, D, A7 J6A, B, A7 J7, A7 J8, A7 J9A, B Signature Analyzer Setup: Refer to table A7-2 +5 V Signature = PFHO</p> | | | | | |
|---|-------------------------------------|--|-----------|-----|-----------|
| Component | Pin | Signature | Component | Pin | Signature |
| U209 | 6 7 8 11 12 13 14 | 354C H837 99UP C5AH F636 PFHO PFHO | U502 | 5 | 7A3F |

10. Put all jumpers in normal (N) position.

11. Signature Analysis Test #4 Setup:

- a. Press the line switch off.
- b. Connect the Signature Analyzer as follows:

Table A7-6 A7 Signature Analyzer Setup #2

| Signal | Polarity | Connection |
|--------|---------------|------------|
| Ground | | A7 J5-1 |
| Clock | Positive edge | A7 J5-3 |
| Stop | Positive edge | A7 TP4 |
| Start | Negative edge | A7 TP4 |

- c. Set jumpers A7 J3A,B,C,D, A7 J6A,B, A7 J7, A7 J8, A7 J9A,B to test (T) position.
- d. Press the line switch on. The FPP status LEDs should read 1111 1111 (1= on, 0= off).

Table A7-7 A7 Signature Analysis Test #4

| Sequencer, PROMs, and Control Test Jumpers in test (T) position: A7 J3A, B, C, D, A7 J6A, B, A7 J7, A7 J8, A7 J9A, B Jumpers in normal (N) position: A7 J1, A7 J2A, B, A7 J4 Signature Analyzer Setup: Refer to table A7-6 +5 V Signature = 7A70 | | | | | | |
|---|------|-----------|-----------|------|-----------|------|
| Component | Pin | Signature | Component | Pin | Signature | |
| U103 | 1 | P030 | U110 | 9 | H52P | |
| | 3 | 4442 | | 10 | P67U | |
| | 6 | 0000 | | 11 | 2443 | |
| | 7 | 7A70 | | 13 | UP53 | |
| | 18 | 4U2A | | 14 | 51F9 | |
| | 20 | 0772 | | 15 | AC1A | |
| | 22 | 9635 | | 16 | PH5P | |
| | 24 | 1734 | | 17 | H4UH | |
| | 26 | 8P54 | | U111 | 9 | 28F6 |
| | 28 | Toggleing | | | 10 | 350P |
| | 33 | H62U | | | 11 | 0A71 |
| | 35 | C21A | | | 13 | P674 |
| | 37 | HA07 | | | 14 | PA97 |
| 39 | H0AA | 15 | 2HCO | | | |
| | | 16 | APU9 | | | |
| U104 | 9 | 51H2 | 17 | 4HFA | | |
| | 10 | 56U8 | U112 | 9 | H9P3 | |
| | 11 | 41P8 | | 10 | 9C60 | |
| | 13 | HAP2 | | 11 | 3UC6 | |
| | 14 | U84A | | 13 | CA5A | |
| | 15 | 4H76 | | 14 | 0U2U | |
| | 16 | A29C | | 15 | 54HA | |
| 17 | PU42 | 16 | | U51C | | |
| U105 | 9 | 70HA | 17 | AUPP | | |
| | 10 | 9561 | U113 | 4 | 85PF | |
| | 11 | 99H0 | | 5 | 45F6 | |
| | 13 | 94A9 | | 6 | F02A | |
| | 14 | C057 | | 9 | 4C4C | |
| | 15 | F034 | | 10 | H02C | |
| | 16 | AAC3 | | 11 | 92A8 | |
| 17 | CU98 | U114 | | 13 | 275H | |
| U106 | 9 | | 06C1 | 14 | P5AC | |
| | 10 | | 13UP | 15 | F2U6 | |
| | 11 | | 3AHA | 16 | 62PH | |
| | 13 | | UP7C | 17 | 2U5H | |
| | 14 | | 5C76 | 18 | 8P1F | |
| | 15 | | CC55 | 19 | PFU1 | |
| | 16 | 4U7A | | | | |
| 17 | 36AP | | | | | |

Table A7-7 A7 Signature Analysis Test #4 cont.

| Component | Pin | Signature | Component | Pin | Signature |
|-----------|------|-----------|-----------|------|-----------|
| U202 | 9 | 0F40 | U313 | 13 | FFPA |
| | 10 | 40CF | | 14 | CP3F |
| | 11 | 48H6 | | 15 | 7A70 |
| | 13 | 5CP8 | | 17 | 0000 |
| | 14 | 677H | 18 | 0000 | |
| | 15 | 0769 | U314 | 15 | 7A70 |
| | 16 | 4PF6 | | 16 | 7A70 |
| 17 | 9HC8 | | | | |
| U213 | 2 | 0797 | | | |
| | 3 | 7HP7 | | | |
| | 7 | 2A6H | | | |
| | 10 | 7A8H | | | |
| | 14 | 2H87 | | | |

12. Set all jumpers to normal position.

E. Oscilloscope Signal Waveforms

The oscilloscope plots are used for troubleshooting the A7. Note that all the measurements are taken with a 10:1 probe. Other notes unique to a measurement are written next to the waveform.

WARNING

Service procedures described in this section are performed with the protective covers removed and power applied. Energy available at many points can, if contacted, result in personal injury.

Table A7-8 FPP Waveforms

| Set all jumpers in normal (N) position Connect ground to A7 TP6, A7 TP11 Probe type 10:1 Power On | | |
|---|----------------------|---------------------------------------|
| Setup | Important Parameters | Waveform |
| <p>8 MHz & 4 MHz</p> <p>Connect CH1 to A7 TP3 Connect CH2 to A7 J5-3</p> <p>Oscilloscope:</p> <p>CH1 V/Div 200 mV/Div CH2 V/Div 200 mV/Div CH1 Coupling dc CH2 Coupling dc Time/Div 50 ns/Div Trigger CH 2</p> | <p>Time</p> | <p style="text-align: center;">#1</p> |

F. After-Repair Adjustments and Tests

Table A7-9 After-Repair Adjustments and Tests

| Perform the following: | Section |
|---|---------|
| Diagnostic Tests: FPP FUNCTN TEST ALL | VII |
| Adjustments: None | III |
| Performance Tests: None | II |
| Operational Verification: None | II |

8-11 A8, GLOBAL RAM/DISPLAY CONTROLLER A17, DISPLAY INTERFACE

The information in this section should be used to isolate faulty subblocks on the global RAM and display interface boards. All procedures assume that the fault isolation procedures in section VII have been used to determine that one of these boards has failed and that the circuit descriptions in Section VI are understood.

WARNING

Service procedures described in this section are performed with protective covers removed and power applied. Hazardous voltages in these circuits can cause personal injury if contacted.

CAUTION

Do not insert or remove any circuit board in the HP 3562A while power is on. Power transients caused by insertion or removal may cause damage to circuits on the board being changed or on other boards.

How to use this section

| | |
|---------------------|---|
| Start | Start troubleshooting with part A, Global RAM Diagnostics. Use of this section will isolate the problem to a subblock of A8 or A17. |
| Reference | Refer to Section IX for the component locators and schematics. Refer to figure 4-1 in Section IV for location of cables and boards. Refer to figure 7-4 in Section VII for power-up test codes. |
| After-Repair | Use table A8-10 to determine which adjustments and tests need to be performed to complete instrument service. |

Troubleshooting Hints

1. Global RAM or Display Interface problems can blank or garble the display. The following features simplify fault isolation when the display is not functioning properly:
 - a. Some diagnostic results are annunciated on the A2 LEDs as well as on the 1345A display. Table A8-1 explains the A2 LED fault codes.
 - b. The A2 LEDs will display B7 when the power-up tests and calibration are finished. If this does not occur, refer to section VII, Fault Isolation.
2. The LED at the top of the A8 board (CR1) indicates RFD on the system bus. It is not used to service the A8 board.

A. Global RAM Diagnostics

Disconnect the power cable from the rear panel and remove the top cover. Place the A8 Global RAM on the 03562-66540 extender card. Reconnect the power cord and turn power on. Initiate the Global RAM diagnostic test using the following keystrokes:

```

PRESET      . . . . . RESET (S8)

SPCL FCTN   . . . . . SERVIC TEST . . . . . TEST
                (S2)                MEMORY . . . . . GLOBAL
                                        (S2)                RAM (S1)
    
```

NOTE

If the display is blank or garbled, the softkey menus may be unreadable. Whenever a softkey is used in this section, the softkey number (S1 through S8 from top to bottom) appears in parentheses after the softkey name.

If the GLOBAL RAM test fails, read the test log on the 1345A display and/or the hex code from the A2 LEDs. Use table A8-1 to find the most likely failure or suggested tests to further isolate the problem. Problems in the A8 Display Control section or A17 Display Interface are not detected by the Global RAM test. If the display is blank or garbled but no faults are annunciated on the A2 LEDs or on the display, go to part B, A8/A17 Circuit Block Tests, to further isolate the problem.

Table A8-1 Global RAM Failures

| Failure Type | A2 LEDs | Description | Probable Fault Location | Further Tests |
|--|---------|--|--|---|
| — | B7 | Power-up tests and calibration done; keys active | — | — |
| — | B5 | Starting Global RAM test | — | — |
| 1 | 9N | Global data bus failure bit "N" | Global Bus line "N" (GDN) Global Bus Transceivers (A8U609, U610), other assemblies on the global bus | Chapter 7-5-F, Global Bus Test Table A8-9 #8 |
| 2 | AN | Memory address failure, bit "N"* | A8 U211, U111, U611, U612 | B.3.d |
| 3 | DN | Repeatable memory failure, bit "N" | Dynamic RAM chip associated with failing bit, GD0 through GD15 | — |
| 4 | EN | Nonrepeatable memory failure, bit "N" | Dynamic RAM chip associated with failing bit, GD0 through GD15, address circuit, global bus transceivers | — |
| 5 | 0B | Global RAM refresh failure | Memory Refresh Timer, Arbiter, Refresh Address Counter | B.3.b, B.3.d, B.3.e |
| — | 81 | Global RAM all bits failed, both bytes | Memory control circuit, A8 U307, U308 | B.3.b, B.3.c, B.3.d, B.3.e |
| — | 82 | Global RAM all bits failed, high byte | A8 U610, U307, U308 | Table A8-9 #8, #9 |
| — | 83 | Global RAM all bits failed, low byte | A8 U609, U307, U308 | Table A8-9 #8, #9 |
| *If the problem is after the multiplexer, the LEDs will display only one of the two address bits multiplexed to the affected line. | | | | |

B. A8/A17 Circuit Block Tests

This section includes three groups of tests which will further isolate failures on the A8 and A17 boards. Some of the tests involve signature analysis. The A8 board must be on an extender card for tests 1 and 3.

Test 1, Display Control, tests the Display Direct Memory Access portion of the A8 board. It verifies correct operation of the address and word counters, display refresh counter, and the display controller.

Test 2, Display Interface, covers problems on the A17 board.

Test 3, Global RAM, tests operation of the arbiter, refresh address counter, and memory address sections of A8.

1. Display Control

a. Display Refresh Timer

- Turn on power.
- Using an oscilloscope, check the following clock signals in the Display Refresh Timer circuits block:

| Signal | Frequency |
|--------|-----------|
| CLK | 8 MHz |
| TP3 | 61 Hz |
| SYNC | 61 Hz |

b. Display Controller

Check TP5, TP6, and TP7 for the waveforms shown in table A8-9 -1.

c. Display DMA Address Counters and Drivers

The following signature analysis test verifies correct operation of the Display DMA circuitry.

- Connect the signature analyzer according to table A8-2.

Table A8-2 Display Controller Signature Analyzer Setup

| Signal | Polarity | Connection |
|--------|---------------|------------|
| Ground | | A8 J1-1 |
| Clock | Negative edge | A8 J1-3 |
| Stop | Negative edge | A8 J1-4 |
| Start | Negative edge | A8 J1-5 |

Table A8-4 Display Controller Signature Analysis Test #2

| Signal Name | IC (Pin) | Signature |
|---------------------------------|----------|-----------|
| Address Drivers: Inputs: | U604(11) | UUUU |
| | (12) | 5555 |
| | (13) | CCCC |
| | (14) | 7F7F |
| | (15) | 5H21 |
| | (16) | 0AFA |
| | (17) | UPFH |
| | (18) | 52F8 |
| | U605(11) | HC89 |
| | (12) | 2H70 |
| | (13) | HPP0 |
| | (14) | 1293 |
| | (15) | HAP7 |
| | (16) | 3C96 |
| | (17) | 3827 |
| | (18) | 755U |

- If the signatures are correct, go to test e, Display DMA Word Counters. If any signatures are incorrect, check the corresponding address counter output. If the signature is correct at the word counter and incorrect at the driver, the problem is a board trace or solder joint. If the signature is also incorrect at the word counter, proceed with step d, Display DMA Address Counters.

d. Display DMA Address Counters

Perform this test only if a failure was found in performing the signature analysis in table A8-4. This test verifies that the address counters are loading correctly. If loading fails, either a data receiver, counter, or board trace is the probable cause of the failure.

- If jumpers A8 J3 and J4 are not in the normal (N) position, turn off power, move jumpers to normal position, and turn power on.
- Press the following key sequence on the HP3562A:

```

SPCL FCTN      . . . . . SERVIC TEST  . . . . . TEST
                (S2)                    MEMORY  . . . . . DSPINT
                (S2)                    TEST 1 (S3)
    
```

The A2 LEDs should display hex B8.

NOTE

The display will blank during the Display Interface tests and the special function menu will disappear.

- Move jumpers A8J3 and A8J4 to the test (T) position.
- Press softkey S4 (A2 LEDs display B9). This loads a hex A into each of the four display address counters (A8 U600 through U603).
- Probe the output pins of U600 through U603. The output of each counter should be hex A (binary 1010, pins 11, 12, 13, and 14).
- Turn off power.
- Move jumpers A8J3 and A8J4 to the normal (N) position.
- Turn on power.
- Press the 3562A keys as follows:

| | | | | | |
|------------------|-------|-------------|-------|--------|--------------|
| SPCL FCTN | | SERVIC TEST | | TEST | |
| | | (S2) | | MEMORY | DSPINT |
| | | | | (S2) | TEST 1 (S3) |

A2 LEDs should display hex B8

- Move jumpers A8J3 and A8J4 to the test (T) position.
 - Press softkey S5 (A2 LEDs display BA). This loads a hex 5 into each of the Display Address Counters (U600 through U603), toggling each bit from the previously loaded hex A.
 - Probe the output pins of U600 through U603. The output of each counter should be hex 5 (binary 0101, pins 11, 12, 13, and 14).
 - Turn off power.
 - Move jumpers A8J3 and A8J4 to the normal (N) position.
- e. Display DMA Word Counters
- Check U501 pin 15 (TCL). The signature should be 6U29. If this signature is incorrect, check the signatures in table A8-5. If any word counter signatures are incorrect, verify that data is getting to the counter inputs and that the signal WLOADL is toggling.

Table A8-5 Display Controller Signature Analysis Test #3

| Signal Name | IC (Pin) | Signature |
|-----------------------|----------|-----------|
| Word Counter Outputs: | U400(15) | P762 |
| | (14) | UUUP |
| | (13) | 5554 |
| | (12) | CCCA |
| | (11) | 7F7H |
| | U401(15) | 6F9C |
| | (14) | 5H20 |
| | (13) | 0AFC |
| | (12) | UPFF |
| | (11) | 52F9 |
| | U501(14) | HC88 |
| | (13) | 2H71 |
| | (12) | HPP1 |
| (11) | 1292 | |

- Turn power off.
- Move jumpers A8J3 and A8J4 to normal (N) position.

f. If these tests pass, the cause of failure is probably on the A17 Display Interface board.

2. Display Interface

Because of the relative cost of the A17 board and troubleshooting time, it is recommended that this board be replaced if defective.

3. Global RAM

a. Setup for Global RAM tests

- Turn off power.
- Move A8J5, J6, J7, J8, and J9 to test (T) position. Jumper J5 disconnects the memory request lines from the arbiter and routes the output from the refresh address counter into the arbiter. This generates every possible combination of requests to the arbiter. The other jumpers affect various control lines (see schematic, figure 9-A8a).
- Connect the signature analyzer according to table A8-6.

Table A8-6 Global RAM Signature Analyzer Setup

| Signal | Polarity | Connection |
|--------|---------------|------------|
| Ground | | A8 J2-1 |
| Clock | Negative edge | A8 J2-3 |
| Stop | Negative edge | A8 J2-4 |
| Start | Negative edge | A8 J2-5 |

- Turn on power.

b. Memory Refresh Timer

- Set up equipment as described in part 3.a above.
- Using an oscilloscope, check the waveforms at the following locations:

| Location | Waveform |
|----------|-------------------------|
| U405(3) | BUS EN 2, table A8-9 #6 |
| U405(5) | 1.06 MHz square wave |
| U404(14) | 1.06 MHz square wave |
| U404(4) | 118 kHz positive pulses |
| U404(11) | 118 kHz negative pulses |

c. Global Timing

- Set up equipment as described in part 3.a above.
- Using an oscilloscope, check the following signals in the global timing circuit block:
 - B2GDSL table A8-9 #5
 - GDSL table A8-9 #5
 - GSMP table A8-9 #6

If any of these signals are incorrect, check the inputs (pin 1) and tapped outputs of the delay lines (U311, U312, and U411) for 2.13 MHz square waves.

d. Refresh Address Counters/Memory Address Drivers

- Set up the equipment as directed in section 3.a above.
- Check the signatures in table A8-7.

Table A8-7 Global RAM Signature Analysis Test #1

| Signal Name | IC (Pin) | Signature |
|--|----------|-----------|
| +5 | | CC34 |
| Counter Outputs: | | |
| C0 | U512(16) | 96PF |
| C1 | (15) | 725C |
| C2 | (14) | P5PH |
| C3 | (13) | 5CP0 |
| C4 | U511(16) | 7P25 |
| C5 | (15) | 85PA |
| C6 | (14) | 77F7 |
| C7 | (13) | 6PCP |
| Memory Address Drivers: | | |
| C0 | U111(13) | 96PF |
| C1 | (2) | 725C |
| C2 | (5) | P5PH |
| C3 | (9) | 5CP0 |
| C4 | U211(9) | 7P25 |
| C5 | (12) | 85PA |
| C6 | (5) | 77F7 |
| C7 | (2) | 6PCP |
| MA0 | U111(11) | 2HH8 |
| MA1 | (3) | F96U |
| MA2 | (6) | 5PH9 |
| MA3 | (8) | P0H4 |
| MA4 | U211(8) | F511 |
| MA5 | (11) | 3PHP |
| MA6 | (6) | FFU3 |
| MA7 | (3) | H58A |
| Memory Address lines: | | |
| MA0* | U110(5) | 2HH8 |
| MA1* | (7) | F96U |
| MA2* | (6) | 5PH9 |
| MA3* | (12) | P0H4 |
| MA4* | (11) | F511 |
| MA5* | (10) | 3PHP |
| MA6* | (13) | FFU3 |
| MA7* | (9) | H58A |
| * These eight signatures should be the same for corresponding pins on U103 through U109 and U203 through U210. | | |

e. Arbiter

- Set up equipment as directed in section 3.a. above.
- Verify that the outputs of U508 (pins 12 through 18) are all high (J5 disables U508).
- Check the clock signals for U506 and U507. The correct waveforms are shown in table A8-9 #6.
- Check the signatures in table A8-8:

Table A8-8 Global RAM Signature Analysis Test #2

| Signal Name | IC (Pin) | Signature |
|---------------------------|----------|-----------|
| IDLE | U509(2) | 6493 |
| MGB2D2L | (3) | 7820 |
| MGFPP | (4) | CPA9 |
| MG68L | (5) | 31H6 |
| MGDF1 | (6) | 9502 |
| MGDF2L | (7) | 0CC1 |
| MGFFT | (8) | 96PF |
| MGRFSL | (9) | 20A7 |
| MGRFSH | (11) | 20A7 |
| MGFFTL | (12) | 96PF |
| MGDF2 | (13) | 0CC1 |
| MGDF1L | (14) | 9502 |
| IMG68L | (15) | 31H6 |
| MGFPPL | (16) | CPA9 |
| MGB2D2 | (17) | 7820 |
| IDLEL | (18) | 6493 |
| Priority Decoder outputs: | | |
| YA | U506(19) | 2HH8 |
| YB | (18) | 2P36 |
| YC | (17) | C085 |
| YD | (16) | 9C93 |
| YE | (15) | F314 |
| YF | (14) | 059H |
| YG | (13) | 8AP2 |
| YH | (12) | HUA7 |

C. Oscilloscope Signal Waveforms

The oscilloscope plots are used for troubleshooting the A8 Global RAM board. Note that all measurements are done with a 10:1 probe. Other notes unique to a measurement are listed next to the waveform.

Table A8-9 Global RAM Signal Waveforms

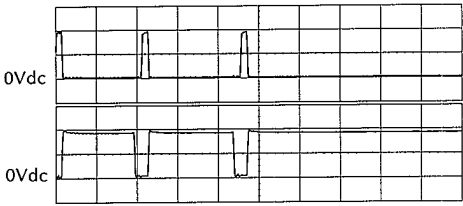
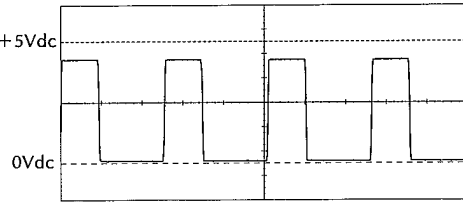
| <p>TP7, TP5 & 6</p> <p>All jumpers in normal (N) position. Power on.</p> | | |
|--|--------------------------|---|
| Setup | Important Parameters | Waveform |
| <p>Connect Ch1 to A8 TP7 Connect Ch2 to A8 TP5 or TP6</p> <p>Scale 2 V/div</p> <p>Timebase 2 μs/div</p> <p>Offset 2 V</p> <p>Trigger Ch 1</p> <p>Coupling dc</p> | <p>Time Polarity</p> |  <p>#1 This series of pulses repeats every 16.4 ms.</p> |
| <p>B2D2 DSA STOP/START</p> <p>Power on. Press the following HP 3562A key sequence:</p> <p>SPCL FCTN SERVIC TEST (S2) TEST MEMORY (S2) DSPINT TEST 1 (S3)</p> <p>Move jumpers A8 J3 and J4 to test (T) position.</p> <p>Press softkey S6.</p> | | |
| Setup | Important Parameters | Waveform |
| <p>Connect Ch 1 to A8 J1(4)</p> <p>Scale 1 V/div</p> <p>Timebase 200 ms/div</p> <p>Offset 2 V</p> <p>Trigger Ch 1</p> <p>Coupling dc</p> | <p>Time</p> |  <p>#2</p> |

Table A8-9 Global RAM Signal Waveforms cont.

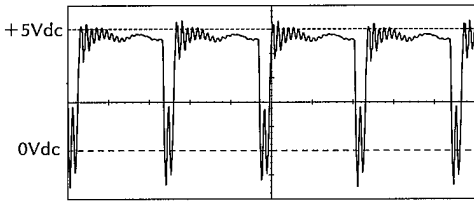
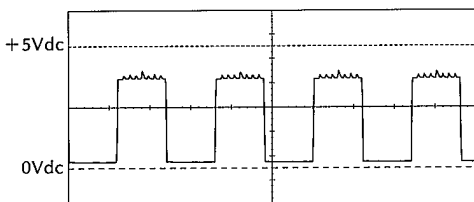
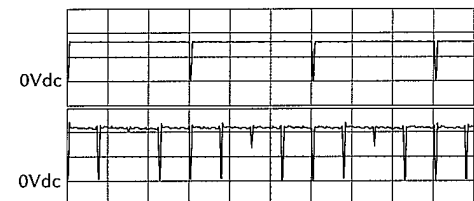
| #3 — #9 Power off. Jumpers A8 J3 and J4 to normal (N) position. Jumpers A8 J5, J6, J7, J8, and J9 to test (T) position. Power on. | | |
|--|----------------------|--|
| Setup | Important Parameters | Waveform |
| <p>GRAM DSA CLOCK</p> <p>Connect Ch1 to A8 J2(3)</p> <p>Scale 1 V/div</p> <p>Timebase 200 ns/div</p> <p>Offset 2 V</p> <p>Trigger Ch 1</p> <p>Coupling dc</p> | Time |  <p>#3</p> |
| <p>GRAM DSA STOP/START</p> <p>Connect Ch 1 to A8 J2(4)</p> <p>Scale 1 V/div</p> <p>Timebase 50 μs/div</p> <p>Offset 2.5 V</p> <p>Trigger Ch 1</p> <p>Coupling dc</p> | Time |  <p>#4</p> |
| <p>B2GDSL, GDSL</p> <p>Connect Ch 1 to U301(8)</p> <p>Connect Ch 2 to U306(8)</p> <p>Scale 2 V/div</p> <p>Timebase 5 μs/div</p> <p>Offset 2 V</p> <p>Trigger Ch 1</p> <p>Coupling dc</p> | Time |  <p>#5</p> |

Table A8-9 Global RAM Signal Waveforms cont.

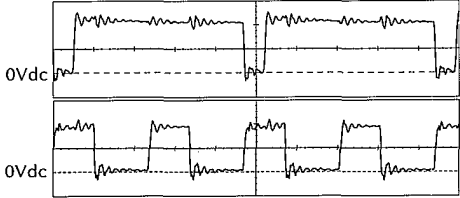
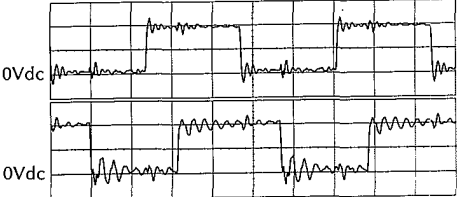


| Setup | Important Parameters | Waveform |
|--|--------------------------------------|--|
| <p>BUS EN 2, GSMP</p> <p>Connect Ch 1 to U409(8) Connect Ch 2 to U309(3)</p> <p>Scale 2 V/div</p> <p>Timebase 100 ns/div</p> <p>Offset 2 V</p> <p>Trigger Ch 1</p> <p>Coupling dc</p> | <p>Time</p> <p>Time relationship</p> |  <p>#6</p> |
| <p>MRAS, MCAS</p> <p>Connect Ch 1 to U307(2) Connect Ch 2 to U308(4)</p> <p>Scale 2 V/div</p> <p>Timebase 100 ns/div</p> <p>Offset 2 V</p> <p>Trigger Ch 1</p> <p>Coupling dc</p> | <p>Time</p> <p>Time relationship</p> |  <p>#7</p> |
| <p>CD, RAMGR/GWL</p> <p>Lower byte: Connect Ch 1 to U609(9) Connect Ch 2 to U609(11)</p> <p>Upper byte: Connect Ch 1 to U610(9) Connect Ch 2 to U610(11)</p> <p>Scale 2 V/div</p> <p>Timebase 200 ns/div</p> <p>Offset 2 V</p> <p>Trigger Ch 1</p> <p>Coupling dc</p> | <p>Time</p> <p>Time relationship</p> |  <p>#8</p> |

Table A8-9 Global RAM Signal Waveforms cont.

| Setup | Important Parameters | Waveform |
|--|--------------------------------------|--|
| <p>RASLL/RASUL, CASLL/CASUL</p> <p>Lower byte (RASLL, CASLL): Connect Ch 1 to U103(4) Connect Ch 2 to U103(15)</p> <p>Upper byte (RASUL, CASUL): Connect Ch 1 to U203(4) Connect Ch 2 to U203(15)9</p> <p>Scale 2 V/div Timebase 100 ns/div Offset 2 V Trigger Ch 1 Coupling dc</p> | <p>Time</p> <p>Time relationship</p> |  <p>#9</p> |

D. After-Repair Adjustments and Tests

Table A8-10 After-Repair Adjustments and Tests

| Perform the following: | Section |
|--|------------|
| <p>Diagnostic Tests:</p> <p>Test All</p> | <p>VII</p> |
| <p>Adjustments:</p> <p>None</p> | |
| <p>Performance Tests:</p> <p>None</p> | |

8-12 HP 1345A DISPLAY

The HP 1345A display is a stand alone digital display. Use the HP 1345A service manual included with the instrument to service the display. To verify the display is failing, set jumper A17 W1 to the test (T) position. The pattern displayed should be the same as shown in figure D-1. To remove the display from the instrument perform steps 1 through 8:

1. Disconnect the main power cord from the rear panel and remove the top cover.
2. Remove the internal shield covering the display unit.
3. Remove the trim strips from the front frame.
4. Remove the front frame and side panel screws as shown in figure D-2.
5. Remove the screws that attach the display to the instrument as shown in figure D-2.
6. Remove the two screws attaching the display adjustments to the rear panel of the instrument.
7. Disconnect the display power cable (W11).
8. Disconnect the display interface cables (W14, W190, W191, W192). The display can now be pulled from the front of the instrument.

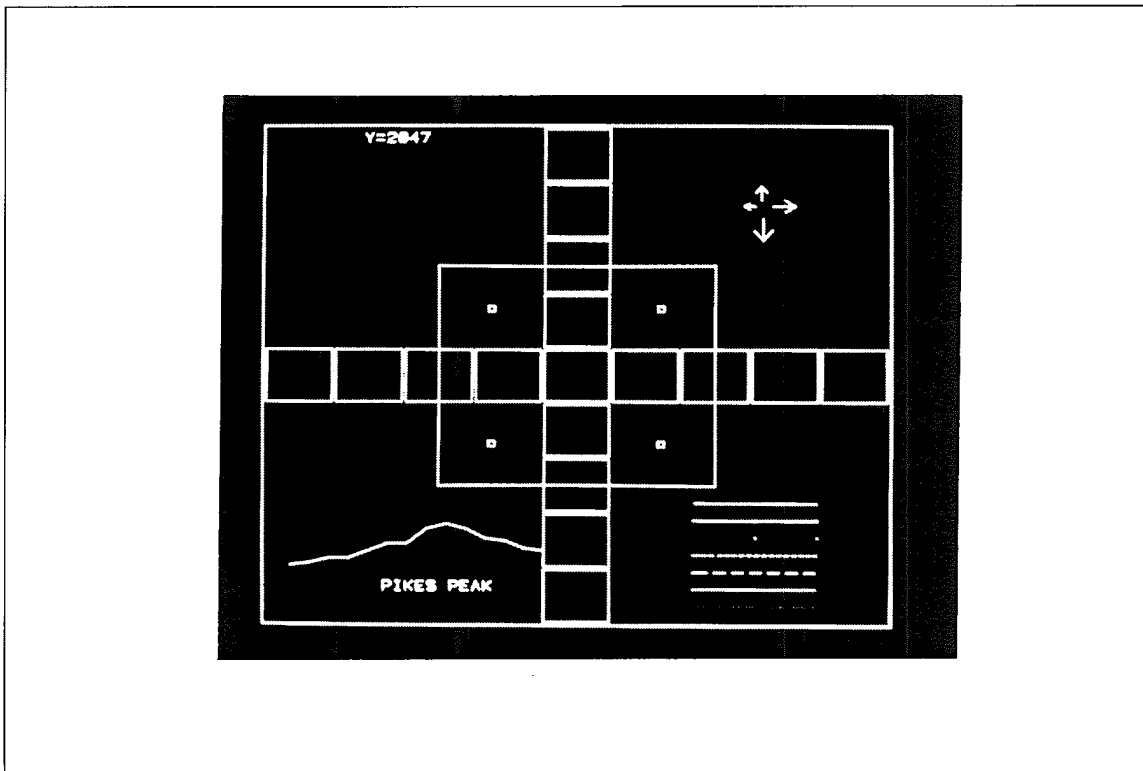


Figure D-1 Display of Verification Pattern

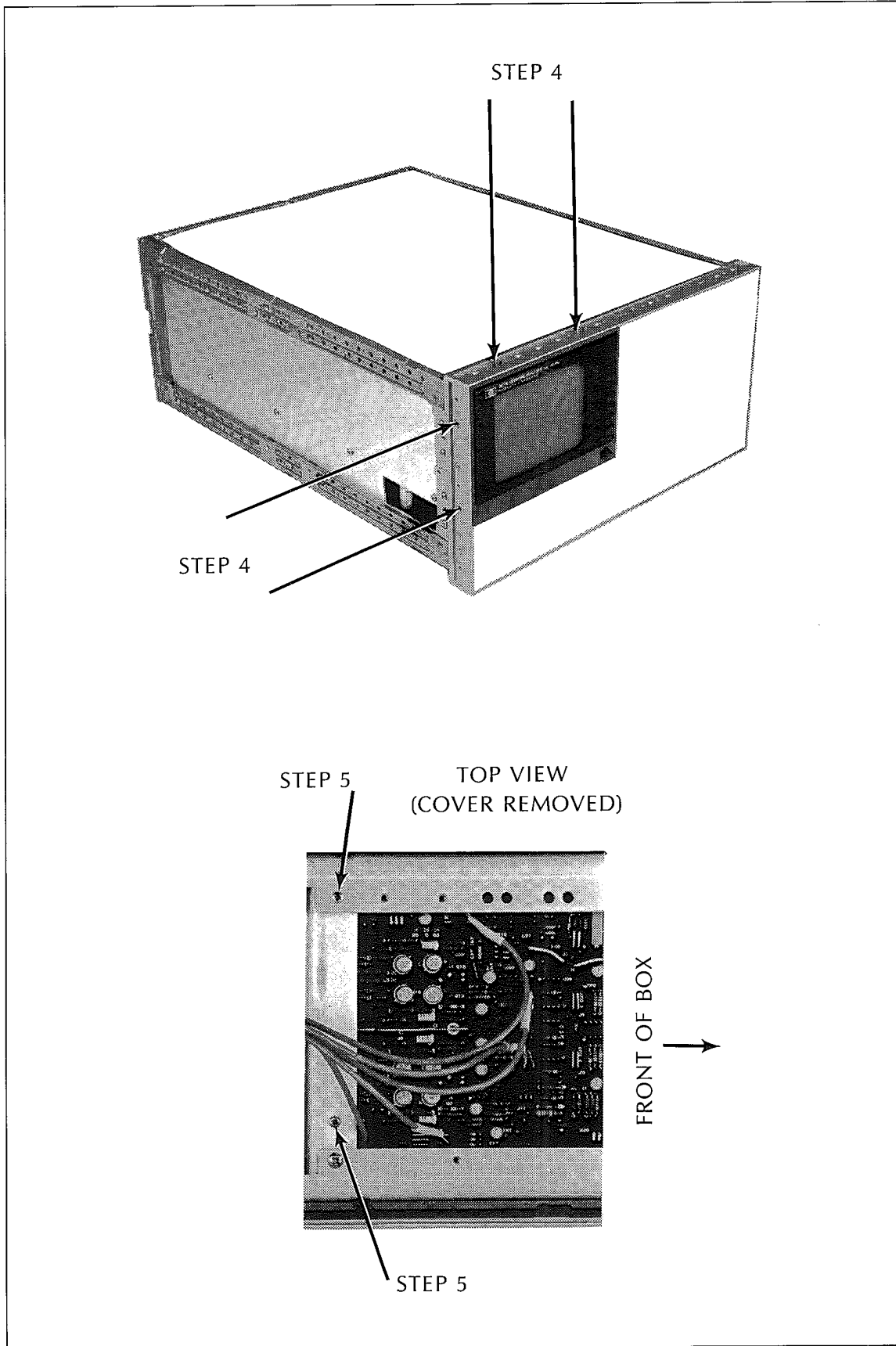


Figure D-2 HP 3562A Removal

8-13 A9, FAST FOURIER TRANSFORM (FFT) PROCESSOR

The information in this section should be used to isolate faulty subblocks on the FFT board. All procedures assume that you have used the fault isolation procedures in Section VII to determine that this board has failed and that you have read and understand the circuit descriptions in Section VI.

WARNING

Service procedures described in this section are performed with protective covers removed and power applied. Hazardous voltages in these circuits can cause personal injury if contacted.

CAUTION

Do not insert or remove any circuit board in the HP 3562A while power is on. Power transients caused by insertion or removal may cause damage to circuits on the board being changed or on other boards.

How to use this section

| | |
|---------------------|---|
| Start | To troubleshoot the FFT board, use the FFT diagnostic tests to further isolate the problem. Circuit descriptions in Section VI provide the background for understanding how the FFT board circuits work. |
| Procedure | Once the problem has been localized to a block of circuits, one of the three digital signature analysis (DSA) tests should be used to troubleshoot individual circuits. Waveforms are provided in table A9-7 to demonstrate the correct appearance of the DSA clock and start/stop signals. |
| Reference | Refer to Section IX for the component locator and schematic. Refer to figure 4-1 in Section IV for the location of cables and boards. |
| After-Repair | Use table A9-8 to determine which adjustments and tests need to be done to complete instrument service. |

Troubleshooting Hints

1. The FFT status LEDs should be OFF during normal operation. They are not used to service the board.
2. A major portion of the FFT process is addressing. Be sure you understand which parts of the circuit are part of the addressing block. Refer to the block diagrams in the circuit descriptions in Section VI.

A. FFT Diagnostics

The diagnostic tests for the FFT board allow you to test groups of circuits to further isolate a problem. A subset of the FFT diagnostic tests run when the instrument power is turned ON, during SELF TEST, or during TEST ALL. Display the FFT-diagnostic test menu using the following sequence of keystrokes:

```

PRESET      . . . . . RESET

SPCL FCTN   . . . . . SERVIC TEST . . . . . TEST PROC . . . . . TEST FFT

```

The menu now contains the following entries of FFT diagnostics tests:

```

FFT FUNCTN
FFT STATUS
FFT INTRPT
FFT RAM
FFT ROM
FFT GL INTFC

```

Details of each test follows:

FFT FUNCTION TEST

This test performs all the tests found in the rest of the menu (status, interrupt, RAM, ROM, and global interface tests). It also exercises the FFT functions by performing a forward and a reverse FFT, and Hanning, uniform, flattop, and user-defined windows on a known block of data. The resulting checksum is compared to a known value by the CPU.

If the FFT function test fails but the analyzer appears to work correctly when analyzing a fixed sine signal and all the rest of the diagnostic tests for this board pass, investigate the pseudorandom number generation block. It is reset prior to doing the math for the special functions of this test so that the resultant checksum is repeatable. If the PRN generator is not reset or does not operate correctly, the checksum generated won't always agree with the stored checksum.

The FFT function test is the most extensive diagnostic test available to test the FFT board. It is executed as a subset of the tests performed whenever the SELF TEST and TEST ALL tests are run.

FFT STATUS TEST

This test quickly checks the operation of the system bus operation between the CPU and the FFT boards. The CPU addresses the FFT board and loads a command to it which causes the FFT microprocessor to return the CPU command data. This tests the system interface circuits (in both directions), the internal data bus, the FFT microprocessor system, the transceiver between the TMS320 microprocessor and the internal data bus, and both interrupt circuits. If this test passes you know that the CPU can talk to the FFT microprocessor and the FFT microprocessor can interpret commands and respond (talk) to the system CPU.

FFT INTERRUPT TEST

This test checks the ability of the FFT board to interrupt the main system CPU and exercises the addressing and global bus circuits. The CPU interrupt must occur within a limited time. Two results are listed if this test is successful: the timeout test (called the "Interrupt Registered" results) and the exercise routine results (called the "FFT Interrupt" results). The test runs as follows:

1. The system CPU (A2) loads a command into a register on the FFT board and starts a timer.

This action utilizes the system bus interface circuits and the FFT interrupt circuit on the FFT board.

2. The FFT microprocessor system interprets the command,
3. stores two numbers (5555H and AAAAH) in the scale factor registers in global RAM and
4. activates the CPU interrupt.

This action utilizes the FFT addressing circuitry, the global bus address and data interface circuits, and the CPU interrupt circuit on the FFT board.

5. If the system CPU receives the interrupt from the FFT board before the end of the timer cycle, the "FFT Interrupt Registered" test passes.
6. The CPU checks the numbers stored in RAM against a known number. If the numbers are identical, the "FFT Interrupt" test passes.

FFT RAM TEST

This test is a self-test run by the TMS320 FFT microprocessor on its own internal RAM. The test program resides in ROM in the FFT microprocessor system. The system CPU addresses the FFT board and loads a command to run the RAM test. After the test is complete the FFT board interrupts the system CPU and passes the test results (pass or fail) back to the CPU.

The system interface and both the FFT and CPU interrupt circuits are exercised as a by-product of this test.

FFT ROM TEST

Each of the program and coefficient ROMs have a checksum number in the last byte. When the ROM test is run the system CPU reads the ROMs, generates its own checksum and compares it with the checksum stored in the program and coefficient ROMs.

To read the contents of the FFT ROMs, the CPU sends instructions to the FFT board causing it to place the ROM contents, one word at a time, into a specific location in global RAM where the CPU can access the data. The FFT board changes contents of another location of global RAM to zero each time it completes the transfer of a word. The CPU monitors this second location for an indication of valid data in the first location.

The system and global interface blocks are exercised as a by-product of this test.

GLOBAL INTERFACE TEST

This tests moves (copies) a block of data from one area of global RAM to another area. It exercises both interrupt circuits and the address circuitry besides testing the global interface circuits.

The CPU instructs the FFT to do a block move, waits for the FFT to signal that it has finished the process, and then compares values of the two areas of RAM to determine whether the data copied is identical to the original data.

B. A9 Signature Analysis Tests

There are three digital signature tests designed to test the digital circuits on the FFT board. These tests are referred to by number as tests 1, 2, and 3.

Test 1 tests the program ROMs (U301 and U303) and, to a limited extent, the TMS320 microprocessor. See table A9-2 for the signatures of test 1. With J3 and J4 in the test position (marked with a "T") the ROM output lines are disconnected and the TMS320 data lines are grounded. This test may be used to test the input and output signals of the ROM integrated circuits. The operation of the microprocessor is partially verified by this test because the address line outputs of the TMS320 are identical to the ROM input lines.

Test 2 may be used to test most of the circuits on the FFT board. The only exceptions are the global bus interface circuits. These require a special clock and are covered in test 3.

Test 3 may be used to test the global bus interface circuits (U511 through U516) and the coefficient ROM outputs (U315 and U317). This test uses the memory grant signal on test point 3 as a clock. See the table for test 3.

Perform the following steps to configure the instrument for any of the three digital signature tests:

- Disconnect the power cable.
- Put the FFT board on an extender card. All jumpers should be in the normal (N) position.
- Select the signature test you wish to perform.
- Connect and configure the signature analyzer as described in the table at the beginning of the test you wish to perform.
- Connect the power cable and turn on power.

1. Digital Signature Test 1

Table A9-1 FFT Signature Analyzer Setup #1

| Signal | Polarity | Connection |
|--------|----------|------------|
| Ground | | A7 J5-1 |
| Clock | Neg edge | A7 J5-3 |
| Stop | Neg edge | A7 J5-4 |
| Start | Pos edge | A7 J5-5 |

Test 1 is activated by performing the following steps:

- a. Move jumpers J3 and J4 to the test (T) position.
- b. Move jumper J1 to the TST2 position.
- c. Press the reset switch on the CPU board (A2 S1).

Table A9-2 FFT Signature Analysis Test #1

| Component | Pin | Signature | Component | Pin | Signature |
|-------------------------------------|------|-----------|--------------------------------|-----|-----------|
| U301 and U303 address (input) lines | 8 | H62U | U303 only; data (output) lines | 9 | 366P |
| | 7 | C21A | | 10 | 2UFH |
| | 6 | HA07 | | 11 | F7A2 |
| | 5 | H0AA | | 13 | O51O |
| | 4 | P030 | | 14 | O637 |
| | 3 | 4442 | | 15 | 2AA9 |
| | 2 | 4U2A | | 16 | CAPA |
| | 1 | 0772 | | 17 | O442 |
| | 23 | 9635 | | | |
| | 22 | 1734 | | | |
| | 21 | 8P54 | | | |
| U301 only; data (output) lines | 9 | 8551 | | | |
| | 10 | 91CO | | | |
| | 11 | 3COC | | | |
| | 13 | U6H7 | | | |
| | 14 | 6P56 | | | |
| | 15 | 29C5 | | | |
| 16 | CFPC | | | | |
| 17 | A484 | | | | |

Return all jumpers to the normal (N) position (either position OK for J1).

2. Digital Signature Test 2

Table A9-3 FFT Signature Analyzer Setup #2

| Signal | Polarity | Connection |
|--------|----------|------------|
| Ground | | A7 J5-1 |
| Clock | Neg edge | A7 J5-3 |
| Stop | Neg edge | A7 J5-4 |
| Start | Pos edge | A7 J5-5 |

Test 2 is activated by performing the following steps:

- a. Move jumper J2 to the test (T) position.
- b. Move jumper J1 to the TST1 position.
- c. Press the reset switch on the CPU board (A2 S1).

Table A9-4 FFT Signature Analysis Test 2

| Signal name | IC (pin) | Signature | Signal name | IC (Pin) | Signature |
|--------------------|----------|-----------|-----------------------|----------|-----------|
| TMS320 data lines: | | | Port decoder inputs: | | |
| D0 | U103(26) | 31HP | | U216(1) | 1894 |
| D1 | (25) | F8F2 | | (2) | O8O6 |
| D2 | (24) | O6FO | | (3) | 9271 |
| D3 | (23) | OO1P | | (6) | P23A |
| D4 | (22) | U7P8 | | (4) | A712 |
| D5 | (21) | 52O4 | | (5) | 3P7P |
| D6 | (20) | O746 | | | |
| D7 | (19) | 118O | | U217(1) | 1894 |
| D8 | (11) | 9376 | | (2) | O8O6 |
| D9 | (12) | P682 | | (3) | 9271 |
| D10 | (13) | 349C | | (6) | P23A |
| D11 | (14) | O53U | | 4) | O865 |
| D12 | (15) | UA51 | Port decoder outputs: | | |
| D13 | (16) | HPH7 | | | |
| D14 | (17) | FO91 | SIRQSYSL | U216(15) | P23A |
| D15 | (18) | 77HP | GDBOUTL | (14) | OHPC |
| Internal data bus: | | | | (13) | 29FF |
| IDB0 | U503(18) | 31HP | SDBUSOUTL | (12) | P23A |
| IDB1 | (14) | F8F2 | LDHWCRLL | (11) | O8O7 |
| IDB2 | (16) | O6FO | LDCTR2L | (10) | 5P63 |
| IDB3 | (17) | OO1P | LDPGSL | (9) | PC2U |
| IDB4 | (15) | U7P8 | | (7) | P23A |
| IDB5 | (11) | 5204 | RIRQSYSL | U217(15) | P23A |
| IDB6 | (13) | O746 | GDBINL | (14) | 2465 |
| IDB7 | (12) | 1180 | PROMINL | (13) | 9CAU |
| IDB8 | U403(18) | 9376 | SDBUSINL | (12) | P23A |
| IDB9 | (17) | P682 | SABUSINL | (11) | P23A |
| IDB10 | (16) | 349C | | (10) | P23A |
| IDB11 | (15) | O53U | CLRSCALEL | (9) | AH5F |
| | | | BFSUBADL | (7) | U8F9 |
| IDB12 | (14) | UA51 | | | |
| IDB13 | (13) | HPH7 | | | |
| IDB14 | (12) | FO91 | | | |
| IDB15 | (11) | 77HP | | | |

Table A9-4 FFT Signature Analysis Test 2 cont.

| Signal name | IC (pin) | Signature | Signal name | IC (Pin) | Signature |
|--|----------|-----------|-----------------------------|----------|-----------|
| I/O Sequencer: | | | Hardware Control Registers: | | |
| SEQSEL0 | U117(9) | OCA9 | IDB15 | U406(2) | 77HP |
| SEQSEL1 | (8) | A107 | IDB14 | (3) | FO91 |
| REALDATA | (7) | OCO3 | IDB13 | (4) | HPH7 |
| TWOCH | (6) | 171A | IDB12 | (5) | UA51 |
| GDINEMPTY | (5) | 6476 | IDB11 | (6) | O53U |
| GDOUTRDY | (4) | PUH1 | IDB10 | (7) | 349C |
| PASSDONE | (3) | 6O52 | IDB9 | (8) | P682 |
| DIDONE | (2) | A7C1 | IDB8 | (9) | 9376 |
| FFTMR | (27) | * | LDHWCR | (11) | O8O7 |
| FFTMG | (26) | * | WINLOC | (19) | 7OP3 |
| WINLOC | (25) | 7O3P | BNKSEL | (18) | AAF4 |
| PASSBIT0 | (22,10) | 14AA | SWAP | (17) | P41A |
| CTR1ENL | (21,13) | 4POA | CTR2DNL | (16) | 8C22 |
| | (20) | P23A | TWOCH | (15) | 171A |
| | (1) | OOOO | REALDATA | (14) | OCO3 |
| | (19) | PA3H | SEQSEL1 | (13) | A107 |
| WINDPGL | (17) | FU43 | SEQSEL0 | (12) | OAC9 |
| FFTWR | (16) | 9758 | IDB7 | U405(2) | 118O |
| POSTINCL | (15) | 15FU | IDB6 | (3) | 0746 |
| REQGBL | (12) | 3176 | IDB5 | (4) | 5204 |
| LDCAL | (11) | 3H4O | IDB4 | (5) | U7P8 |
| * use test 3 for signatures of these signals | | | IDB3 | (6) | OO1P |
| Sequence decoder: | | | IDB2 | (7) | O6FO |
| SEQSEL1 | U115(1) | A107 | IDB1 | (8) | F8F2 |
| SEQSEL0 | (2) | OAC9 | IDB0 | (9) | 31HP |
| CTR2DNL | (3) | 8C22 | LDHWCR | (11) | 0807 |
| CTR1ENL | (4) | 4POA | LEV2 | (19) | PACU |
| POSTINCL | (5) | 15FU | LEV1 | (18) | F167 |
| CLKOUTL | (6) | OOOO | LEV0 | (17) | H441 |
| REQGBL | (7) | 3176 | TBSEL2 | (16) | F789 |
| FFTWR | (8) | 9758 | TBSEL1 | (15) | 815H |
| CTRB11 | (9) | 8OUA | TBSEL0 | (14) | 3A5O |
| W11 | (11) | 2U78 | SCALE1 | (13) | C1CP |
| CLRRDYL | (19) | P8PO | SCALE0 | (12) | 8H36 |
| CLREMPYL | (18) | 7228 | | | |
| FA11 | (17) | H351 | | | |
| INC1L | (15) | 4348 | | | |
| DEC2L | (14) | U42A | | | |
| INC2L | (13) | A2AH | | | |

Table A9-4 FFT Signature Analysis Test 2 cont.

| Signal name | IC (pin) | Signature | Signal name | IC (Pin) | Signature | |
|--------------------------------|------------|-----------|-------------------------------|----------|-----------|------|
| Pseudo Scale: | | | Global Address Bus Interface: | | | |
| IDB8 | U305(5) | 9376 | FA15 | U512(2) | 9993 | |
| IDB9 | (6) | P682 | FA14 | (3) | 2O88 | |
| IDB10 | (7) | 349C | FA13 | (4) | 3FU7 | |
| IDB11 | (4) | O53U | FA12 | (5) | O8P8 | |
| IDB12 | (3) | UA51 | FA11 | (6) | H351 | |
| IDB13 | (2) | HPH7 | FA10 | (7) | 6739 | |
| IDB14 | (1) | FO91 | FA9 | (8) | 1P6P | |
| IDB15 | (15) | 77HP | FA8 | (9) | C9O4 | |
| | (12) | 8O9O | REQGBL | (11) | 3176 | |
| | (11) | 54H8 | | | | |
| CLRSCALEL | U208(5,11) | AH5F | FA7 | U511(2) | 5C91 | |
| GDBOUTL | (4,12) | OHPC | FA6 | (3) | H289 | |
| | | | FA5 | (4) | F6C8 | |
| DIVBY4 | (7) | 1384 | FA4 | (5) | 444H | |
| DIVBY2 | (9) | H4UC | | | | |
| Pseudorandom Number Generator: | | | FA3 | (6) | 85PP | |
| | | | FA2 | (7) | 46C7 | |
| | | | FA1 | (8) | 7H94 | |
| | | | FA0 | (9) | 4282 | |
| CLRPRNL | U105(9) | P1HF | Global Data Bus Interface: | | | |
| GDBOUTL | (12) | OHPC | IDB15 | U516(2) | U515(19) | 77HP |
| | (11) | 284A | IDB14 | (3) | (18) | F091 |
| PRN | (14) | 5828 | IDB13 | (4) | (17) | HPH7 |
| | | | IDB12 | (5) | (16) | UA51 |
| | U106(11) | 8H75 | | | | |
| | (5) | 21U9 | IDB11 | (6) | (15) | O53U |
| | U107(11) | 5H4P | IDB10 | (7) | (14) | 349C |
| | U108(11) | F61F | IDB9 | (8) | (13) | P682 |
| | | | IDB8 | (9) | (12) | 9376 |
| | U108(4) | PC89 | | | | |
| | U408(11) | FA7O | IDB7 | U514(2) | U513(19) | 118O |
| Test Bit Mux: | | | IDB6 | (3) | (18) | O746 |
| DIVBY4 | U206(2) | 1384 | IDB5 | (4) | (17) | 52O4 |
| DIVBY2 | (1) | H4UC | IDB4 | (5) | (16) | U7P8 |
| PASSDONE | (15) | 6052 | | | | |
| PRN | (13) | 5828 | IDB3 | (6) | (15) | OO1P |
| | | | IDB2 | (7) | (14) | O6FO |
| | (5) | A251 | IDB1 | (8) | (13) | F8F2 |
| | | | IDB0 | (9) | (12) | 31HP |

Table A9-4 FFT Signature Analysis Test 2 cont.

| Signal name | IC (pin) | Signature | Signal name | IC (Pin) | Signature |
|--------------------------------|----------------------------------|------------------------------|----------------------------------|-------------------------------|------------------------------|
| Counter One: | | | Counter Two continued: | | |
| LDCTR2L | U209(13) (12) (11) (10) | UU11 OCA2 A172 5P63 | IDB4 LDCTR2L | (15) (11) (4) (5) | U7P8 5P63 21AP 3HA8 |
| PASSDONE DIDONE | (3) (2) (1) (15) | 6O52 A7C1 A512 U9F5 | | (13) (12) (7) (6) | CPH4 PP8P 56O3 U4C2 |
| LDCTR2L | U210(13) (11) (10) (9) | UU11 A172 5P63 OCA2 | IDB3 IDB2 | (2) (3) U409(9) (10) | 662A 83C6 OO1P O6FO |
| | (7) (6) (5) (4) | 958O C207 859C 653O | IDB1 IDB0 LDCTR2L DEC2L | (1) (15) (11) (4) | F8F2 31HP 5P63 U42A |
| | (3) (2) (1) (15) | P49O A634 4O48 6OH1 | INC2L | (5) (13) (12) (7) | A2AH 21AP 3HA8 UAH2 |
| Counter Two: | | | | (6) (2) (3) | 9AC9 2813 FH82 |
| IDB11 IDB10 IDB9 IDB8 | U411(9) (10) (1) (15) | O53U 349C P682 9376 | | | |
| LDCTR2L | (11) (4) (5) (13) | 5P63 CPH4 PP8P 3O44 | | | |
| | (12) (7) (6) (2) | 9PAC 8OUA 4673 38OO | | | |
| IDB7 IDB6 IDB5 | (3) U410(9) (10) (1) | 6HOA 118O O746 52O4 | | | |

Table A9-4 FFT Signature Analysis Test 2 cont.

| Signal name | IC (pin) | Signature | Signal name | IC (Pin) | Signature |
|--------------|--------------------------------|------------------------------|-----------------------------------|------------------------------|------------------------------|
| Counter MUX: | | | Butterfly Type PLA (U207): | | |
| DIDONE | U311(5) (11) (14) (6) | A7C1 A512 U0F5 4673 | | U207(1) (2) (3) (4) | A7C1 A512 U9F5 958O |
| | (10) (13) | 38OO 6HOA | | (5) (6) | C207 859C |
| ACB10 | (7) | 7U15 | | (7) | 653O |
| ACB9 | (9) | 7FAH | | (8) | P49O |
| ACB8 | (12) | AO33 | LEV0 | (9) | H441 |
| CTR1ENL | (1) | 4POA | LEV1 | (11) | F167 |
| | U310(2) | 958O | LEV2 | (12) | PACU |
| | (5) | C2O7 | TYPE2BF | (15) | 44CP |
| | (11) (14) | 859C 653O | Butterfly Subroutine Address ROM: | | |
| | (3) (6) | 56O3 U4C2 | SCALE0 | U502(10) | 8H36 |
| | (10) (13) | 662A 83C6 | SCALE1 | (11) | C1CP |
| ACB7 | (4) | 86H2 | PASSDONE | (12) | 6052 |
| ACB6 | (7) | O169 | TYPE2BF | (13) | 44CP |
| | (9) | OCH4 | BFSUBADL | (15) | U8F9 |
| ACB5 | (12) | O152 | IDB0 | (1) | 31HP |
| ACB4 | (1) | 4POA | IDB1 | (2) | FBF2 |
| CTR1ENL | U309(2) | P49O | IDB2 | (3) | O6FO |
| | (5) (11) (14) | A634 4O48 6OH1 | IDB3 | (4) | OO1P |
| | (3) | UAH2 | IDB4 | (5) | U7P8 |
| | (6) (10) (13) | 9AC9 2813 FH82 | IDB5 | (6) | 52O4 |
| ACB7 | (4) | 349A | IDB6 | (7) | O746 |
| | (7) (9) (12) | 6AH1 1U59 4282 | IDB7 | (9) | 118O |
| ACB6 | (7) | 6AH1 | | | |
| ACB5 | (9) | 1U59 | | | |
| ACB4 | (12) | 4282 | | | |
| CTR1ENL | (1) | 4POA | | | |

(ACB is address count bus)

Table A9-4 FFT Signature Analysis Test 2 cont.

| Signal name | IC (pin) | Signature | Signal name | IC (Pin) | Signature |
|---------------------|----------|-----------|------------------|----------|-----------|
| Address Translator: | | | Coefficient ROM: | | |
| FFTW | U307(4) | 9758 | FA0 | U412(2) | 4282 |
| SWAP | (5) | P41A | FA1 | (3) | 7H94 |
| | (6) | A7C3 | FA2 | (4) | 46C7 |
| | | | FA3 | (5) | 85PP |
| ACB2 | U314(1) | 6AH1 | | | |
| ACB4 | (2) | O152 | FA4 | (6) | 444H |
| ACB6 | (3) | O169 | FA5 | (7) | F6C8 |
| ACB8 | (4) | AO33 | | (19) | 1411 |
| | (5) | H8A6 | | (18) | 2277 |
| LEV0 | (6) | H441 | | (17) | 5P2H |
| LEV1 | (7) | F167 | | (16) | A57C |
| LEV2 | (8) | PACU | | (15) | U27A |
| | | | | (14) | 6C31 |
| WINDPGL | (9) | FU43 | | | |
| FFTW | (11) | 9758 | FA6 | U413(2) | H289 |
| FA2 | (19) | 46C7 | FA7 | (3) | 5C91 |
| FA4 | (18) | 444H | FA8 | (4) | CPO4 |
| | | | FA9 | (5) | 1P6P |
| FA6 | (17) | H289 | | | |
| FA8 | (16) | C9O4 | FA10 | (6) | 6739 |
| FA10 | (12) | 6739 | FA11 | (7) | H351 |
| | | | FA12 | (8) | O8P8 |
| ACB1 | U313(1) | 1U59 | FA13 | (9) | 3FU7 |
| ACB3 | (2) | 349A | | | |
| ACB5 | (3) | OCH4 | LDCAL | (11) | 3H4O |
| ACB7 | (4) | 86H2 | | (19) | F186 |
| | | | | (18) | PU29 |
| ACB9 | (5) | 7FA4 | | (17) | 2U4O |
| FA1 | (19) | 7H94 | | | |
| FA3 | (18) | 85PP | | (16) | 6AHA |
| FA5 | (17) | F6C8 | | (15) | 47HH |
| | | | | (14) | H351 |
| FA7 | (16) | 5C91 | | (13) | O8P8 |
| FA9 | (12) | 1P6P | | | |
| | | | | | |
| ACB0 | U307(12) | 4282 | | U315(10) | U317(10) |
| PASSBIT0 | (13) | 14AA | | (9) | (9) |
| FA0 | (11) | 4282 | | (8) | (8) |
| | | | | (7) | (7) |
| | | | | | |
| | | | | (6) | (6) |
| | | | | (5) | (5) |
| | | | | (4) | (4) |
| | | | | (3) | (3) |
| | | | | | |
| | | | | (25) | (25) |
| | | | | (24) | (24) |
| | | | | (21) | (21) |
| | | | | (23) | (23) |
| | | | | | |
| | | | | (2) | (2) |

(ACB__ is address count bus;
FA__ is FFT address bus)

Table A9-4 FFT Signature Analysis Test 2 cont.

| Signal name | IC (pin) | Signature |
|----------------------------|----------|-----------|
| Coefficient ROM continued: | | |
| IDB0 | U517(18) | 31HP |
| IDB1 | (17) | F8F2 |
| IDB2 | (16) | O6FO |
| IDB3 | (15) | OO1P |
| IDB4 | (14) | U7P8 |
| IDB5 | (13) | 52O4 |
| IDB6 | (12) | O746 |
| IDB7 | (11) | 118O |
| IDB8 | U518(18) | 9376 |
| IDB9 | (17) | P682 |
| IDB10 | (16) | 349C |
| IDB11 | (15) | O53U |
| IDB12 | (14) | UA51 |
| IDB13 | (13) | HPH7 |
| IDB14 | (12) | FO91 |
| IDB15 | (11) | 77HP |

Return all jumpers to the normal (N) position (either position OK for J1).

3. Digital Signature Test 3

Connect the signature analyzer as described in table A9-5.

Table A9-5 FFT Signature Analyzer Setup #3

| Signal | Polarity | Connection |
|--------|----------|------------|
| Ground | | A7 J5-1 |
| Clock | Pos edge | A7 TP3 * |
| Stop | Neg edge | A7 J5-4 |
| Start | Pos edge | A7 J5-5 |

* note change from test 2

Test 3 is activated by performing the following steps:

- a. Move jumper J2 to the test (T) position.
- b. Move jumper J1 to the TST1 position.
- c. Press the reset switch on the CPU board (A2 S1).

Table A9-6 FFT Signature Analysis Test 3

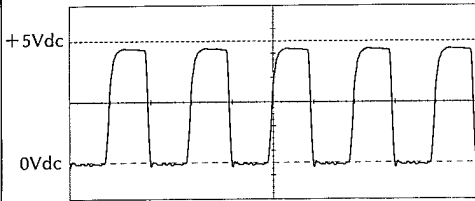
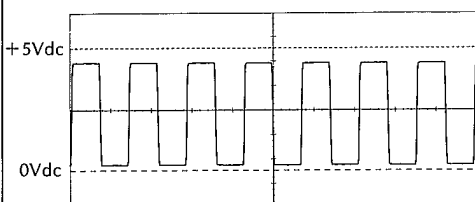
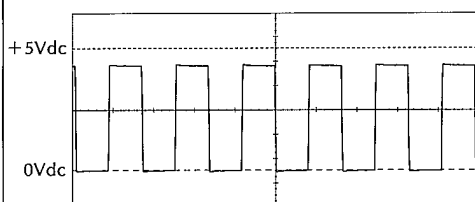
| Signal name | IC (pin) | Signature | Signal name | IC (Pin) | Signature | | |
|---------------------------------------|----------------------------------|------------------------------|------------------------------|------------------------------------|----------------------------------|------------------------------|------------------------------|
| | U315(11) (12) (13) (15) | U517(2) (3) (4) (5) | 47FP 3246 HA4U 9O3F | Global Data Bus Interface Outputs: | | | |
| | (16) (17) (18) (19) | (6) (7) (8) (9) | AP58 OO11 C668 3FO8 | GD15L GD14L GD13L GD12L | U516(19) (18) (17) (16) | U515(2) (3) (4) (5) | 3347 U9FH 3347 U9FH |
| | U317(11) (12) (13) (15) | U518(2) (3) (4) (5) | 6P1C POHU CC3C 4472 | GD11L GD10L GD9L GD8L | (15) (14) (13) (12) | (6) (7) (8) (9) | 3347 U9FH 3347 U9FH |
| | (16) (17) (18) (19) | (6) (7) (8) (9) | PHH1 OHHA H231 OHP6 | GD7L GD6L GD5L GD4L | U514(19) (18) (17) (16) | U513(2) (3) (4) (5) | 3347 U9FH 3347 U9FH |
| PROMINL | U517(1) | U518(1) | FA8A | GD3L GD2L GD1L GD0L | (15) (14) (13) (12) | (6) (7) (8) (9) | 3347 U9FH 3347 U9FH |
| Global Address Bus Interface Outputs: | | | Handshake: | | | | |
| GA16L | | U512(19) | 3347 | FFTMG | | U212(12) | F59A |
| GA15L | | (18) | 18C1 | | | (13) | FA8A |
| GA14L | | (17) | 4UAU | FFTMR | | (11) | OU1O |
| GA13L | | (16) | 7FH4 | | | U211(12,13) | OOOO |
| GA12L | | (15) | U839 | FFTWR | | U501(2) | F59A |
| GA11L | | (14) | A44O | REQGBL | | (3) | FA8A |
| GA10L | | (13) | 4O2O | LDGDBRL | | U214(3) | FA8A |
| GA9L | | (12) | 15PP | GR/GWL | | U211(8) | OU1O |
| GA8L | | U511(19) | 4PP9 | MGFFTL | | U215(13) | OOOO |
| GA7L | | (18) | U5U7 | GDSL | | U214(2) | FA8A |
| GA6L | | (17) | 4291 | MRFFTL | | U211(11) | FA8A |
| GA5L | | (16) | 6F84 | | | | |
| GA4L | | (15) | 3831 | | | | |
| GA3L | | (14) | A997 | | | | |
| GA2L | | (13) | FF53 | | | | |
| GA1L | | (12) | P39F | | | | |

Return all jumpers to the normal (N) position when testing is complete.

C. Oscilloscope Signal Waveforms

The following table of illustrations are oscilloscope plots of digital signature analysis signals (CLOCK and START/STOP) at J5. These should appear on the test pins when the DSA jumpers are in the positions specified in the waveform setup.

Table A9-7 FFT Signal Waveforms

| Jumpers in normal position | | |
|--|--|--|
| Setup | Important Parameters | Waveform |
| <p>CLKOUT (5 MHz)</p> <p>Signal at pin 3 of J5 (CLK on DSA connector)</p> <p>Scale 1 V/div Timebase 100 ns/div Offset 2.5 V Delta V 5 V</p> <p>Trigger Ch 1 Coupling dc</p> | <p>Time period and pulse shape</p> |  <p>#1</p> |
| <p>Put J2 in the test (T) position, J1 in the TST1 position, and press the reset button on the CPU board (A2 S1).</p> | | |
| <p>SRT/STP TST 1 (1.4 Hz)</p> <p>Signal at pin 4 and 5 of J5 (DSA connector)</p> <p>Scale 1 V/div Timebase 500 ms/div Offset 2.5 V Delta V 5 V</p> <p>Trigger Ch 1 Coupling dc</p> | <p>Time period and pulse shape</p> |  <p>#2</p> |
| <p>Put J3 and J4 in the test position and J2 in the TST2 position</p> | | |
| <p>SRT/STP TST 2 (1.2 kHz)</p> <p>Signal at pins 4 and 5 of J5 (DSA connector)</p> <p>Scale 1 V/div Timebase 500 us/div Offset 2.5 V Delta V 5 V</p> <p>Trigger Ch1 Coupling dc</p> | <p>Time period and pulse shape</p> |  <p>#3</p> |

D. After-Repair Adjustments and Tests**Table A9-8 After-Repair Adjustments and Tests**

| Perform the following: | Section |
|-------------------------------|----------------|
| Diagnostic Tests: Test All | VII |
| Adjustments: None | |
| Performance Tests: None | |

